Durand Jarrett-Amor

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EDUCATION

UNIVERSITY OF TORONTO-TORONTO, ON
Doctor of Philosophy - Electrical Engineering September 2017 – Present

RYERSON UNIVERSITY-Toronto, ON
Master of Applied Science - Electrical Engineering November 2017
Bachelor of Engineering (Honours) - Electrical Engineering June 2015

UNIVERSITY OF WATERLOO-Waterloo, ON June 2009
Bachelor of Science Degree - Honours Physics, Pure Mathematics Minor

RESEARCH EXPERIENCE

M.A.Sc. Student - Ryerson University, Toronto, ON January 2016 – June 2017
Integrated Circuits and Systems Research Group

- Designed and implemented a 0.1µW integrating frequency difference detector (iFDD) in IBM 130nm, 1.2V CMOS technology
- Researched frequency-to-voltage converters, frequency-locked loops (FLLs), and passive wireless microsystems to design a low-power iFDD for application in FLLs
- Performed a mathematical analysis to describe the time and frequency domain behaviour of the iFDD to demonstrate that the FLL had no steady-state frequency error
- Verified the theoretical findings through transient simulations of the output voltage of the iFDD and the frequency error of the FLL using SpectreRF
- Performed PVT analysis using SpectreRF to verify robustness of FLL across all corners

M.A.Sc. Student - Ryerson University, Toronto, ON September 2015 – January 2016
Integrated Circuits and Systems Research Group

- Designed and implemented a phase-locked loop (PLL) that used time amplification to shorten the lock time of the PLL in IBM 130nm, 1.2V CMOS technology
- Researched time amplifiers (TAs) and PLLs with fast lock times
- Demonstrated that the PLL with the TA could achieve lock times up to 2 times faster than the PLL without the TA
- Published conference paper in IEEE ISCAS 2016 conference in Montreal

Undergraduate Research Assistant - Ryerson University, Toronto, ON May 2014 – July 2015
Integrated Circuits and Systems Research Group

- Researched and developed a current-integrating bang-bang phase-locked loop (IBBPLL) for clock and data recovery in IBM 130nm, 1.2V CMOS technology
- Researched bang-bang phase detectors and the effect of transient disturbances on CMOS circuits
- Demonstrated the superior transient noise rejection of the IBBPLL to a phase-locked loop implemented with a full-rate Alexander phase detector
- Published conference paper in IEEE NEW Circuits and Systems 2016 conference in Vancouver

Undergraduate Research Assistant - Ryerson University, Toronto, ON May 2013 – August 2013
Integrated Circuits and Systems Research Group

- Researched cyclic, pulse-shrinking time-to-digital converter architectures
- Developed a pulse-shrinking circuit element to shrink the width of a square-wave pulse
- Implemented the circuit in IBM 130nm, 1.2V CMOS technology
- Analyzed and verified the circuit's ability to shrink the width of square-wave pulses using SpectreRF
- Communicated research results to supervisor in 1-3 page weekly progress reports

JOURNAL PUBLICATIONS

- **D. Jarrett-Amor**, and F. Yuan, "Low-power integrating frequency difference-to-voltage converter with applications in injection-locked FLL," *Analog Integrated Circuits and Signal Processing*, vol. 95, no. 1, pp. 53-65, Apr. 2018.

CONFERENCE ABSTRACTS

- **D. Jarrett-Amor**, and F. Yuan, "Data Transient Insensitive Phase-Locked Loops," *Proc. IEEE NEW Circuits and Systems*, pp.1-4, Vancouver, 2016.

CONFERENCE PROCEEDINGS

- **D. Jarrett-Amor**, and F. Yuan, "Frequency Calibration of Passive Wireless Microsystems using a Low-Power Frequency-Locked Loop." Created and presented poster in Teledyne DALSA Componentware/CAD Award category at TEXPO Graduate Student Competition & Exposition, Montreal, Quebec, 17 October, 2016.
- Y. J. Park, **D. Jarrett-Amor**, and F. Yuan, "Time Integrator for Mixed-Mode Signal Processing," *Proc. IEEE Int'l Symp. Circuits and Systems*, pp. 816-829, Montreal, 2016.
    - Researched papers on time integrators and assisted in writing the introduction of the paper
- **D. Jarrett-Amor**, Y. J. Park and F. Yuan, "Time-Mode Techniques for Fast-Locking Phase-Locked Loops," *Proc. IEEE Int'l Symp. Circuits and Systems*, pp. 1790-1793, Montreal, 2016.
    - Created presentation for lecture at IEEE ISCAS conference, Montreal, Quebec, 24 May, 2016.

INVITED JOURNAL REVIEWS

- *Electronic Letters* 2019
    - Manuscript: "10 GHz all-digital bang-bang phase-locked loop with double-path adaptive loop gain controller"

HONOURS AND AWARDS

University of Toronto

- NSERC PGS D3 2018 – 2021
- Edward S. Rogers Sr. Graduate Scholarship 2017, 2018
- Queen Elizabeth II Graduate Scholarship in Science and Technology 2017

Ryerson University

- Ontario Graduate Scholarship 2015 – 2016
- Graduate Research Excellence Award 2016
- Department of Electrical and Computer Engineering Academic Excellence Award 2014
- Capstone Design Project Excellence Award 2014
- Dean's List in Faculty of Engineering and Architectural Science 2011, 2012, 2014
- Ryerson Student Scholar 2011 – 2015

TEACHING EXPERIENCE

- **Teaching Assistant** – University of Toronto, Toronto, ON September 2019 – Present
  ECE 430, Analog Integrated Circuits
- **Teaching Assistant** – University of Toronto, Toronto, ON September 2019 – Present
  ECE 360, Electronic Circuits
- **Teaching Assistant** – University of Toronto, Toronto, ON September – December 2018
  ECE 360, Electronic Circuits
- **Teaching Assistant** - Ryerson University, Toronto, ON January – April 2017
  ELE 614, CMOS Analog Integrated Circuits
- **Teaching Assistant** - Ryerson University, Toronto, ON January – April 2017

ELE 404, Electronic Circuits I

- **Lead Teaching Assistant** - Ryerson University, Toronto, ON — September – December 2016
  ELE 504, Electronic Circuits II
- **Teaching Assistant** - Ryerson University, Toronto, ON — January – April 2016
  ELE 404, Electronic Circuits I
- **Teaching Assistant** - Ryerson University, Toronto, ON — September – December 2015
  ELE 504, Electronic Circuits II
- **Teaching Assistant** - Ryerson University, Toronto, ON — January – April 2015
  ELE 404, Electronic Circuits I

TECHNICAL SKILLS

- Cadence Design Systems
- Multisim
- HSPICE
- MATLAB
- Simulink
- VerilogA

PROFESSIONAL DEVELOPMENT

- APS1203: Teaching Engineering in Higher Education — January – June 2019
  University of Toronto, Toronto, ON
- Prospective Professors in Training Program — January – June 2019
  University of Toronto, Toronto, ON

SERVICE ACTIVITIES

- Vice Chair of the IEEE Circuits and Devices Chapter — May 2019 – Present
  Region 7, Toronto Section
- Engineering Graduate Education Committee — December 2018 – May 2019
  University of Toronto, Toronto, ON
- Electrical and Computer Engineering Department Council Member — September 2016 – 2017
  Ryerson University, Toronto, ON
- Graduate Program Council Member — September 2015 – January 2017
  Ryerson University, Toronto, ON

PROFESSIONAL MEMBERSHIPS

- IEEE Circuits and Systems Member — January 2017 – Present
- IEEE Solid-State Circuits Society Member — January 2016 – Present
- IEEE Student Member — March 2011 – Present