Durand Jarrett-Amor

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EDUCATION

UNIVERSITY OF TORONTO-TORONTO, ON
Doctor of Philosophy - Electrical Engineering September 2017 – Present

RYERSON UNIVERSITY-Toronto, ON
Master of Applied Science - Electrical Engineering November 2017
Bachelor of Engineering (Honours) - Electrical Engineering June 2015

UNIVERSITY OF WATERLOO-Waterloo, ON June 2009
Bachelor of Science Degree - Honours Physics, Pure Mathematics Minor

WORK EXPERIENCE

Analog and Mixed-Signal Design Engineer, Staff
Marvell Technology Canada, Toronto, ON, Canada Start June 24 2024 –

Analog Engineer Intern
Intel Technology Canada, Toronto, ON, Canada June 27 2022 – January 28 2023

- Created test lists for level-shifters and power supply detection to verify specifications are met for each block for 116G SerDes project
- Created testbenches in Cadence for level-shifters, power supply detection, and ADPLL for 116G SerDes project
- Verified level-shifters, programmable divider for PLL, and power supply detection blocks satisfied transient functionality specifications across PVT, aging, and Monte Carlo using Cadence for 116G SerDes project
- Verified level-shifters, programmable divider for PLL, and power supply detection satisfied electrical overstress performance requirements for 116G SerDes project
- EM flow verification of level-shifters in Cadence for 116G SerDes project
- Fixed design of low-voltage-to-low-voltage level-shifter to pass electrical overstress tests for 116G SerDes project

RESEARCH PROJECTS

Passive Hybrid Transceiver (TRX) for Simultaneous Bidirectional (SBD) Signaling in 16-nm FinFET
University of Toronto, Ph.D. Candidate 2019 – 2022

- Successfully designed and verified a 32 Gbps, 0.4pJ/bit TRX for single-ended SBD signaling in ultra-short reach (USR) links
- Created and analyzed a general SBD link model to obtain signal integrity constraints
- Verified and tested SBD link model using Matlab
- Designed a passive filter to remove echo in SBD signaling
- Designed a low-power, high-speed transimpedance voltage-mode driver to minimize signal reflections and power consumption
- Developed top-level floorplan for placement of the TRX system
- Completed and verified layout of driver and passive filter via extracted transient and AC simulations using Spectre

- Completed and verified power routing for the TRX system via extracted AC simulations using Spectre
- Integrated and verified top-level via top-level testbench transient simulations using Spectre
- Documented progress via design review presentations with Huawei design team

Low Power, Integrating Frequency Difference-to-Voltage Converter in IBM 130-nm CMOS
Ryerson University, M.A.Sc Candidate 2018

- Designed and verified a sub-microwatt switched-capacitor integrating frequency difference-to-voltage converter for frequency calibration of a frequency-locked loop for low power biomedical applications
- Published a journal paper in Analog Integrated Circuits and Signal Processing

Time-Mode Phase-Locked Loop (PLL) in IBM 130-nm CMOS
Ryerson University, M.A.Sc Candidate 2016

- Designed a variable-gain time amplifier that dynamically changed the loop dynamics of a PLL
- Designed and verified a fast-locking (<1μs locking time) time-mode PLL in 130-nm CMOS
- Published a conference paper in the International Symposium on Circuits and Systems conference

Current-Integrating Bang-Bang Phase-Locked in IBM-130nm, 1.2 V CMOS
Ryerson University, B.Eng–Research Assistant 2014 – 2015

- Researched and implemented a current-integrating bang-bang phase-locked loop (IBBPLL) for clock and data recovery in IBM-130nm, 1.2 V CMOS technology
- Compared the transient noise rejection of the IBBPLL to a phase-locked loop implemented with a full-rate Alexander phase detector (BBPLL) using Spectre with BSIM4 device models
- Completed project by publishing co-authored paper in IEEE NEWCAS

ACADEMIC PROJECTS

ECE 1392H – Integrated Circuits for Data Communication, University of Toronto 2018
Phase Rotator for Clock and Data Recovery in TSMC 65nm

- Implemented and tested in TSMC 65-nm, 1.2V CMOS technology the phase rotator in the 2016 ISSCC paper "A 16-Gb/s 1 IIR + 1 DT DFE Compensating 28dB Loss with Edge-Based Adaptation Converging in 5μs"
- Summarized results of the project in a 12-page report and a class presentation

ECE 1371H – Advanced Topics in Analog Circuits, University of Toronto 2018
A 14-bit 3rd-order 9-level 32 OSR CRFB $\Delta\Sigma$ ADC

- Designed, implemented, and tested in TSMC 180-nm, 1.8V CMOS technology a 3rd-order, 9-level, 32 OSR cascade-of-resonators feedback delta-sigma ADC to achieve a Figure-of-Merit of 159.79 dB
- Summarized the results of the project in a 28-page report and a class presentation

ELE 724 – CMOS Mixed-Mode Circuits, Ryerson University 2014
Dependent Transient Noise Rejecting Bang-Bang Phase-Locked Loop

- Designed and implemented a bang-bang phase-locked loop (BBPLL) in IBM 130-nm, 1.2V CMOS technology that could reject data transients present on the incoming data signal
- Compared the BBPLL to a linear phase-frequency detector PLL by analyzing each circuit's ability to reject data transients using SpectreRF
- Performed four-corner analysis of both circuits using SpectreRF
- Summarized the results of the project in a 26-page report

ELE 863 – VLSI Systems and Circuits for Data Communications, Ryerson University 2014

A Type-II PLL Frequency Synthesizer

- Designed and implemented a type-II PLL frequency synthesizer with a divide-by-4 in feedback loop in IBM 130-nm, 1.2V CMOS technology
- Successfully generated a 1GHz clock from a 250MHz reference clock
- Summarized the results of the project in a 22-page report

RELEVANT COURSE WORK

Univeristy of Toronto

- ECE 1371H – Advanced Topics in Analog Circuits 2018
- ECE 1392H – Integrated Circuits for Digital Communications 2018
- ECE 1352H – Analog Circuit Design I 2018
- ECE 1388H – VLSI Design Methodology 2017

Ryerson University

- ELE 724 – CMOS Analog Integrated Circuits 2014
- ELE 863 – VLSI Systems and Circuits for Data Communications 2014

TECHNICAL SKILLS

- Cadence Design Systems
- HSpice
- Matlab
- ADS
- Simulink

PUBLICATIONS

- **D. Jarrett-Amor**, K. Yadav, D. Zhang, B. Yang, S. Jalali, and T. C. Carusone, “A 32 Gb/s, 0.42 pJ/bit Passive Hybrid Simultaneous Bidirectional Transceiver for Die-to-Die Links,” in *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2023, pp. 1–5. doi: 10.1109/ISCAS46773.2023.10181991.
- **D. Jarrett-Amor**, and F. Yuan, “Low-power integrating frequency difference-to-voltage converter with applications in injection-locked FLL,” *Analog Integrated Circuits and Signal Processing*, vol. 95, no. 1, pp. 53-65, Apr. 2018.
- **D. Jarrett-Amor**, and F. Yuan, "Data Transient Insensitive Phase-Locked Loops," *Proc. IEEE NEW Circuits and Systems*, pp.1-4, Vancouver, 2016.
- Y. J. Park, **D. Jarrett-Amor**, and F. Yuan, "Time Integrator for Mixed-Mode Signal Processing," *Proc. IEEE Int'l Symp. Circuits and Systems*, pp. 816-829, Montreal, 2016.
- **D. Jarrett-Amor**, Y. J. Park and F. Yuan, "Time-Mode Techniques for Fast-Locking Phase-Locked Loops," *Proc. IEEE Int'l Symp. Circuits and Systems*, pp. 1790-1793, Montreal, 2016.

HONOURS AND AWARDS

University of Toronto

- NSERC PGS D3 2018 – 2021
- Edward S. Rogers Sr. Graduate Scholarship 2017 – 2021
- Queen Elizabeth II Graduate Scholarship in Science and Technology 2017

Ryerson University

- Ontario Graduate Scholarship 2015 – 2016
- Graduate Research Excellence Award 2016

- Department of Electrical and Computer Engineering Academic Excellence Award 2014
- Capstone Design Project Excellence Award 2014
- Dean's List in Faculty of Engineering and Architectural Science 2011, 2012, 2014
- Ryerson Student Scholar 2011 – 2015

PROFESSIONAL MEMBERSHIPS

- IEEE Member January 2022 – Present
- IEEE Electron Devices Society Member January 2021 – Present
- IEEE Electron Packaging Society Member January 2021 – Present
- IEEE Circuits and Systems Member January 2017 – Present
- IEEE Solid-State Circuits Society Member January 2016 – Present
- IEEE Student Member March 2011 – 2021

SERVICE ACTIVITIES

- Chair of the IEEE Circuits and Devices Chapter May 2023 – Present
  Region 7, Toronto Section
- Vice Chair of the IEEE Circuits and Devices Chapter May 2019 – May 2023
  Region 7, Toronto Section
- Engineering Graduate Education Committee December 2018 – May 2019
  University of Toronto, Toronto, ON
- Electrical and Computer Engineering Department Council Member September 2016 – 2017
  Ryerson University, Toronto, ON
- Graduate Program Council Member September 2015 – January 2017
  Ryerson University, Toronto, ON