24 GHz LOW-NOISE AMPLIFIERS USING HIGH Q SERIES-STUB TRANSMISSION LINES IN 0.18 μm CMOS

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Abstract

Single-ended and differential low-noise amplifiers (LNAs), designed in 0.18 μm CMOS for operation at 24 GHz, are introduced in this paper. Novel, high-Q series-stub transmission lines (SSTLs) are used in the matching networks of both LNAs. This SSTL structure shows a notable Q factor improvement over the commonly used spiral inductor, which helps to minimize the losses and noise produced in the LNA matching networks, making these topologies suitable for sensitive receiver front ends.

The single-ended amplifier uses two cascode stages to help improve gain and reverse isolation when compared to common source stages. Results show that the cascode LNA is able to produce an excellent compromise between ease of design, gain and noise. After optimizing transistor sizes to produce minimum noise, the single-ended amplifier produces a simulated noise figure of only 4.9 dB and a gain of 17.4 dB. The differential LNA uses two capacitively neutralized stages to improve reverse isolation. Chip production has been delayed by the foundry, but simulated results of the differential LNA show an excellent noise figure of 4.2 and a gain of 12.3 dB.

Keywords*—LNA; transmission lines; inductor; cascode.*

1 Introduction

As CMOS technology sizes continue to scale downwards in size, the speed of the analog circuitry designed in it climbs by roughly one order of magnitude every ten years [1]. While this means that that CMOS can now provide an attractive alternative to GaAs or SiGe technologies, even at frequencies above 20 GHz, it also means that several obstacles to RF circuit design that could once be neglected are now becoming more problematic. One such problem is the fact that as gate lengths continue to decrease, the gate-drain overlap capacitance C_{gd}, which is a product of the lateral diffusion of the drain dopant under the polysilicon gate material, remains relatively constant. As a result, C_{gd} now comprises a sizable portion of the total MOSFET input capacitance and amplifier designers can no longer neglect its effects. Since C_{gd} adds a (noninverting) signal path between the gate and drain terminals of the MOSFET, it is detrimental in that it reduces both forward gain and reverse isolation [2].

A second unavoidable trend associated with the evolution of CMOS technology is the fact that on-chip passive structures such as Metal-Insulator-Metal (MIM) capacitors and spiral inductors often account for the majority of the chip area consumed. Spiral inductor structures are of particular concern since they not only require a tremendous amount of chip space, but also contribute heavily to the loss and noise generated by the circuit at frequencies above 20 GHz.

This paper addresses both of the above issues. Firstly, Section 2 introduces a novel series-stub transmission line (SSTL) inductor architecture, which improves the inductor Q factor without requiring the excessively large chip area often required by transmission line inductors. Next, Section 3 explores the use of these inductors in a Low-Noise Amplifier (LNA), which uses a cascode topology to improve reverse isolation. Section 4 then briefly introduces ongoing work on a differential LNA structure.

	Inductance (nH)	Q Factor
Asitic	188	5.402
Momentum	362	12.358
Measured	351	7.429

TABLE I
MODELING OF A SINGLE-TURN, 100 μM DIAMETER, 15 μM TRACE WIDTH, SQUARE SPIRAL INDUCTOR AT 24 GHZ.

2 On-Chip Inductors

2.1 Spiral Inductors

Spiral inductors have traditionally offered the most compact, and therefore economical, means of producing an on-chip inductor in CMOS circuit design. Their use in the low gigahertz range has been well characterized and through the efforts of many recent publications, summarized in [3] and [4], their optimization and implementation has become fairly straight forward in this frequency range. However, as operating frequencies surpass 20 GHz, the behaviour of spiral inductors becomes more complex due to the fact that (a) substrate eddy currents become more prevalent and limit the Q factor and (b) magnetic coupling to the substrate begins to have a significant effect on the overall inductance value [1].

Since both of the above factors require a detailed knowledge of the substrate profile to be accurately modeled, optimization and implementation of spiral inductors at these frequencies becomes a non-trivial concern for the circuit designer. To illustrate this, Table I shows the measured inductance and Q Factor of a single-turn, 100 μm diameter, square spiral inductor and compares these results to an electromagnetic (EM) simulation conducted in ADS Momentum and a pie-model based simulation conducted in Asitic. The apparent differences highlight the non-trivial nature of high-frequency spiral inductor modeling, resulting an undesirable degree of uncertainty when using such structures in circuit designs.

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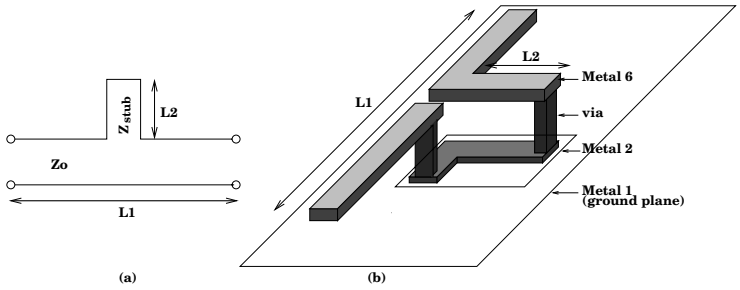

Figure 1. The (a) equivalent circuit of transmission line with series stub and (b) proposed CMOS implementation.

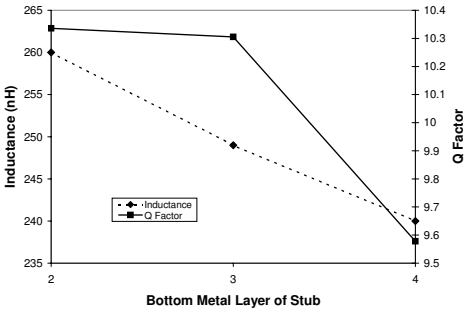

Figure 2: Choice of the series-stub bottom metal layer.

2.2 SSTL Inductors

As an alternative to spiral inductors, transmission lines can also provide an equivalent on-chip inductance. Microstrip transmission lines are particularly attractive to circuit designers since these structures employ the use of a ground plane on a low metal layer, shielding the structure from the substrate. This results in substantially confined electric and magnetic fields and hence simplifies modeling considerably [1]. The downside, which has limited the usefulness of using microstrips as inductors, is the fact that the line lengths required to achieve the necessary inductance values can be prohibitively long.

Traditionally, the addition of a series-stub section to a microstrip line, as illustrated in Figure 1.(a), does not reduce the chip area consumed by the transmission line and is difficult to implement due to the need for an isolated ground reference. Figure 1.(b) illustrates the novel SSTL structure introduced in this section, which takes advantage of the 3-dimensional aspect of multiple metal layers in CMOS technology. This not only reduces the required length of transmission line $L1$ by twice the length of the series stub ($2 * L2$), but also reduces the chip area consumed by the inductor without sacrificing too much Q Factor.

By removing a section of the Metal 1 ground plane directly beneath the series-stub, the capacitance to the ground plane is minimized thereby maximizing the SSTL inductance. This in turn allows for a small amount of coupling to the substrate and raises the question as to whether the lower layer of the series-stub should be placed on a high metal layer so as to reduce this substrate coupling, or on a low metal layer so as to reduce the capacitance between this line and the upper layer of the series-stub. Full EM simulations of an SSTL inductor with a main transmission line length of 500 μm and a stub length of 100 μm (and therefore equivalent line length of 700 μm) were conducted to test the effects of the choice of metal layer for the lower layer of the series-stub. These results, which are displayed in Figure 2, display a uniform decrease in both the total inductance and Q Factor of the SSTL inductor as the bottom metal layer is moved farther from the substrate. This indicates that the capacitive coupling between the top and bottom layers of the series-stub is more significant than any substrate losses incurred and justifies the choice of the use of metal 2 in the SSTL structure.

With the SSTL inductor structure optimized, an in-depth analysis of its inductive behaviour was conducted. Since microstrip

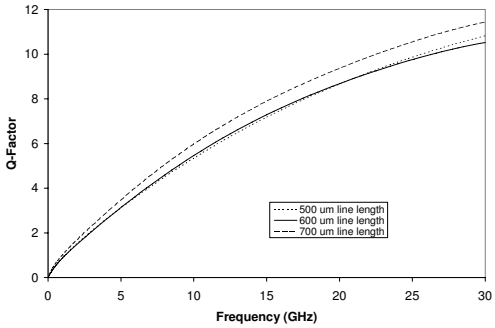

Figure 3: Simulated Q Factor of SSTL inductors.

structures inherently shield the transmission line from the substrate, the only sources of resistive loss that remain are a small amount of coupling to the substrate in the series-stub area, and the ohmic resistance of the line itself. The overall effect of this is that the Q factors of SSTL structures are weakly independent of the line length and hence the inductance value. This contrasts sharply with spiral inductor structures where longer line lengths lead to increased substrate coupling and hence lower Q. Also, since the substrate coupling is limited to a very small area, one can intuitively see that the reactive portion of the impedance should increase more quickly than the resistive portion over a very wide frequency range. This dictates that the Q Factor of the device ($Q = \omega L/R$) should also increase over the same frequency range. This behaviour is verified by the EM simulation results in Figure 3, which display a monotonically increasing Q Factor with a variation of less than 1 as the equivalent line length is varied from 500 μm to 700 μm.

Measurements were completed on an Agilent 8510 vector network analyzer (VNA). These results are displayed in Figure 4 and show a good correlation between simulated and measured results for the 500 μm long SSTL inductor, but show that as the equivalent line length is increased to 600 μm, the measured Q Factor begins to drop away at high frequencies. This is likely due to inadequate modeling of the skin effect, which will increase the ohmic resistance of the transmission line at high frequencies.

The second parameter of importance, the inductance value itself, also shows a strong correlation to simulated data, as can be seen in Figure 5. This therefore validates the assertion that the

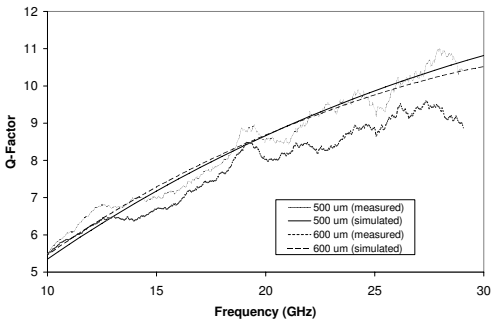

Figure 4: Simulated vs measured SSTL Q Factor.

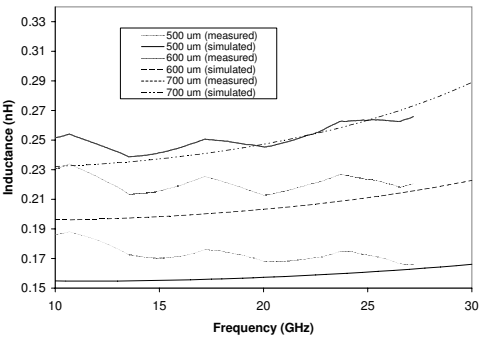

Figure 5: Simulated vs measured SSTL inductance.

SSTL inductor structure lends itself more effectively to modeling and optimization. In addition, Figure 6 compares the measured Q Factor of SSTL inductors to spirals of approximately the same surface area and shows a distinct high frequency advantage in favour of the SSTL structure. As a result of these two factors, the SSTL inductor provides a very attractive alternative to spiral inductors at frequencies above 20 GHz.

3 Cascode Low-Noise Amplifier

As described in the introduction, the gate to drain capacitance inherent to MOSFET devices is of growing concern as CMOS operating frequencies venture beyond 20 GHz. This capacitance

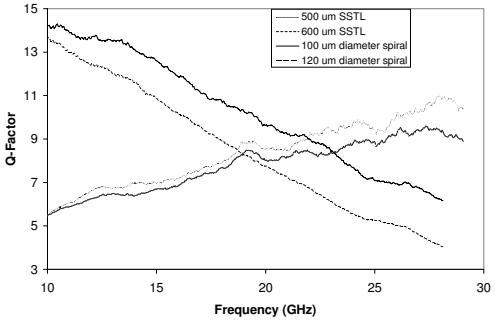

Figure 6: Q Factors of SSTL and spiral inductors.

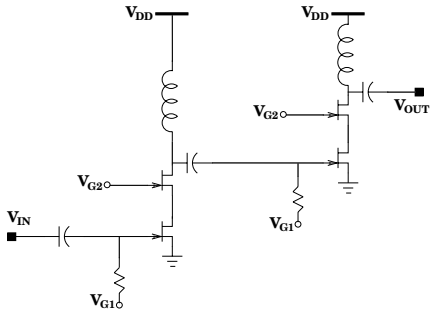

Figure 7: Basic circuit schematic for the cascode LNA.

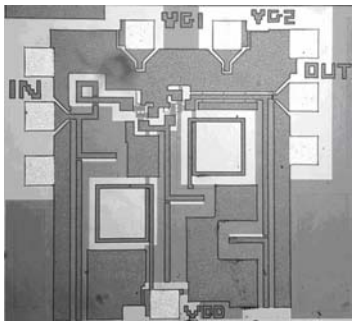

Figure 8: Chip photograph.

introduces a feedback path, which not only increases the potential for amplifier instability, but also makes it very challenging to accurately design optimal matching networks since most LNA design techniques require input and output networks to be considered separately [5]. One amplifier topology that is well-known for its ability to mitigate feedback and improve reverse isolation is the cascode configuration. Although fairly common in lower frequency ranges, the cascode structure has seen limited use in recent literature due to the fact that a two-transistor stack is not optimal for low voltage applications and that the addition of a common-gate stage inherently adds a small amount of noise.

The basic circuit diagram including bias networks of the single-ended, 24 GHz LNA presented in this section is shown in Figure 7. It uses a two-stage cascode structure, in combination with the high-Q SSTL inductors presented in the previous section, in an attempt to show that the cascode configuration can be used to mitigate the effect of the overlap capacitance while still providing a noise figure amongst the lowest presented in standard 0.18 μm CMOS technology. Figure 8 shows a photograph of the 800 μm x 800 μm chip (including pads), which gives a clear picture of the implementation of the SSTL inductors and their integration with the other circuit components.

Simulated and measured s-parameter data for this circuit are presented in Figure 9. Simulated data at 24 GHz shows the amplifier to have an excellent gain and output return loss of 17.4 dB and 19.9 dB respectively. The input, which is designed for minimum noise, shows an input return loss of 4.9 dB and, as expected, the cascode structure provides an impressively high reverse isolation of 43.7 dB. In addition, the simulated noise fig-

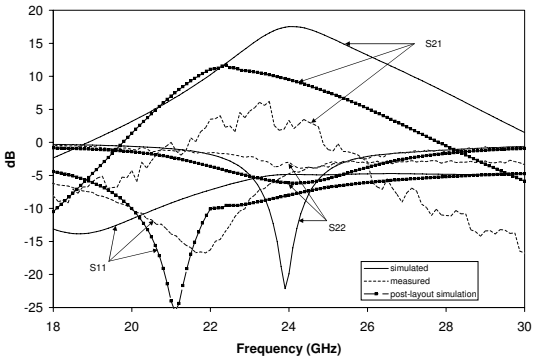

Figure 9: S-parameters of the cascode LNA.

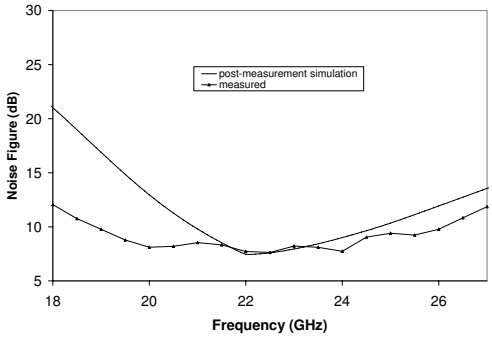

Figure 10: Measured and post-measurement simulation NF performance.

ure is 4.9 dB, which ranks amongst the best performance of other LNAs in recent literature [6]-[7].

S-parameter measurements were completed using an Agilent 8510 VNA while an Agilent 4446A spectrum analyzer was used for noise figure measurement. S-parameter results show that although the amplifier does achieve gain at the correct frequency, there is notable discrepancy between the measured and simulated curves. In particular, the output return loss of approximately 3 dB is much lower than simulated results. Post-layout simulation has revealed that a problem in the original EM simulation resulted in the use of a spiral inductor that was beyond resonance in the drain bias network of the first LNA stage. By including the effects of this inductor in simulation both the s-parameter results, included in Figure 9, and noise figure results, shown in Figure 10, show a good match to measured data. This is encouraging as it indicates that the noise model used for circuit design is accurate and that, after fixing the bias inductor error, the circuit performance should resemble the original simulation results very closely.

4 Differential Low-Noise Amplifier

Research is currently being conducted regarding a differential amplifier topology which also makes use of the SSTL inductors and attempts to improve gain and reverse isolation through the use capacitive neutralization. Simulated results indicate that this LNA design should provide a gain of over 12 dB and a noise figure of only 4.2 dB, which to the author's knowledge, is the lowest noise figure reported for any differential LNA in standard 0.18 μm CMOS. Unfortunately, the run to which the design was submitted was unexpectedly deferred, meaning that measured data is not yet available.

5 Conclusions

A novel SSTL inductor structure with Q Factors above those available from standard spiral inductors has been presented for use at frequencies above 20 GHz. These inductors were then implemented in a 24 GHz cascode LNA, which has been designed, fabricated and tested in TSMC standard 0.18 μm CMOS process. The LNA achieves a gain of 17.4 dB, a noise figure of 4.9 dB, an input return loss of 4.9 dB and an output return loss of 19.9 dB in simulation. Measured results could not verify simulation due to an error in the spiral inductor used to bias the first stage of the LNA. However, adjusting the simulation to mimic these errors provides a noise figure of 9 dB, which is very close to the measured data, indicating that correcting the bias inductor problem will achieve results close to what simulations predict.

Acknowledgments

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