Accumulation-Mode MOS Varactors for RF CMOS Low-Noise Amplifiers

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***Abstract*— A new RF model for an AMOS varactor is presented for 0.18 μm CMOS. This model is the first reported for frequencies above 20 GHz in a standard CMOS technology. It does not rely on boundary conditions for different modes of operation and all component values in the model are calculated using clearly defined physical equations, making it easily adaptable to any varactor layout or even other CMOS technology nodes. The presented varactors are then implemented as neutralizing capacitances in a 23 GHz, two-stage, differential low-noise amplifier (LNA) design. Measured results of the fabricated LNA include a peak gain of 7.7 dB and a minimum noise figure of 4.5 dB at a frequency of approximately 23 GHz.**

I. Introduction

By tying the source, drain and bulk terminals of a MOSFET together and varying the voltage applied between the resulting terminal and the gate, the charge layer beneath the gate oxide in a standard NMOS transistor will vary. This creates a capacitance between the heavily doped n^+ polysilicon gate electrode and the drain/source/body connection that can be easily tuned by varying a single DC voltage.

It is possible to modify the NMOS device such that it is limited to operation in the accumulation and depletion regions only, allowing the circuit designer to tune the varactor between a high and low capacitance value over a large range of bias voltages. Such a varactor is known as an Accumulation-mode MOS (AMOS) varactor and can be created by placing the n^+ diffusion regions of an NMOS device in an n well region. The resulting varactor is illustrated by a cross-section of the device in Figure 1.

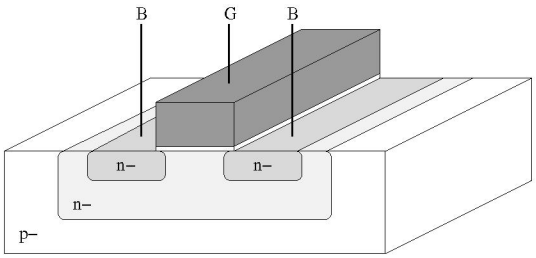

Fig. 1. Cross-section of an AMOS varactor.

The resulting capacitance seen between the varactor terminals, C_{var}, can then be roughly approximated according to the equation

$$C_{var} = W_{eff} L_{eff} \frac{C'_{ox} C'_{dep}}{C'_{ox} + C'_{dep}} n \tag{1}$$

where L_{eff} is the effective channel length, W_{eff} is the effective channel width, n is the number of gate fingers used and C'_{ox} and C'_{dep} are the capacitances per unit area of the oxide and depletion regions, respectively.

II. AMOS Varactor Modeling

Recent publications that have explored the varactor modeling challenge suffer from at least one of the following difficulties:

- They rely on components which are derived from extracted data, as can be seen in [1], and often use non-physical, curve-fitting parameters.
- They employ separate models for the various operating regimes, making their use extremely difficult in circuit simulation.

In this paper, a new AMOS varactor model is presented that addresses each of these issues. The final model is shown in Figure 2 and is followed by an in-depth analysis of all the parasitics associated with the AMOS varactor, which is essential to producing a accurate results.

A. Channel Capacitance

When the voltage seen at the gate terminal drops below the voltage of the channel, a depletion region begins to form beneath the gate oxide. The width of this depletion region varies with the magnitude of the voltage difference, creating an additional capacitance, C_{dep}, in series with the gate-channel capacitance, C_{gc}, which reduces the total capacitance seen. If we define the effective gate area A_g as

$$A_g = L_{eff} W_{eff} \tag{2}$$

then the width of the depletion region can be calculated as [2]

$$w_d = \sqrt{\frac{2\epsilon_{si}}{qN_{well}}} \sqrt{V_{eff} - \frac{Q_{dep}}{C'_{ox} A_g}} \tag{3}$$

where ϵ_{si} is the permittivity of silicon, q is the elementary charge and N_{well} is the carrier concentration of the n well

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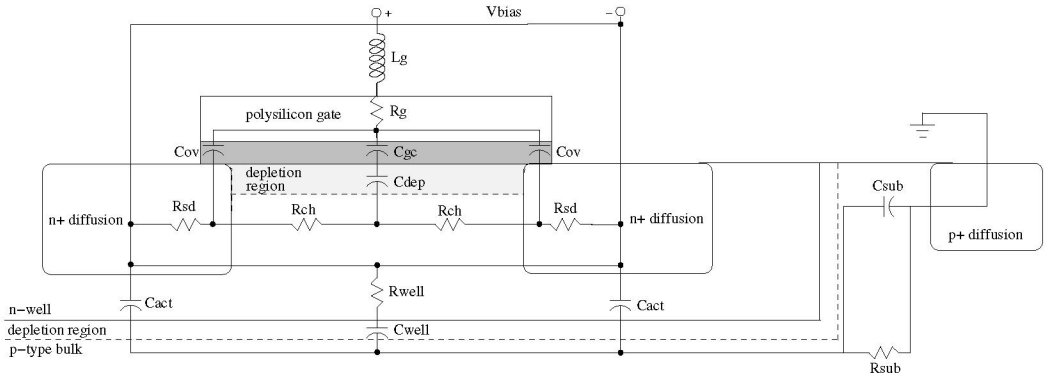

Fig. 2. Cross-section of an AMOS varactor showing the lumped element components used in this model.

region. Q_{dep} is the depletion region charge, which is calculated as

$$Q_{dep} = qN_{well}w_dA_g \tag{4}$$

Finally, V_{eff} represents the effective voltage seen across the variable capacitance and is used to ensure that Q_{dep} approaches zero with the device being driven into accumulation. It can be calculated by [2]

$$V_{eff} = \frac{1}{2}\left(\sqrt{V_{bias}^2 + \delta_d} - V_{bias}\right) \tag{5}$$

where V_{bias} is the applied bias voltage and δ_d is used to determine the speed at which w_d (and hence C_{dep}) changes with the applied voltage and is usually chosen to have a value of approximately 0.01.

By substituting equation (3) into equation (4) we obtain the following result for the depletion region charge

$$Q_{dep} = -qN_{well}\frac{\epsilon_{si}}{C'_{ox}}A_g \pm \sqrt{q^2N_{well}^2\frac{\epsilon_{si}^2}{\left(C'_{ox}\right)^2}A_g^2 + 2qN_{well}\epsilon_{si}V_{eff}A_g^2} \tag{6}$$

Then, by using this expression in equation (3) we obtain a continuous function for w_d at any applied bias voltage. Although this function never reaches zero regardless of the bias voltage applied, w_d is very small for positive gate voltages. Since C_{dep} is simply calculated as

$$C_{dep} = \frac{\epsilon_{si}}{w_d}A_gn \tag{7}$$

this implies that C_{dep} actually increases as w_d decreases. Then, by examining equation (1), it becomes apparent that as C_{dep} continues to increase, its effect on the overall capacitance decreases and eventually becomes negligible.

B. Overlap Capacitance

The second major contributor to the capacitance seen between the varactor terminals is the overlap capacitance, C_{ov}, created by the overlap of each gate finger over the n^+ diffusion regions. To model this contribution, we begin by calculating the actual parallel plate capacitance of the overlap as

$$C_{pp} = C'_{ox}W_{eff}L_{ov}n \tag{8}$$

where L_{ov} is the length of the overlap region on one side of the channel.

Secondly, we examine the extrinsic fringing capacitance, C_{ext}, which is calculated using the following equation from [4]

$$C_{ext} = \frac{2}{\pi}\epsilon_{ox}\ln\left(\frac{t_{poly}}{t_{ox}}\right)W_{eff}2n \tag{9}$$

where t_{poly} is the thickness of the polysilicon gate material and t_{ox} and ϵ_{ox} are the thickness and permittivity of the gate oxide, respectively.

Although the top side of the gate is separated from the diffusion region by at least $t_{poly} + t_{ox}$, it can also have a significant effect on the overlap capacitance, and can be calculated using [3]

$$C_{top} = \epsilon_{ox}\ln\left(1 + \frac{L}{t_{poly} + t_{ox}}\right)W_{eff}2n \tag{10}$$

where L is the drawn gate length.

Since C_{int} occurs through the channel region, it can only exist in the absence of a charge layer. As a result, C_{int} varies with the width of the depletion region and can be calculated using [4]

$$C_{int} = \frac{2}{\pi}\epsilon_{si}\ln\left(1 + \frac{w_d}{t_{ox}}\sin\left(\frac{2\epsilon_{ox}}{\pi\epsilon_{si}}\right)\right)W_{eff}2n \tag{11}$$

The total overlap capacitance can now be calculated using

$$C_{ov} = C_{pp} + C_{ext} + C_{top} + C_{int} \tag{12}$$

This overlap capacitance is significant as it can contribute more strongly to the overall capacitance seen across the varactor terminals than the channel capacitance itself, especially when the device is in depletion mode.

C. Channel Resistance Model

Increasing the width of the depletion region also results in an increase in the channel resistance. By adapting the channel resistance equation given in [2], the following equation can be used to model this resistance

$$R_{ch} = \frac{\frac{L_{eff}}{2}}{qN_{well}\mu A_{ch}n} \tag{13}$$

where μ is the mobility of electrons in the channel and A_{ch} is the cross-sectional area of the channel, which is depends on the depth of the n^+ diffusion region, X_j, and is given by

$$A_{ch} = W_{eff}\,(X_j - w_d) \tag{14}$$

D. Substrate Model

To develop an accurate substrate model, we begin by calculating the capacitance C_{act} between the charge layer formed at the bottom of n^+ diffusion region and the n well to p substrate interface. The resulting equation for this calculation is therefore a function of the total area beneath all n^+ diffusion regions, A_{act}, as

$$C_{act} = \frac{\epsilon_{si}}{D_n - X_j} A_{act} \tag{15}$$

where D_n is the depth of the n well.

Secondly, the vertical resistance from the n^+ diffusion regions, through the n well, to the p substrate can be obtained. By taking the total area of the n well region as the cross-sectional area, A_{well}, to be used in the resistance equation, we obtain

$$R_{well} = \frac{D_n - X_j}{qN_{well}\mu_n A_{well}} \tag{16}$$

Next we determine the cross-sectional area of one side of the p^+ ground contact as

$$A_{sub} = X_p L_{con} \tag{17}$$

where X_p is the depth and L_{con} is the length of the p^+ ground contact implanted in the substrate. With this parameter, the resistance seen between the n well and ground contact, R_{sub}, which is dependent on the distance between these structures, D_{gnd}, and can be calculated as

$$R_{sub} = \frac{D_{gnd}}{qN_{sub}\mu_n A_{sub}} \tag{18}$$

where N_{sub} is the substrate carrier concentration.

The area of the side of the n well ($A_{well}^{side} = L_{well}D_n$) can then be used to calculate the substrate capacitance as

$$C_{sub} = \frac{\epsilon_{si}}{D_{gnd}} A_{well}^{side} \tag{19}$$

It should also be noted that if multiple ground connections are in place in the circuit layout then the resulting resistances and capacitances should be considered to be in parallel.

The varactor configuration discussed thus far relies on a bias voltage applied to the gate terminal, meaning that the RF signal enters the varactor's n well through the n^+ diffusion regions. This in turn means that whatever DC bias voltage, V_{DC}, is in place in the circuit at the varactor's drain/source connection point is also passed to the n well, effectively reverse biasing the $p{-}n$ junction at the well to substrate interface and allowing C_{well} to be calculated using [5]

$$C_{well} = \epsilon_{si} A_{well} \sqrt{\frac{q}{2\epsilon_{si}\,(\Phi_{Bi} + V_{DC})} \left(\frac{N_{sub}N_{well}}{N_{well} + N_{sub}}\right)} \tag{20}$$

where Φ_{Bi} is the built in electrostatic potential barrier, which is defined as the difference between the fermi levels of the p and n materials respectively [5].

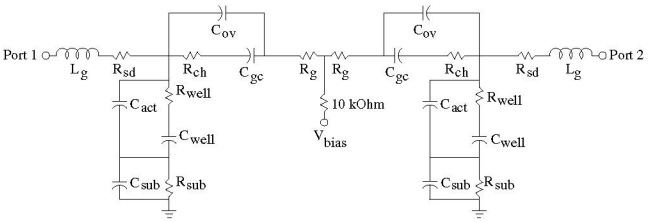

Fig. 3. Back-to-back varactor model including all parasitic components.

E. Additional Parasitics

The resistance inherent to the use of n^+ polysilicon as the gate material, R_g, has been well documented and can be calculated as

$$R_g = \frac{W_{eff}}{L}\frac{R_{sq}^g}{12n} \tag{21}$$

where R_{sq}^g is the resistance per square of the gate material and the factor of 12 is used to account for the fact that the gate fingers are connected at each end.

The resistance through the n^+ diffusion region relies on the length, L_{dif}, and sheet resistance, R_{sq}^d, of the n^+ diffusion region as

$$R_{sd} = \frac{\frac{L_{dif}}{2}}{2nW_{eff}} R_{sq}^d \tag{22}$$

The inductance of the via connection, L_g, is obtained by treating the via as an antenna and taking the integral over volume of the magnetic field. Using this approach we obtain

$$L_g = \frac{\mu_0 L_{via}}{6\pi r_{via}} \tag{23}$$

where r_{via} and L_{via} are the radius and length of the via respectively.

III. Measured Results

In order to isolate the varactor control voltage from the circuit connection points a differential structure is often used as illustrated in Figure 3. In this setup, which we will call "gate-biased", V_{bias} is applied to the varactor gates. An alternative configuration, which we will call "diffusion-biased", reverses each varactor so that V_{bias} is instead applied to the diffusion regions, which has the inherent effect of improving the Q factor.

To validate the presented model, simulations were run at 25 GHz and the results are compared to the W = 9 x 2.5 μm varactors fabricated in 0.18 μm CMOS in [6] in Figure 4 (a) and (b). Figure 4 (c) validates the model for other varactor sizes by comparing the simulation results to a fabricate W = 16 x 2.5 μm, diffusion-biased varactor.

IV. Differential Low-Noise Amplifier

A two-stage LNA designed for operation at 23 GHz is shown in Figure 5. This design uses neutralizing capacitors, C_N, to improve the reverse isolation of the amplifier by canceling the feedback path through the gate-drain capacitance, C_{gd}, of each transistor. This technique is difficult to implement since a small mismatch between C_N and C_{gd} can produce

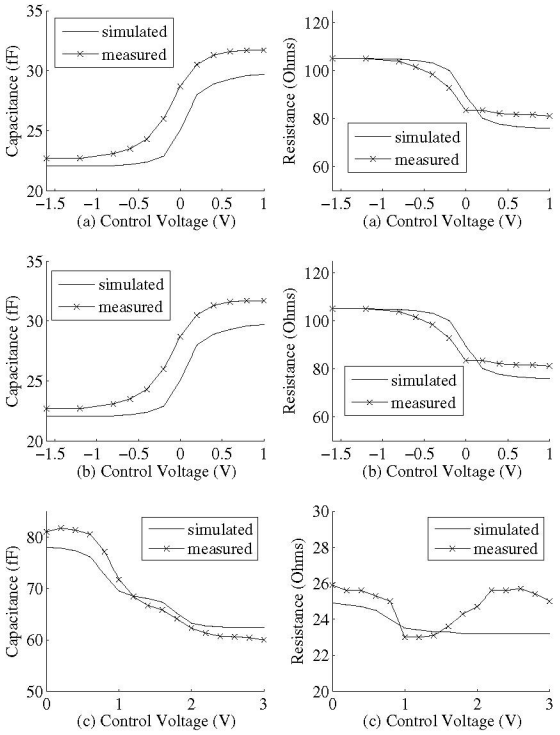

Fig. 4. Measured and simulated behaviour of (a) gate-biased 22.5 μm, (b) diffusion-biased 22.5 μm and (c) diffusion-biased 40 μm varactors.

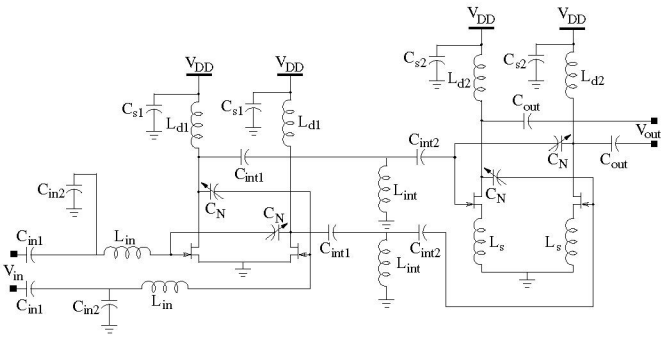

Fig. 5. Schematic of the differential LNA including matching and drain bias networks.

instability. To compensate for this 40 μm wide, diffusion-biased varactors were implemented for each C_N.

Thanks to the accuracy of the varactor model presented in this paper, along with their tunability, the risk of creating instability in the amplifier due to improperly chosen values of C_N was low. The measured noise and gain performance of the fabricated circuit is then shown in Figure 6, along with the simulated results that were obtained by using the presented varactor model. The good agreement between these curves provides further evidence of the validity of the varactor model. In addition, the excellent minimum noise figure of 4.5 dB at a frequency of 23.5 GHz is the best noise figure reported

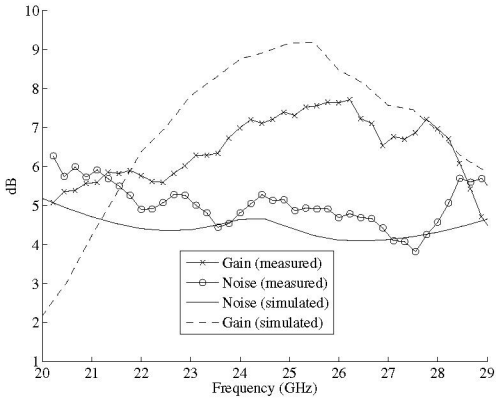

Fig. 6. Measured noise figure and gain.

for a differential amplifier in standard 0.18 μm CMOS at frequencies above 20 GHz to date.

V. Conclusion

A lumped element model has been presented for an AMOS varactor. This model relies on the technology parameters and layout dimensions, making it easily adaptable to any varactor size in any standard CMOS technology. It is also valid in any mode of operation, making its implementation in any circuit simulator straight forward. The presented model compares well to measured results for different size varactors using different bias configurations and its successful implementation in a 23 GHz differential LNA gives strong support to the validity of the model.

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References

[1] S. Song and H. Shin, "An RF Model of the Accumulation-Mode MOS Varactor Valid in Both Accumulation and Depletion Regions," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1997-1999, September 2003.

[2] J. Maget, R. Kraus and M. Tiebout, "A Physical Model of a CMOS Varactor with High Capacitance Tuning Range and its Application to Simulate a Voltage Controlled Oscillator," *International Semiconductor Device Research Symposium*, pp. 609-612, 2001.

[3] C.H. Wang, "Identification and Measurement of Scaling-Dependent Parasitic Capacitances of Small-Geometry MOSFET's," *IEEE Trans. Electron Devices*, vol. 43, no. 6, pp. 965-972, June 1996.

[4] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill, 1999.

[5] B. Streetman, *Solid State Electronic Devices*, Prentice Hall, 1995.

[6] J.P. Carr and B.M. Frank, "A 38 GHz Accumulation MOS Differentially Tuned VCO Design in 0.18 μm CMOS," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 170-173, 2006.