Hao Jun Liu

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EDUCATION

Bachelor of Applied Science and Engineering, University of Toronto 2006-

- Electrical Engineering, 4rd Year
- Relevant Courses:
  - Parallel Programming
  - Advanced Computer Architecture
  - Digital System Design
  - Compiler Optimization
- CGPA: **3.52/4.0** (Dean's List)
- Technical CGPA: **3.82/4.0**

TECHNICAL SKILLS

- FPGA CAD: Xilinx ISE/EDK
- Hardware Simulation: Modelsim
- Modeling: MATLAB
- Programming: C/C++, Perl, Python, Shell
- HDL: Verilog HDL, VHDL

ENGINEERING WORK EXPERIENCE

Summer Research Assistant, FPGA Accelerator, U of T 2010.05-08

FPGA Partial Reconfiguration

- Designed digital system based on partial reconfiguration
- Test the functionality of the design
- Collect running time and reconfiguration time
- Analysis of the running time and reconfiguration time
- Paper to be published

Part Time Research Assistant, FPGA Accelerator, U of T 2009.09-

Molecule Dynamic Simulation with MPI on FPGA 2010.04

- Designed digital system based on MPI
- Test the functionality of the design
- Collect statistics about running time
- Analysis of the running time

Software Engineering, Compiler Developer, IBM Canada 2009.05-

Compiler Build Specialist 2010.04

- Monitor build status and open defect if there is to ensure the software development process is running smoothly
- Develop and test tools for build to make the build better using Shell scripting and Perl
- Test Products to be shipped to ensure the software can run on customers' platform

Summer Research Assistant, NAND Flash chip controller design, U of T 2008.05-08

The NAND Flash chip controller can read/write/erase NAND flash chips. A PC can control it via PCI Express Interface.

- Designed and implemented the controller using Quartus II and DE2 board (An FPGA developing board) from Altera
- Designed and implemented an interface between the controller and PCI Express using Quartus II and Stratix II GX PCI Express

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Development Board from Altera
- Used Verilog HDL to improve design maintainability
- Designed a PCB that connects to development board and NAND flash chips.
- Tested and debugged the system using module simulation and digital logic to ensure functionality of the controller
- Implemented customized assembly and compiler that convert assembly code to Verilog HDL to improve testing efficiency
- Wrote project summary for to properly document the project

AWARDS
- 2010 NSERC Research Award ($5625)
- 2009 IEEE Canada Foundation Scholarship($3500)
- 2009 NSERC Research Award ($5625, Offered but Declined)
- 2009 Winter term, Honors Dean's List (Top 10%, GPA 3.78/4.00)
- 2008 Fall term, Honors Dean's List (Overload, Top 10%, GPA 3.94/4.00)
- 2008 Faculty Research Award ($3000)
- 2008 Winter term, Honors Dean's List (Top 5%, GPA 4.00/4.00)
- 2007 Fall term, Honors Dean's List (Top 10%, GPA3.74/4.00)
- 2006 Fall term, Honors Dean's List (Top 10%, GPA3.54/4.00)
- 2006 Structure, Material and Design - Bridge Design Runoff 5th place

PROFESSIONAL MEMBERSHIPS
- Institute of Electrical and Electronics Engineers (IEEE), Member 2006-
  Read Magazines published by IEEE and its' societies to update knowledge from the most recent development of technology

- IEEE U of T Student Branch
  -Chair 2010-
  - Lead the branch to organize events
  - Oversee the running of the branch

  - Chair Advisor 2009-2010
  - Provide Guidance to fellows to ensure the branch is in normal running process

  - Vice Chair for Professional Development 2008-2009
  - Invite professors and professionals to discuss about their research opportunity of advance in industry and industry knowledge
  - Prepare and schedule study group to increase students interaction while increase students' understanding of specific subject area

  - Professional Development Officer 2007-2008
  - Assist Vice Chair for Professional Development for inviting speakers and prepare study group material