Quantum Efficiency Modeling of Amorphous/Crystalline Silicon Heterojunction Photovoltaic Devices

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ABSTRACT

Amorphous/crystalline silicon (a-Si/c-Si) heterojunctions are of particular importance in photovoltaic (PV) energy conversion in a cost-effective way. This is principally due to the low temperature (low-T) nature of the process. In this work, we have analyzed a (n)a-Si/(i)a-Si/(p)c-Si heterojunction solar cell structure using theoretical models for internal quantum yield (IQY) and I-V behavior. We considered low-quality (low bulk lifetime), cheaper substrates. Thin, low bulk lifetime substrates in combination with a low-T bulk passivation scheme and low rear surface recombination can lead to a cost effective device fabrication process with competitive conversion efficiency.

INTRODUCTION

a-Si/c-Si heterojunction technology is very attractive for cost-effective PV device fabrication. Since this is essentially a low-T process (<250°C), there is a possibility to use certain moderate quality Si substrates (e.g. ribbons) whose bulk lifetime degrades after high-T thermal excursions. Further, the low-T nature of the process allows bulk defect passivation techniques such as plasma hydrogenation be implemented prior to device fabrication. In a a-Si/c-Si device, the quality of the heterointerface is very crucial. By introducing an intrinsic a-Si layer at the interface, the defect density can be reduced. This way, very high efficiency (HIT) solar cells have been fabricated using single crystalline Si [1]. Comprehensive theoretical models have also been developed on the charge carrier transport of this heterojunction structure [2,3]. In this work, we have analyzed a (n)a-Si/(i)a-Si/(p)c-Si solar cell structure using these models for internal quantum efficiency with special emphasis on low bulk quality Si substrates. IQY has been calculated for different regions of the device. Thinner, low bulk-lifetime substrates in combination with a low-T bulk passivation scheme and reduced rear effective surface recombination can lead to a cost effective fabrication process with reasonably high efficiencies.

CARRIER TRANSPORT

Figure 1(a) shows a schematic cross section of the cell structure. (i)a-Si, (n)a-Si, and a transparent conductive oxide (TCO) are deposited on a (p)c-Si substrate. Regions 2 and 4 represent the depletion regions. The rear side of the cell is shown completely covered with metal. However, to reduce the rear surface recombination, one can implement additional design features such as a rear p-i-p” heterojunction, or a passivation film with contact vias. In the present case, we represent the rear surface recombination by a surface recombination velocity, $S_n$. The bulk quality of the (p)c-Si substrate is represented by the electron diffusion length, $L_n$.

The approach follows the general procedure described in [3]. Figure 1(b) shows the energy band diagram. The band offset $\Delta E_C$ affects both the dark current as well as the photocurrent. For small forward voltages ($V_F$), the electrons photo-generated in region 5 will
diffuse towards region 4. Once they reach the 4/5 interface, they will be swept toward the heterojunction interface 4/3. The electrons generated in region 4 will also be swept toward interface 4/3. Since the electrons gain an energy $qV_p$ upon traversing region 4, they now have to overcome an energy barrier of $(\Delta E_C - qV_p)$. Since $V_p$ is large for small $V_F$, $\Delta E_C$ will have no lowering effect on current. (dark current is either absent or cannot compensate the photocurrent). For large $V_F$ there will be high enough dark current which compensates the photocurrent. The forward electrons will have to pass through the i-layer (region 3) which limits the carrier velocity.

**Figure 1.** (a) Schematic cell structure, (b) Energy band diagram for (n)a-Si/(i)a-Si/(p)c-Si cell

The effective velocity of electrons in the i-layer is given by [3],

\[
v_{\text{eff}} = \frac{-\mu_n E_i}{1 - \exp(V_i/V_t)}
\]

(1)

where, $\mu_n$, $V_i$, and $E_i$ are electron mobility, potential drop, and electric field in the (i)a-Si film. By considering the thermionic emission theory across heterojunctions [4], we can represent the electron flux $F_{34}$ at the “region-3 side” of interface 3/4 as,

\[
F_{34} = v_{\text{eff}} n_{23} \exp\left(-\frac{V_i}{V_t}\right) - v_{\text{eff}} n_{34}, \quad \text{and} \quad n_{34} = n_{23} \exp\left(-\frac{V_i}{V_t}\right) - \frac{F_{34}}{v_{\text{eff}}}
\]

(2)

Further, while passing over $\Delta E_C$, the velocity of the electrons will be limited by the effective Richardson velocity, $v_R$ [5]. So we write,

\[
F_{34} = v_R n_{34} - v_R n_{43} \exp\left(-\frac{\Delta E_C}{kT}\right), \quad \text{and} \quad n_{43} = n_{34} \exp\left(\frac{\Delta E_C}{kT}\right) - \left(\frac{F_{34}}{v_R}\right) \exp\left(\frac{\Delta E_C}{kT}\right)
\]

(3)
From (2) and (3),

\[ n_{43} = n_{23} \exp\left(\frac{\Delta E_C - qV_i}{kT}\right) \left(\frac{F_{34}}{v_R} + \frac{F_{34}}{v_{eff}}\right) \exp\left(\frac{\Delta E_C}{kT}\right) \]  

(4)

The electron current at the interface 4/5 is given by, \( J_{n45} = q\left(L_n / \tau_n\right)n_{43} \exp\left(-V_p / V_T\right) \), where \( L_n \) and \( \tau_n \) are the diffusion length and lifetime respectively. Combining with (4), we can write,

\[ J_{n45} = q\left(\frac{L_n}{\tau_n}\right)n_{43} \exp\left(\frac{\Delta E_C - qV_i - qV_p}{kT}\right) - qF_{34} \left\{ \frac{L_n}{\tau_n v_R} + \frac{L_n}{\tau_n v_{eff}} \right\} \exp\left(\frac{\Delta E_C - qV_p}{kT}\right) \]  

(5)

Therefore, the lowering factor (LF) for the electron forward current (dark and photo) \( J_{n45} \) will be:

\[ 1 + \left(\frac{L_n}{\tau_n v_R} + \frac{L_n}{\tau_n v_{eff}}\right) \exp\left(\frac{\Delta E_C - qV_p}{kT}\right) = 1 + LF_n \]  

(6)

Now, without considering the lowering factor, we can write \( J_{n45} \) as,

\[ J_{n45} = q\left(\frac{L_n}{\tau_n}\right)n_{43} \exp\left(\frac{\Delta E_C - qV_i}{kT}\right) \]  

(7)

The current coming from the intrinsic layer can be written as,

\[ J_{n34} = qv_{eff} n_{23} \exp\left(-\frac{qV_i}{kT}\right) \]  

(8)

Combining (7) and (8), we get,

\[ J_{n45} = J_{n34} \frac{L_n}{\tau_n v_{eff}} \exp\left(\frac{\Delta E_C - qV_p}{kT}\right) = J_{n34} \times (LF_3) \]  

(9)

This means that the electron current in the intrinsic layer should be multiplied by the factor LF3, while considering the final electron current entering the p bulk region. The same procedure can be applied to electron current collected in region 2. The total electron (dark + photo) current can be written as,

\[ J_n = \left(\frac{qL_n n_{po}}{\tau_n (1 + LF_n)}\right)v_T \left(\frac{v_T}{v_R} - 1\right) + J_{n5} + J_{n4} + (J_{n34} \times LF_3) + (J_{n2} \times LF_2) \]  

(10)

where,

\[ LF_2 = \frac{L_n}{\tau_n v_{eff}} \exp\left(\frac{\Delta E_C - qV_i - qV_p}{kT}\right) \]  

(11)
Similarly, one can write expressions for the hole current ($J_p$), entering the n bulk region. For the hole current under forward bias, there is only one limiting region (i-layer) since there is no barrier in valence energy band in the heterointerface. The complete I-V relationship can therefore be developed for the cell. Figure 2 illustrates the influence of the lowering factors on the I-V behavior. Actually $L_{F_\text{n}}$ includes $\Delta E_C$ and the field effect in the i-layer [2]. For low $V_F$, $V_P$ is high and hence $L_{F_\text{n}}$ will be $<<1$. For high $V_F$, $V_P$ decreases, and hence the suppression effect shows up (Figure 2).

**Internal Quantum Yield (IQY)**

The major contributor to the photocurrent is the base c-Si substrate. As far as the (p)c-Si contribution to IQY is concerned (short circuit conditions), it will be the same as that of a pn homojunction cell [5]. We calculated the total IQY of the device by considering the contribution of each region, i.e., the (p)c-Si, (i)a-Si, and depletion regions. For this, the continuity and drift diffusion current equations were solved for excess carriers by considering the generation/recombination and boundary conditions in each region. The absorption coefficient data from literature were used for a-Si, and c-Si. Figure 3 shows the contribution of the (i)a-Si layer to IQY. When the layer is thin (as in practical cells), the contribution to photocurrent is also low. The IQY of the c-Si base is shown in figure 4 for different levels of bulk quality. Heterojunction process can use temperature-degradable, defective Si, whose $L_n$ is low. The low-T nature of the process allows bulk passivation techniques such as hydrogenation, prior to cell fabrication, to increase $L_n$. Figure 4 shows that even small improvement in bulk quality can lead to significant gains in IQY.

**Figure 2.** I-V curve of the cell showing the effect of lowering factor at high $V_F$.

**Figure 3.** Internal quantum yield of the (i)a-Si layer for various layer thicknesses.

**Figure 4.** Internal quantum yield of the (p)c-Si base region for various electron diffusion lengths.
Another parameter that influences the base IQY is the rear surface recombination ($S_n$), which can be reduced by an appropriate surface passivation scheme. However, the rear surface passivation can be beneficial only if $L_n$ is comparable to the wafer thickness. This is illustrated in figures 5 and 6. Figure 5 shows that for thicker wafers with moderate $L_n$ (i.e., $L_n <$ wafer thickness), the passivation has only a negligible effect on IQY. However, if the wafer is thinned down to values comparable to $L_n$, (i.e. a $120 \mu m$ $L_n$ with a $100 \mu m$ thick wafer) then surface passivation can be very beneficial (Figure 6). Since low-T surface passivation options are available (pip$^+$ heterojunction, or PECVD nitride) in the heterojunction process, it would be advantageous to use thinner wafers if the bulk $L_n$ is not very high. Figure 7 shows the total IQY (i.e., including all regions of the cell) of the cell. Understandably, increased (i)a-Si thickness results in the reduction of IQY in the short wavelength region. (with increased $i$-layer thickness, more photons which would otherwise have been absorbed in the c-Si region, will be absorbed in the (i)a-Si). For practical cells however, the i-layer is usually very thin, so its contribution to IQY is small.
I-V Characteristics

The complete illuminated I-V characteristics can be obtained by combining the dark I-V and the photocurrent. As shown in figure 2, the current suppression via lowering factor (LF) is stronger at high $V_F$. In equation (1), $v_{\text{eff}}$ depends both on $V_F$ and on i-layer width. Either increasing $V_F$ (i.e., decrease $V_i$), or increasing the i-layer width will cause a stronger suppression [3]. Overall, the suppression of dark and photocurrent (contributing from p-bulk) is stronger at higher $V_F$ and thicker i-layers. The photogenerated short-circuit current can be obtained by integrating IQE curves with the standard (AM 1.5) solar radiation spectrum. Figure 8 shows the Illuminated I-V characteristics calculated for standard solar radiation. Table I shows how the short circuit current ($J_{SC}$) and the open circuit voltage ($V_{OC}$) vary with intrinsic layer thickness. What we observe is that for small range of intrinsic layer widths (<100nm), the $V_{OC}$ remains unchanged whereas there is a sharp drop in $J_{SC}$.

Table I. Variation of $J_{SC}$ and $V_{OC}$ with intrinsic layer thickness

<table>
<thead>
<tr>
<th>i-layer (nm)</th>
<th>5</th>
<th>10</th>
<th>30</th>
<th>50</th>
<th>75</th>
<th>100</th>
<th>250</th>
<th>500</th>
<th>750</th>
<th>1000</th>
</tr>
</thead>
<tbody>
<tr>
<td>$J_{SC}$ (mA/cm²)</td>
<td>30.8</td>
<td>30.7</td>
<td>30.2</td>
<td>29.8</td>
<td>29.4</td>
<td>29.0</td>
<td>27.8</td>
<td>26.9</td>
<td>26.5</td>
<td>26.3</td>
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<td>$V_{OC}$ (mV)</td>
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<td>592</td>
<td>592</td>
<td>592</td>
<td>592</td>
<td>594</td>
<td>600</td>
<td>610</td>
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CONCLUSIONS

(n)a-Si/(i)a-Si/(p)c-Si heterojunction solar cell structure has been studied using theoretical models for internal quantum efficiency and I-V behavior for low quality silicon substrates. For the quantum yield analysis, different regions of the device have been treated separately and the total quantum yield obtained. Internal quantum yield and I-V curves were used to look at the performance of the heterojunction cell for various device parameters, with the focus on silicon materials with moderate bulk quality. Thinner substrates in combination with a low temperature bulk passivation scheme and reduced rear effective surface recombination velocity can lead to a cost effective device fabrication process, enabling the use of low bulk-quality silicon. While an (i)a-Si film is necessary to passivate the a-Si/c-Si interface, it has to be as thin as possible.

REFERENCES