Luke Wang

Electrical Engineering
University of Toronto

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EDUCATION

Bachelor of Applied Science (BASc), Honours Electrical Engineering
University of Waterloo, Waterloo, ON September 2006 – April 2011

Master of Applied Science (MASc), Electrical Engineering
University of Toronto, Toronto, ON September 2011 – June 2014
Supervisor: Professor Anthony Chan Carusone
Thesis: Timing skew calibration in time-interleaved (TI) analog to digital converters (ADC)

- 10GS/s 8-bit 8-way time-interleaved SAR ADC in TSMC 65nm CMOS process
- Clock distribution and top level integration with output decimation
- Novel timing skew correction algorithm development and verification in MATLAB

Doctor of Philosophy (PhD), Electrical Engineering
University of Toronto, Toronto, ON January 2014 – Present
Supervisor: Professor Anthony Chan Carusone
Research Topic: Reconfigurable and optimal ADC for wireline communications

- Design, layout and testing of reconfigurable 6-bit 32GS/s folding flash ADC in TSMC 16nm FinFET CMOS (published in ISSCC 2018)
- Implementation of ADC-based receiver impairment model & equalizer in software
- Greedy search strategy for ADC link power scaling using information metric (BER), currently in patent application process

SUMMARY OF QUALIFICATIONS

- Experience in design/verification/layout in TSMC 16nm FinFET CMOS process
- Industrial experience in layout of high speed analog blocks in TSMC 7nm FinFET CMOS process
- Industrial experience with circuit analysis/simulation/layout in TSMC 28nm process
- Experience in high speed ADC design, testing and knowledge of key calibration algorithms and their implementation
- Experience in ADC and wireline link modelling, with system knowledge of typical SERDES receiver
- Experience in implementing digital signal processing systems on FPGA
- Experience in designing and modeling algorithms in MATLAB/Simulink
- Familiar with EM simulation using ADS Momentum and Sonnet

WORK EXPERIENCE

IC Design Engineer Intern November 2016 – November 2017
Huawei Canada, Toronto, ON

- Investigated ADC-based receiver structures for PAM-4 short-reach to median-reach electrical links in TSMC 16nm FinFET CMOS process
- Experienced in high speed analog layout in TSMC 7nm FinFET CMOS process with dual-patterning: blocks include 8GHz high speed latch for mixed-signal receiver and input stage of trans-impedance amplifier (TIA) for 64Gb/s receiver analog front-end

Analog/Mixed Signal IC Design Intern July 2013 – October 2013
Broadcom, Irvine, CA, USA

- 28nm SERDES verification including return loss, top level functional and mixed signal AMS with digital CDR
- Schematic design, layout, and verification of subblocks including clock drivers, duty cycle corrector, and resistor ladder for signal detector
- Verification included VAVO IR analysis and EMRC analysis using Cadence 6

Nanotechnology Research Engineering September 2010 – December 2010
ICSPI, Waterloo, ON

- Participated in characterization of MEMS actuators and sensors
- Designed hardware and Labview software for driving and sensing MEMS devices

Vision Neuroscience Lab Research Intern
Hospital for Sick Children, Toronto, ON January 2010 – April 2010

- Designed and configured experimental setup for research studies
- Developed MATLAB tools for data processing and analysis of eye and finger trajectories
- Implemented algorithms such as Dynamic Time Warp for defining position variability

Emerging Radio Systems Group Undergraduate Research Assistant
University of Waterloo, Waterloo, ON September 2009 – December 2009
Supervisor: Dr. Slim Boumaiza

- Exposed to a Radio Frequency (RF) pre-distorter system for a power amplifier
- Tested RF frontend including analog-to-digital converters and modulators

Signal Processing Module Developer
Defence Research and Development Canada, Ottawa, ON May 2009 – August 2009

- Researched FPGA based algorithms used to minimize interference on GPS signals
- Developed software models of signal processing algorithms in MATLAB
- Designed and verified digital circuits for FPGA using Simulink and Altera DSP Builder
- Programmed microprocessor on FPGA for data transfer and system configuration
- Investigated system performance to improve time and accuracy critical component

Electricity Market Analyst
Independent Electricity System Operator, Mississauga, ON September 2008 – December 2008

- Designed and developed automated surveillance tools that detect anomalies and inefficiencies in the electricity market
- Converted existing tools to the new and more stable Microsoft .NET platform
- Improved functionality of tools through system integration using Excel, Access, Hyperion, and MATLAB

Electrical Controls Engineering
Siemens Power Generation Canada, Hamilton, ON January 2008 – April 2008

- Configured Programmable Logic Controllers (PLC) for hardware testing
- Designed and developed Human Machine Interfaces for turbine control
- Provided excellent onsite support for transition shop control software and system networking with minimal supervision and assistance

Teaching Assistant
University of Toronto, ON

- Tutorial tutor for **ECE110**: Electrical Fundamentals (2012)
- Head tutorial tutor for **ECE159**: Engineering Science equivalent of ECE110 (2015,2016)
- Lab & tutorial tutor for **ECE212**: Circuit Analysis Fundamentals (2015, 2016, 2017, 2018)
- Lab tutor for **ECE331**: Analog Electronics (Diodes, basic MOSFET/BJT)
- Tutorial tutor for **ECE360**: Engineering Science equivalent of ECE331 (2017)
- Tutorial tutor for **ECE354**: Analog Electronics II (frequency response, differential amplifier, feedback) (2018)
- **SKULE** (University of Toronto Engineering Society) tutor: tutored more than 20 students on circuit courses

AWARDS

- Edward Rogers Sr. Graduate Scholarship (2017)
- NSERC Postgraduate Scholarship-Doctoral Program (PGS-D) (2015-2017)*
- Ontario Graduate Scholarship (2014-2015)
- Queen Elizabeth II Graduate Scholarship in Science and Technology (2012-2013)
- NSERC Alexander Graham Bell Canada Graduate Scholarship M (2011-2012)*
- University of Waterloo President's Research Award (2009)
- University of Waterloo President's Scholarship (2006)
- University of Waterloo Nortel Networks Award (2006)
- University of Waterloo Dean's Honours List (2006-2010)
- Queen Elizabeth II Aiming for the Top Scholarship (2006-2010)
- Esse Quam Videri Award (Academics and Contribution to School Life 2006)
- Bill Hodsell Electronics Award (Rotary Club for excellence in Computer Tech. 2005)

*National level scholarships provided by The Natural Sciences and Engineering Research Council of Canada (NSERC)

PUBLICATIONS

- L. Wang, Y. Fu, M. LaCroix, E. Chong, A. Chan Carusone, "A 64Gb/s PAM-4 Transceiver Utilizing an Adaptive Threshold ADC in 16nm FinFET," *International Solid State Circuits Conference (ISSCC)*, Feb. 11-15, 2018.
- L. Wang, M. LaCroix, A. Chan Carusone, "A 4GS/s Single Channel Reconfigurable Folding Flash ADC for Wireline Applications in 16nm FinFET," *IEEE Transactions on Circuits and Systems II*, Dec. 2017.
- L. Wang, M. LaCroix, A. Chan Carusone, "A 4GS/s Reconfigurable Folding Flash ADC for Time Interleaving in 16nm FinFET," *International Symposium on Circuits and Systems* (*ISCAS) Late Breaking News*, Baltimore, MD, USA, May 28-31, 2017.
- S. Chen, L. Wang, H. Zhang, R. Murugesu, D. Dunwell, A. Chan Carusone, "All-Digital Calibration of Timing Mismatch Error in Time-Interleaved Analog-to-Digital Converters," *IEEE Transactions on VLSI Systems*, 2017.
- L. Wang, Q. Wang, A. Chan Carusone, "Time Interleaved C-2C SAR ADC with Background Timing Skew Calibration in 65nm CMOS", *European Solid State Circuits Conference (ESSCIRC)*, Sept. 22-26, 2014.
- L. Wang and A.Yasotharan, "FPGA-based QR decomposition signal processor for GPS anti-jamming array antenna", Tech. Memo TM 2009-025, DRDC Ottawa, Nov. 2009.