Harmonic and Loss Analysis of Space-Vector Modulated Converters

A. Mehrizi-Sani, S. Filizadeh, and P. L. Wilson

***Abstract*—Space Vector Modulation (SVM) is an alternative method to the conventional, sinusoidal PWM for control of high-power converters. It is known for its higher utilization of the dc-bus voltage as well as being readily available for digital implementation. This paper presents the SVM method and a number of its variations, which are implemented in a digital transient simulation program (PSCAD/EMTDC). The developed model is used to study the performance of SVM in terms of its harmonic spectrum and associated losses. These factors are compared against different SVM implementations as well as the sinusoidal PWM strategy. The suitability of the model is hence ascertained.**

***Keywords*—Harmonic analysis, space-vector modulation, switching losses, transient simulation, voltage-sourced converter.**

I. Introduction

THE ABILITY of high-power electronic apparatus in controlling the flow of real and reactive power through designated electrical paths, improvement of dynamic and transient performance of the system, and support of voltage profile has led to their widespread use in modern power networks. Among the most employed high-power electronic apparatus are voltage-sourced converters (VSCs), which are able to operate as controlled voltage-sources that convert an essentially constant dc-voltage to an ac voltage of controllable magnitude, frequency, and phase.

Pulse-width modulation (PWM) schemes are used to synthesize the output voltage of a VSC [1]. In PWM methods switching instants are chosen so that the desired fundamental component is obtained while acceptable harmonic performance is achieved. The output waveform of a VSC consists of a series of voltage pulses. In a two-level VSC, which is studied in this paper, the voltage levels are $+V_{dc}/2$ and $-V_{dc}/2$, where V_{dc} is the dc-link voltage. In this case, the output voltage of each leg (of three legs) of the converter is determined through comparison of a modulating, high-frequency saw-tooth waveform and the desired sinusoidal voltage. This is done independently for each leg.

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An alternative method to PWM, space-vector modulation (SVM), places the converter in a number of states (that correspond to the so-called space-vectors), which are determined by the ON/OFF state of its controlled switches [2]. Synthesis of the output voltage along with crafting the desired harmonic performance is done by carefully selecting the appropriate states and their time-shares so that the desired voltage is best approximated.

The SVM method features a higher level of dc-bus voltage utilization compared to the conventional PWM. It also offers flexibility in its digital implementation by providing several optimization parameters [3], such as enabling different approaches to place space-vectors [4], [5] and the number and arrangement of samples in each cycle [6], [7]. SVM has found numerous applications in both power systems and industrial motor drives.

This paper presents an implementation of the SVM method in the PSCAD/EMTDC electromagnetic transients simulation program [8]. The developed model covers the entire range of operation from linear mode to overmodulation. It generates firing pulses to control the six switches of a two-level VSC for different space-vector placement strategies. The model is used to assess the harmonic behavior of the synthesized output voltage by studying the impact of such factors as space-vector assignment strategy and reference vector sampling rate.

Two factors contribute to the converter-related losses: switching losses, which become especially important at high switching frequencies and harmonic losses, which result in excessive heating in the load. These two loss categories are presented and the performance of SVM methods in comparison with the conventional PWM is investigated.

II. Overview of SVM Methods

Space-vector modulation is well-known for its convenient digital implementation. As mentioned earlier, in SVM the converter (Fig. 1) is controlled through the concept of converter states. Each converter state corresponds to a certain combination of switches. There are two switches in each leg of a two-level converter. As the switches in one leg cannot be both ON or OFF at the same time (the former leads to a short circuit of the associated phase, and the latter results in an open circuit), and there are three converter legs in a three-phase system, the total number of converter states is 8 (Table I). States are numbered in binary format (0 for OFF state of the upper switch and 1 for its ON state) from 000 to 111.

Each of the eight states of the converter is mapped into a voltage space-vector in the complex plane using the *dq0*

transformation, forming the vertices of a hexagon (Fig. 2) [9]. Two of eight states correspond to combinations in which all legs are in the same state (000 and 111). These two states generate a line voltage of zero and hence are called zero space-vectors. The remaining six states divide the complex plane of space-vectors into six regions. Each region is bounded by two adjacent non-zero (or active) vectors.

In SVM, a reference voltage-vector (Fig. 2), which rotates in the *dq*-plane at the frequency of desired output voltage, is used. The magnitude of the constructed three-phase voltage is proportional to the magnitude of this reference vector and the phase angle of the reference vector is equal to that of the phase-*a* of the output voltage. The reference vector is sampled evenly within the desired fundamental period (which is reciprocal of frequency of the output waveform).

As SVM aims to approximate the reference voltage as a series of voltage pulses, a sequence of converter states is applied. This is in contrast to the conventional sinusoidal PWM in which duty cycles for each phase are determined independently.

The time-share of each space-vector is determined by the following equations.

$$T_1 = \frac{\sqrt{3}}{2} T_s \, m \, \sin(\pi/3 - \theta) \tag{1}$$

$$T_2 = \frac{\sqrt{3}}{2} T_s \, m \, \sin(\theta) \tag{2}$$

$$T_0 + T_7 = T_s - T_1 - T_2 \tag{3}$$

where T_0, T_1, T_2, and T_7 are time shares of respective voltage vectors, T_s is the sampling period, θ is the phase angle at which the reference vector is sampled (Fig. 2), and m is the modulation index. Modulation index shows the relative magnitude of the output waveform to the dc-bus voltage and is defined as

$$m = \frac{V_{ref}}{V_{dc}/2} \tag{4}$$

where V_{ref} is the amplitude of desired output fundamental-component and V_{dc} is the available dc-bus voltage. The value of m determines whether the converter is in linear or nonlinear region. As mentioned, only the behavior of the converter in linear region is considered, which corresponds to values of m less than $2/\sqrt{3} = 1.15$. The maximum possible m is 4/3 = 1.33, which happens for square-wave operation that each switch stays ON for the entire positive half-cycle and remains OFF for the entire negative half-cycle.

Voltage vectors are applied accordingly so that their average over the sampling period is equal to the sampled reference voltage (Fig. 3) as shown in the following equation.

$$\mathbf{V}_{\text{ref}} = \frac{\mathbf{V}_0 \times T_0 + \mathbf{V}_n \times T_1 + \mathbf{V}_{n+1} \times T_2 + \mathbf{V}_7 \times T_7}{T_s} \tag{5}$$

where n is the sector in which $\mathbf{V}_{\text{ref}}$ is sampled, and T_0, T_1, T_2, and T_7 are as defined earlier.

TABLE I
SPACE-VECTORS AND THE CORRESPONDING PHASE VOLTAGES

State	c, b, a	V	Phase Voltages		
			V_{an}	V_{bn}	V_{cn}
0	000	**0**	0	0	0
1	001	$2V_{dc}/3\ e^{j0}$	$2V_{dc}/3$	$-V_{dc}/3$	$-V_{dc}/3$
2	011	$2V_{dc}/3\ e^{j\pi/3}$	$V_{dc}/3$	$V_{dc}/3$	$-2V_{dc}/3$
3	010	$2V_{dc}/3\ e^{j2\pi/3}$	$-V_{dc}/3$	$2V_{dc}/3$	$-V_{dc}/3$
4	110	$2V_{dc}/3\ e^{j\pi}$	$-2V_{dc}/3$	$V_{dc}/3$	$V_{dc}/3$
5	100	$2V_{dc}/3\ e^{j4\pi/3}$	$-V_{dc}/3$	$-V_{dc}/3$	$2V_{dc}/3$
6	101	$2V_{dc}/3\ e^{j5\pi/3}$	$V_{dc}/3$	$-2V_{dc}/3$	$V_{dc}/3$
7	111	**0**	0	0	0

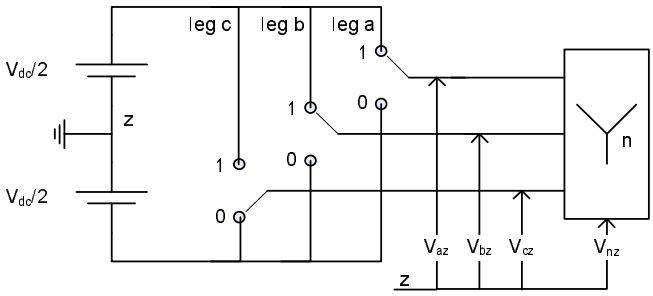

Fig. 1. Two-level three-phase voltage-sourced converter in the 011 state.

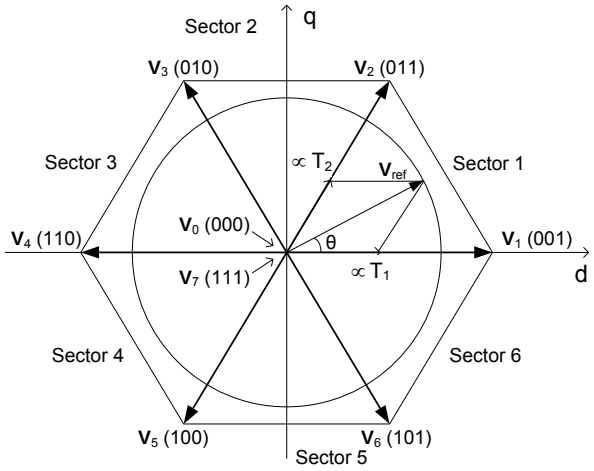

Fig. 2. Arrangement of active and zero vectors in a hexagon based on leg states.

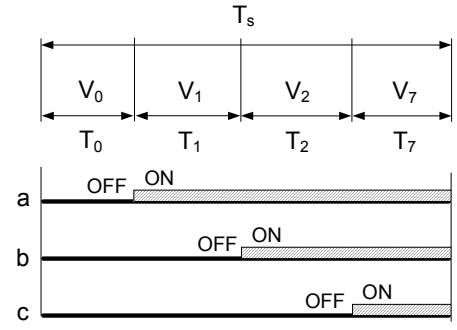

Fig. 3. Averaging of space vectors over time and the corresponding switch states.

There are several methods suggested in the literature for arrangement of states in a sampling period [5]-[7]. These methods are different in the number of states used, their order, and shares of zero-vectors, which further lead to different number of switching actions, switching losses, and harmonic behavior of the converter. Although according to (1)-(3), two active space-vectors and the zero space-vector must be applied, their sequence is left unspecified. Some possible switching sequences are shown in Fig. 4.

Referring to converter states by their numbers, the conventional SVM uses successions of **0127** and **7210** in the first sector, to take advantage of the inherent symmetry in this method. Another suggested strategy for the first sector is **012** followed by **721**. By eliminating one zero-vector in each cycle, this method ensures minimum number of switchings by alternating between states that are different only in one leg state [10], [11]. This family of methods is called discontinuous (or bus-clamped), in contrast to the conventional SVM, which is identified as a continuous method [9]. In discontinuous strategies, each phase is clamped to the top or bottom dc rail for one-third (120°), one-sixth (60°), or one-twelfth (30°) of the fundamental cycle, which eliminates the switching of that phase during the corresponding period.

Aside from freedom in arranging the converter states within one sampling period, which is absent in the conventional waveform-comparing PWM methods, SVM is superior to conventional PWM in that it is innately designed for digital implementation. This makes it readily available for microcomputer-based implementation as well as simulation with digital simulators. In the next section, implementation of SVM in one such simulator is presented.

III. Digital Implementation

In this section, a digital implementation of space-vector modulation is presented. Generation of high-order voltage and current harmonics as a result of rapid switchings of a converter necessitate the use of a transient simulation tool. As a platform able to handle extensive network studies in power systems, digital implementation and testing of SVM is carried out using the electromagnetic transients simulation program PSCAD/EMTDC [8].

The model is able to generate firing pulses for different strategies. It is also able to work in the overmodulation region (a mode with a modulation index of larger than 1.15 in which the converter produces an output voltage with an amplitude higher than what is available in conventional methods, at the expense of downgrading the harmonic spectrum [12]), however, this paper does not consider behavior of the model in this region. The model and its output signals are shown in Fig. 5. Fig. 6 shows typical traces of the line voltage and currents.

The PSCAD component for SVM is used in conjunction with a Multiple Run component that allows parametric studies. The results are presented in the next section.

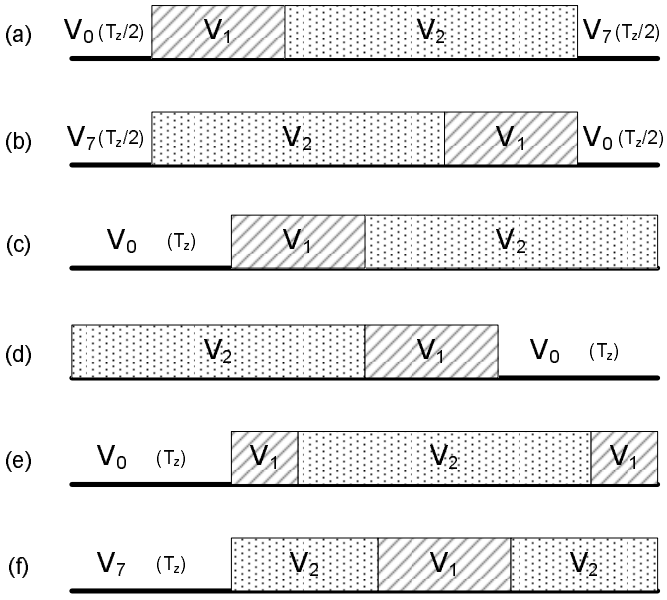

Fig. 4. Some of the possible switching sequences shown for the first sector. (a), (b): conventional SVM, (c), (d): 120° bus-clamped SVM, and (e), (f): 60° bus-clamped SVM. (T_z is $T_s - T_0 - T_1$.)

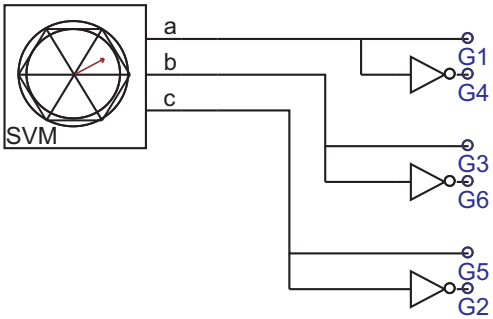

Fig. 5. The SVM model developed in the PSCAD/EMTDC program.

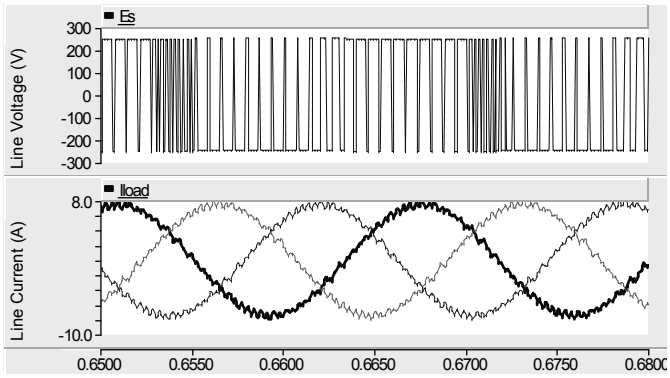

Fig. 6. Line voltage and currents of the space-vector modulator (for conventional SVM).

IV. Harmonic Performance

In conventional power systems, harmonics arise because of nonlinear system elements. In power electronic circuits such as converters, however, nonlinearity is the direct product of turn-ON and turn-OFF action of switches that results in distortion of the waveforms. While harmonics in a power

system consume the current capacity of transmission lines, they do not transmit useful power, hence leading to over-heating and overloading of equipment. In order to reduce these effects, study of harmonics of the proposed method is of primary importance.

Total Harmonic Distortion THD, reflects energy of the waveform harmonic content and is defined as

$$\mathrm{THD} = \frac{\sqrt{\sum_{h=2}^{n} V_h^2}}{V_1} \qquad (6)$$

where V_1 is the rms value of the fundamental-component voltage and V_h is rms value of the hth harmonic. As suggested in the IEEE Standard 519 [13], the first 50 harmonics are used for calculation of THD (n = 50 in the above equation). The maximum permissible THD for low voltage applications is 5% and the maximum individual voltage harmonic is 3%.

Presence of inductances in power systems causes higher order current harmonics to damp out more quickly. This implies that a high order harmonic is not as severe as a lower order one. THD, however, disregards this difference and treats all harmonics equally. Another figure of merit, known as the Weighted THD (WTHD), gives a better measure of harmonic pollution by using the order of each harmonic component as its weight factor. WTHD is used for comparison of harmonic performance of different methods and is defined as

$$\mathrm{WTHD} = \frac{\sqrt{\sum_{h=2}^{n} \left(\frac{V_h}{h}\right)^2}}{V_1} \qquad (7)$$

In order to study the harmonic performance of the set of SVM strategies, simulation results for combinations of normalized sampling frequency F_{sn}, modulation index m, and arrangement of space vectors within a sampling period are collected. Of the possible arrangement schemes, conventional (**0127**|**7210**), 120° bus-clamped (**012**|**210**, **032**|**230**) [5], and minimum loss SVM (**012**|**721**) [14] are considered. (In this implementation of 120° bus-clamped SVM, negative side of the dc-bus is chosen as the clamp to which each phase is connected for one-third of the fundamental period. This eliminates the $\mathbf{V}_7$ zero space-vector, leaving $\mathbf{V}_0$ as the only zero space-vector used. The performance in the case of using the positive side as clamp is similar, but a different sequence from what stated here should be used to keep the number of switchings at its minimum.)

As the study is confined to voltage harmonics, no-load conditions are simulated. In a real-world case, this leads to slightly different results, as the voltage drop across switches and line impedances as well as time-delays associated with the time-constant of the circuit exacerbate the performance.

The WTHD values for normalized sampling frequency F_{sn} and modulation index m are recorded. Three normalized sampling frequencies of 24 (1440 Hz), 48 (2880 Hz), and 96 (5760 Hz) (which are chosen to be integer multiples of 6 to prevent non-characteristic harmonics) are used.

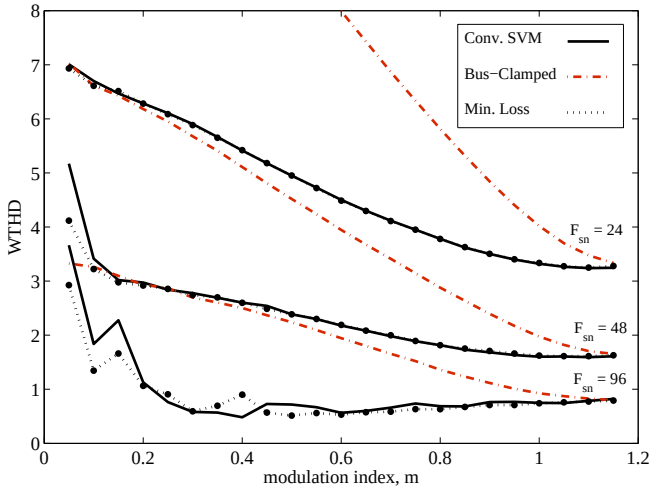

Fig. 7. The effect of different sampling frequencies (24, 48, and 96 times fundamental frequency) for three SVM strategies of conventional, 120° bus-clamped, and minimum-loss.

There is no difference between fundamental harmonic components of the constructed voltage waveforms. This is, however, expected as the fundamental is directly controlled by time-shares of voltage space-vectors.

Fig. 7 shows WTHD vs. m for different values of sampling frequency for the conventional, bus-clamped, and minimum-loss arrangements. Except for high values of F_{sn}, where the curve is almost flat (excluding the bus-clamped method for which the first group of harmonics cluster around $F_{sn}/2$), WTHD decreases as m increases. Since increasing the sampling frequency F_{sn} causes the harmonics to move to higher orders (clustering around the F_{sn} or $F_{sn}/2$, depending on the strategy), a higher F_{sn} always corresponds to a lower WTHD. This is the main advantage of operating at a higher sampling frequency in PWM switching schemes.

As such, a high modulation index m that remains in the linear region generally corresponds to a lower WTHD. This is particularly true for lower values of F_{sn} where the significant harmonic is of a low order. For a higher F_{sn}, as can be seen for the case of $F_{sn} = 96$, the effect of such harmonics is already small because of the weight used and this general trend is no longer valid.

V. Switching Loss Behavior

In addition to the harmonic content of generated output waveform, the losses associated with the converter are of fundamental importance. Furthermore, losses result in temperature increase in both the switches and the load, which could damage the device. Hence, it is important to estimate such losses.

In this section, temperature increase and losses of switches are estimated using the method presented in [15]. In addition to power electronic device electrical specifications, accurate modeling of losses needs values of thermal resistance and capacitance of the semiconductor and its heat sink. As these parameters are not always conveniently accesible and an error as high as 20% in temperature calculations is normal [16], the

results are mainly used as a qualitative measure for comparison of different methods. The PSCAD components used for calculation of the losses are shown in Fig. 8.

To assess the second category of losses, which occur in the load supplied by the converter, another figure of merit is used, which is the harmonically weighted loss factor [17]. It assumes an inductive load (e.g., a motor) for the converter and approximates the losses due to harmonics in the output waveform. The harmonically weighted loss factor σ is defined as

$$\sigma = \sum_{h=2}^{n} \frac{V_h^2}{(h\, f_1)^{3/2}} \qquad (8)$$

where f_1 is the fundamental frequency, h is the harmonic order, V_h is the hth voltage harmonic component, and n is the total number of harmonics considered (63 in this case). Note that as σ also reflects harmonic pollution of the waveform, its definition is close to WTHD.

Generally, the smaller the loss factor, the lesser the losses in the load. However, as the loss factor is defined essentially for a motor load, it is biased toward losses in the load and does not consider the converter switching losses, which are obtained in the previous method.

Switching losses and WTHD for the three aforementioned SVM schemes (conventional, 120° bus-clamped, and minimum-loss) as well as sinusoidal PWM are obtained. Thermal parameters of the Toshiba ST1500GXH24 are used for simulation. The voltage and current ratings of this device are 4500 V and 1500 A, respectively. For all cases the simulation is performed for $m = 0.8$, which is in the linear region. The sampling frequency is 2880 Hz, 48 times the fundamental frequency of 60 Hz.

For each switching scheme, junction temperature of the IGBT T_J, switching losses P_L, WTHD (as a measure of harmonic performance), and the loss factor σ are recorded. The dc-bus voltage is provided by two series 250-V dc sources. The load is 27 Ω at 60 Hz excitation. Load details are shown in Table II.

Simulation results are summarized in Table III. Although sinusoidal PWM demonstrates a moderate amount of converter losses, its WTHD (4%) is the highest among the four modulation methods studied. Loss factor of the sinusoidal PWM (1.00) is also higher than other methods, reflecting the non-optimized situation. The conventional SVM has the highest converter losses because of employing four states in each sampling period. On the other hand, its harmonic performance, as implied by a WTHD of 1.8%, is fairly good. Because of generation of low harmonic voltages, its loss factor is also small (0.28). The WTHD and loss factor of conventional SVM are comparable to the minimum-loss SVM, with the latter showing a modest superiority. Minimum-loss SVM, however, displays the lowest temperate increase and switching losses, hence the name. The 120° bus-clamped SVM strategy features close, but higher, switching losses than the minimum-loss method. Its loss factor (0.61) and WTHD (2.9) are inferior to those of the conventional and minimum-loss methods. Its first notable generated voltage harmonic is 22nd, while for the minimum-loss SVM it is the 20th.

Although the sampling frequency is kept constant in this study, note that as in the 120° bus-clamped and minimum-loss methods the number of switchings is smaller than the conventional SVM method, they can operate at a higher frequency (33% higher) and do not exceed thermal capability of switches, provided that the control circuitry is able to operate at higher frequencies.

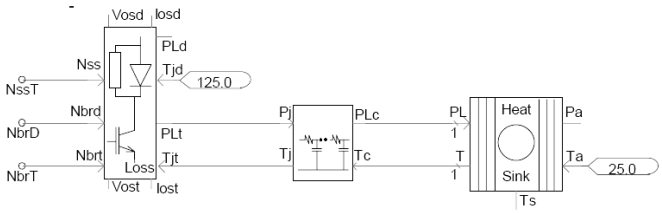

Fig. 8. Switching loss calculation blocks in PSCAD.

TABLE II
SIMULATION PARAMETERS FOR LOSS CALCULATIONS

V_{dc} (V)	f (Hz)	R (Ω)	L (mH)
2 × 250	60	25	24.4

TABLE III
COMPARISON OF SWITCHINGS LOSSES, TEMPERATURE, AND WTHD OF THE DIFFERENT MODULATION SCHEMES

Parameter	SPWM	SVM		
		(a)	(b)	(c)
T_J (increase, °C)	35	45	32	30
P_L (per-unit of SPWM)	1.00	1.33	0.83	0.80
WTHD (%)	4	1.8	2.9	1.8
σ (per-unit of SPWM)	1.00	0.28	0.61	0.27

(a) conventional SVM
(b) 120° bus-clamped SVM
(c) minimum-loss

VI. CONCLUSIONS

A digital implementation of space-vector modulation switching scheme for a transient simulation program has been presented in this paper. The model is capable of generating firing pulses for the whole range of operation of modulation as well as different switching strategies including conventional, bus-clamped, and minimum-loss SVM.

The harmonic performance of generated waveforms of each scheme is studied and compared to others (using WTHD as the figure of merit). It is found that the conventional and minimum-loss methods provide the least harmonic distortion, with the minimum-loss method, which only uses three space-vectors in each sampling cycle, producing lower switching losses. The losses in an inductive load are estimated using the loss factor, which in turn depends on the harmonic behavior of the modulation scheme. The loss factors of the conventional and minimum-loss SVM methods are almost identical and are the lowest. The downside of the minimum-loss method is that its first significant voltage harmonic is at a smaller order than

other methods. Sinusoidal PWM method has intermediate switching losses, but its WTHD is significantly higher.

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