ECE1371 Advanced Analog Circuits
Lecture 2

EXAMPLE DESIGN– PART 1

Richard Schreier
`richard.schreier@analog.com`

Trevor Caldwell
`trevor.caldwell@utoronto.ca`

Course Goals

- **Deepen understanding of CMOS analog circuit design through a top-down study of a modern analog system**

  The lectures will focus on Delta-Sigma ADCs, but you may do your project on another analog system.

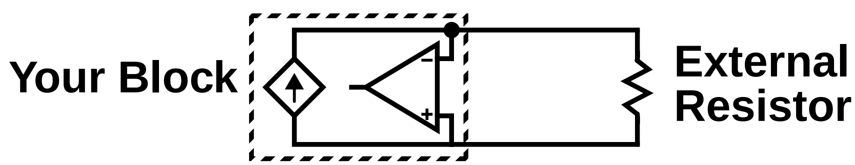
- **Develop circuit insight through brief peeks at some nifty little circuits**

  The circuit world is filled with many little gems that every competent designer ought to recognize.

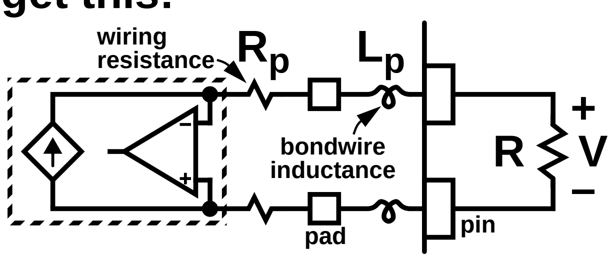
Date	Lecture			Ref	Homework
2008-01-07	RS	1	Introduction: MOD1 & MOD2	S&T 2-3, A	Matlab MOD2
2008-01-14	RS	2	Example Design: Part 1	S&T 9.1, J&M 10	Switch-level sim
2008-01-21	RS	3	Example Design: Part 2	J&M 14	Q-level sim
2008-01-28	TC	4	Pipeline and SAR ADCs		Arch. Comp.
2008-02-04	ISSCC– No Lecture				
2008-02-11	RS	5	Advanced $\Delta\Sigma$	S&T 4, 6.6, 9.4, B	CTMOD2; Proj.
2008-02-18	Reading Week– No Lecture				
2008-02-25	RS	6	Comparator & Flash ADC	J&M 7	
2008-03-03	TC	7	SC Circuits	J&M 10	
2008-03-10	TC	8	Amplifier Design		
2008-03-17	TC	9	Amplifier Design		
2008-03-24	TC	10	Noise in SC Circuits	S&T C	
2008-03-31	Project Presentation				
2008-04-07	TC	11	Matching & MM-Shaping		Project Report
2008-04-14	RS	12	Switching Regulator		Q-level sim

NLCOTD: Kelvin Connection

- **You want to this make this:**



- **But you get this:**



- **How to measure V accurately (for accurate feedback) when $R_p + \omega L_p$ is a significant fraction of R?**

Highlights
(i.e. What you will learn today)

1 MOD2 implementation

2 Switched-capacitor integrator

SC summer & DAC too

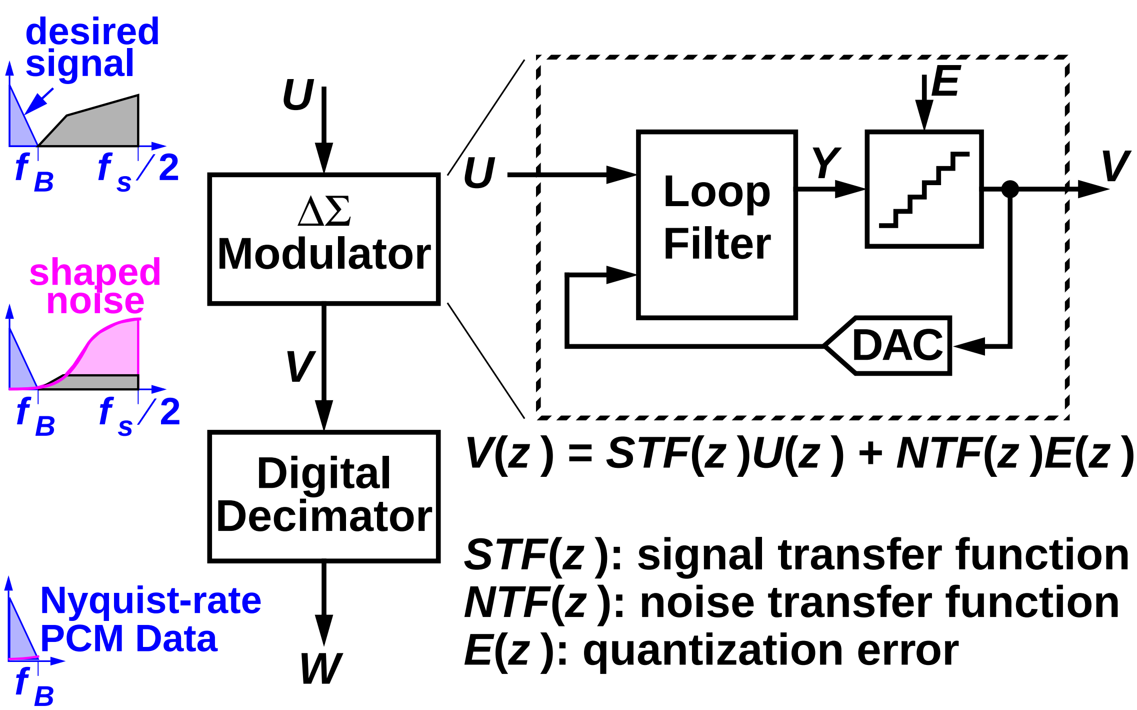
3 Dynamic-range scaling

4 kT/C noise

5 Some MOD2 nonlinear theory

6 Verification strategy

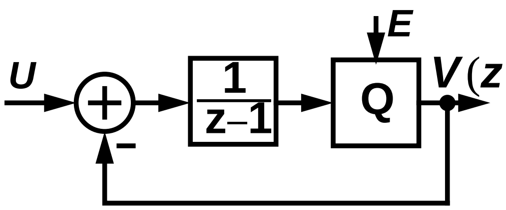
Review: A ΔΣ ADC System



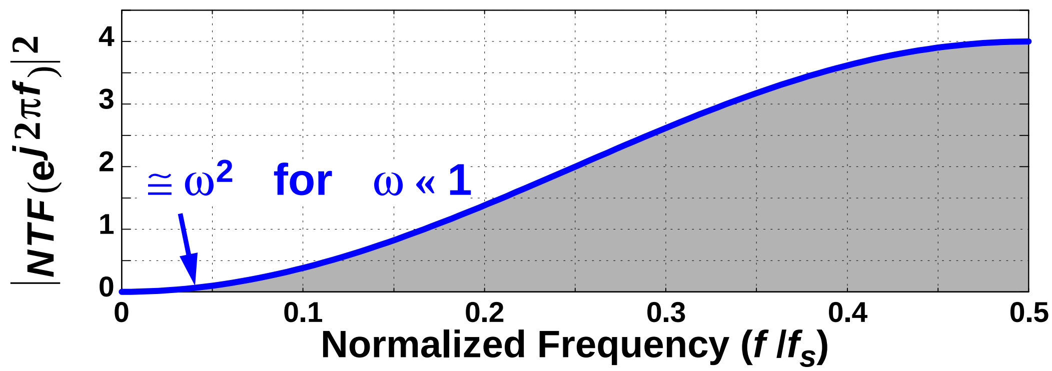
$V(z) = STF(z)U(z) + NTF(z)E(z)$

$STF(z)$: signal transfer function
$NTF(z)$: noise transfer function
$E(z)$: quantization error

Review: MOD1



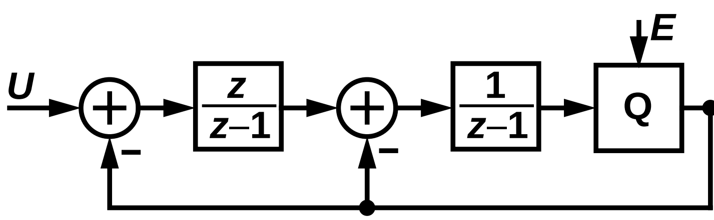
$$V(z) = NTF(z)E(z) + STF(z)U(z)$$
$$NTF(z) = (1 - z^{-1})$$
$$STF(z) = z^{-1}$$



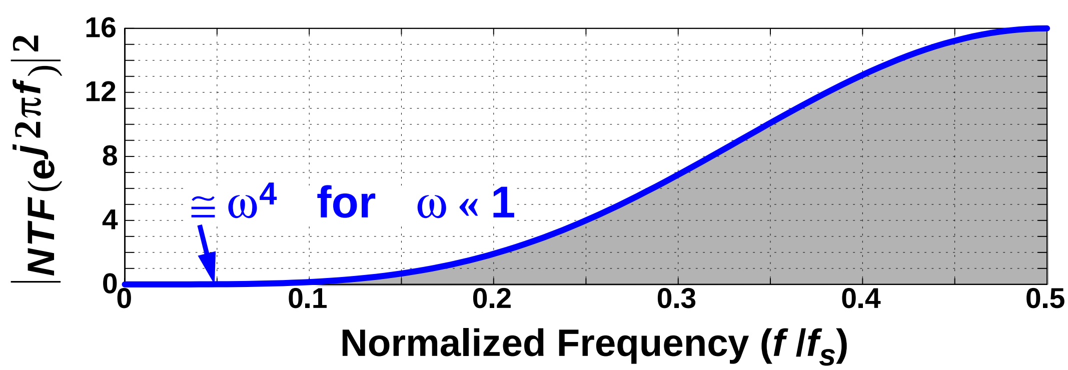
- **Doubling OSR improves SQNR by 9 dB**

  Peak SQNR $\approx$ **dbp**$(9 \cdot OSR^3 / (2\pi^2))$; **dbp**$(x) \equiv 10\log_{10}(x)$

Review: MOD2



$$NTF(z) = (1 - z^{-1})^2$$
$$STF(z) = z^{-1}$$

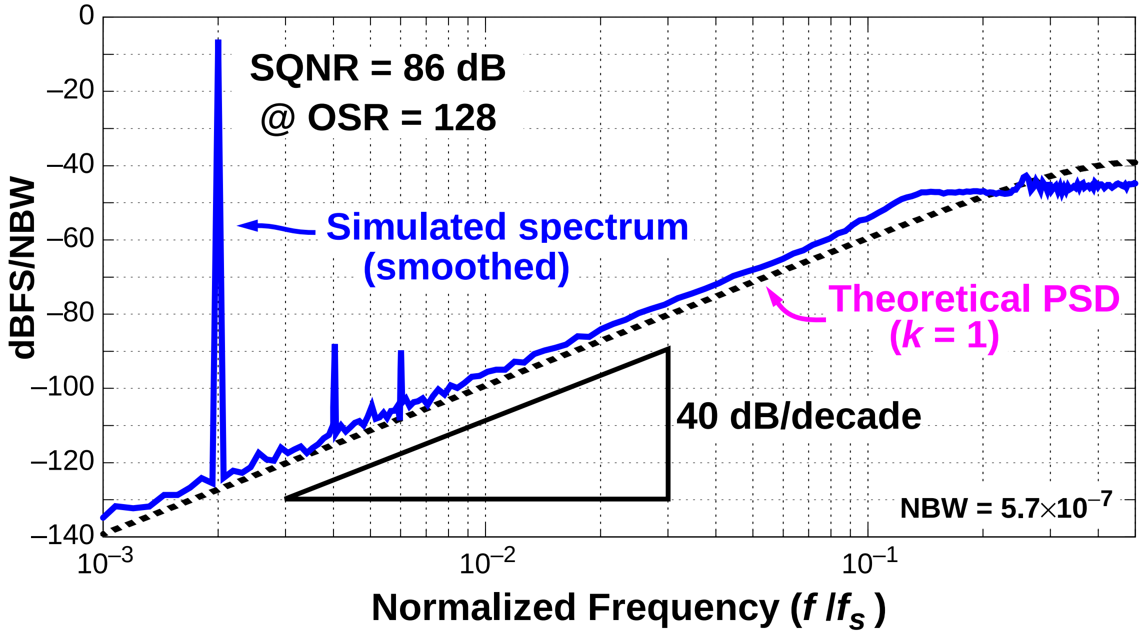


- **Doubling OSR improves SQNR by 15 dB**

  Peak SQNR $\approx$ **dbp**$((15 \cdot OSR^5)/(4\pi^4))$

Review: Simulated MOD2 PSD

Input at 50% of FullScale



Review: Advantages of $\Delta\Sigma$

- **ADC: Simplified Anti-Alias Filter**

  Since the input is oversampled, only very high frequencies alias to the passband. These can often be removed with a simple RC section.

  If a continuous-time loop filter is used, the anti-alias filter can often be eliminated altogether.

- **DAC: Simplified Reconstruction Filter**

  The nearby images present in Nyquist-rate reconstruction can be removed digitally.

\+ **Inherent Linearity**

  Simple structures can yield very high SNR.

\+ **Robust Implementation**

  $\Delta\Sigma$ tolerates sizable component errors.

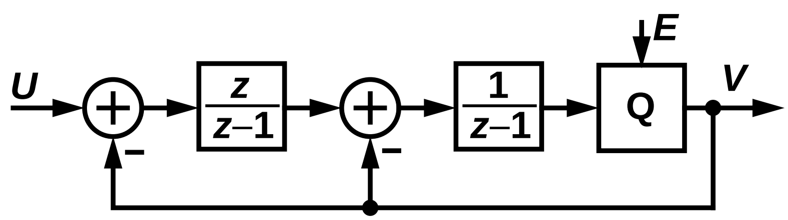
Let's Try Making One!

- **Clock at f_S = 1 MHz.**
  Assume BW = 1 kHz.

$$\Rightarrow OSR = f_s / (2 \cdot BW) = 500 \approx 2^9$$

- **MOD1: SQNR ≈ 9 dB/octave • 9 octaves = 81 dB**
- **MOD2: SQNR ≈ 15 dB/octave • 9 octaves =135 dB**
  Actually more like 120 dB.
- **SQNR of MOD1 is not bad, but SQNR of MOD2 is awesome!**
  In addition to MOD2's SQNR advantage, MOD2 is usually preferred over MOD1 because MOD2's quantization noise is more well-behaved.

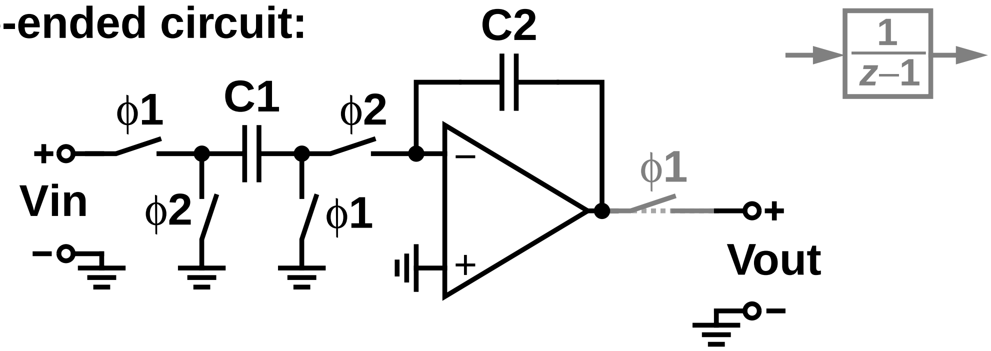
What Do We Need?



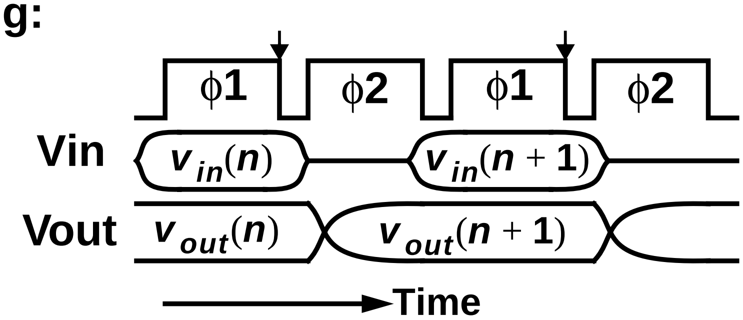
1. **Summation blocks**
2. **Delaying and non-delaying discrete-time integrators**
3. **Quantizer (1-bit)**
4. **Feedback DACs (1-bit)**
5. **Decimation filter (not shown)**
   Digital and therefore "easy"

Switched-Capacitor Integrator

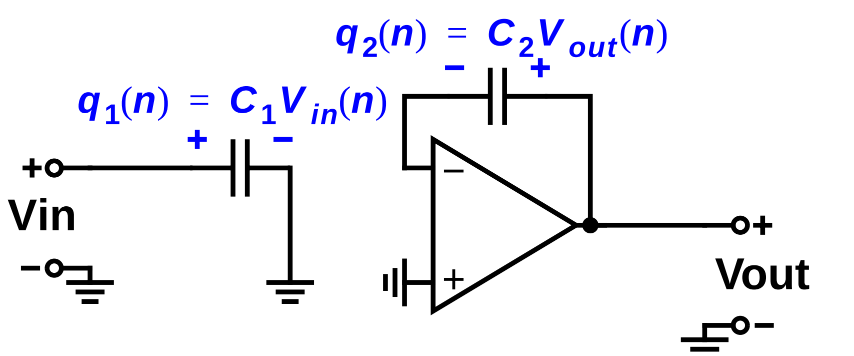
Single-ended circuit:



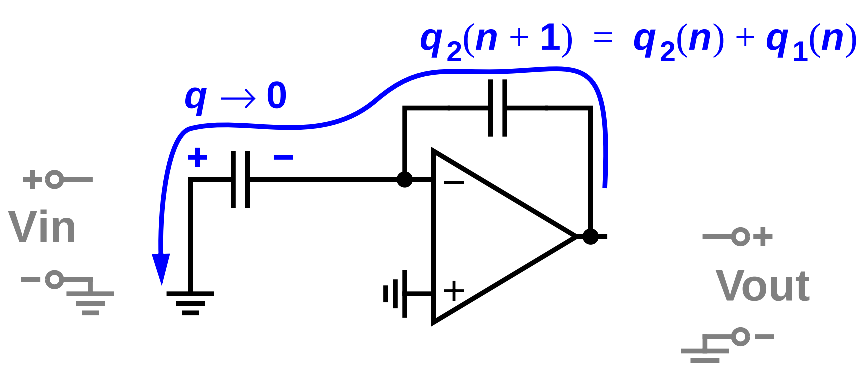
Timing:



φ1:



φ2:



$$q_2(n+1) = q_2(n) + q_1(n)$$

$$zQ_2(z) = Q_2(z) + Q_1(z)$$

$$Q_2(z) = \frac{Q_1(z)}{z-1}$$

- **This circuit integrates charge**

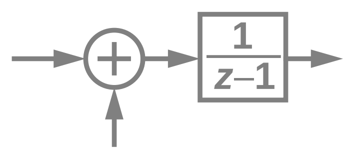
- **Since $Q_1 = C_1 V_{in}$ and $Q_2 = C_2 V_{out}$**

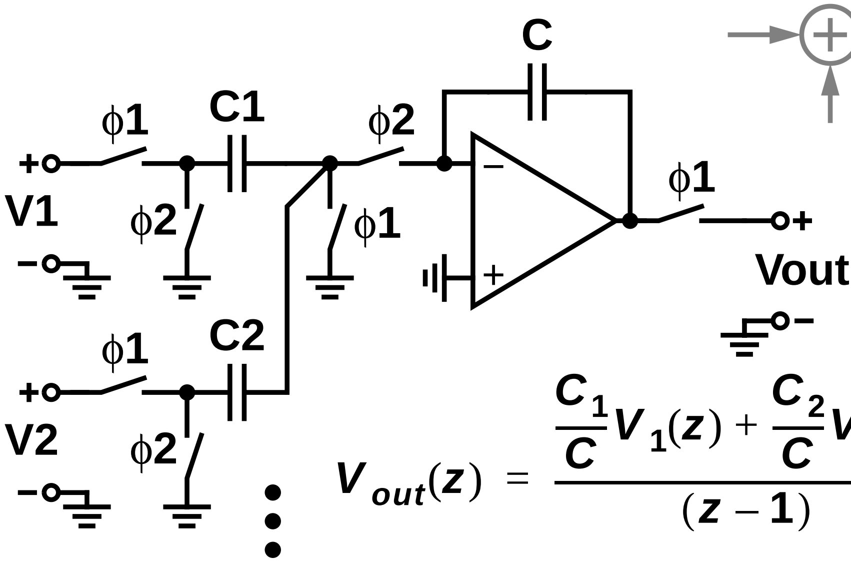
$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1/C_2}{z-1}$$

- **Note that the voltage gain is controlled by a *ratio* of capacitors**

  With careful layout, 0.1% accuracy is possible.

Summation + Integration

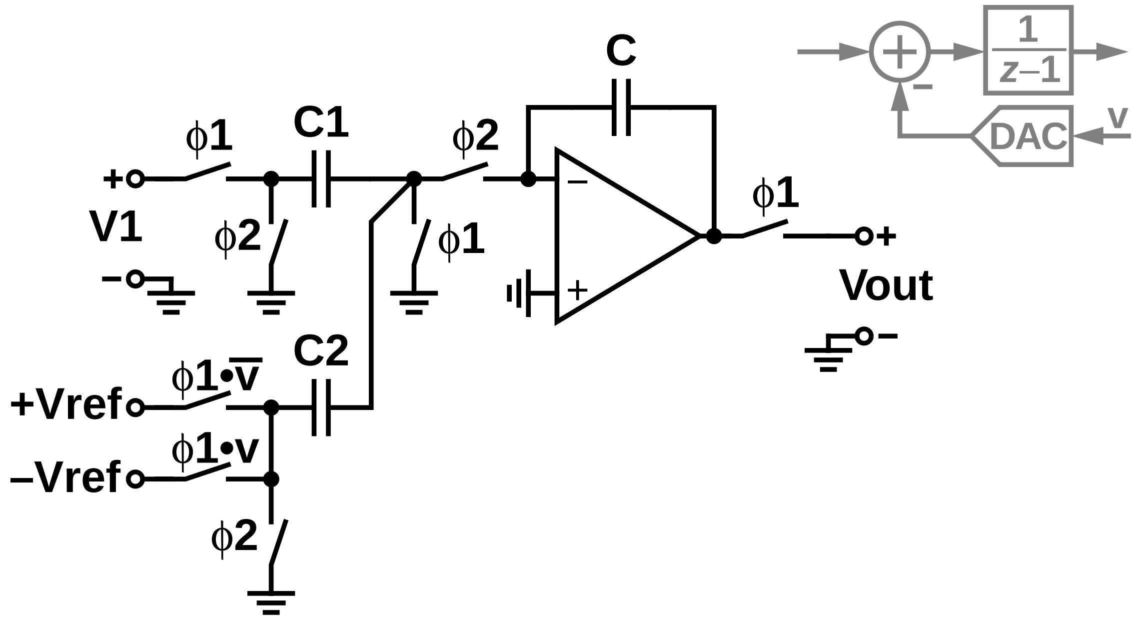




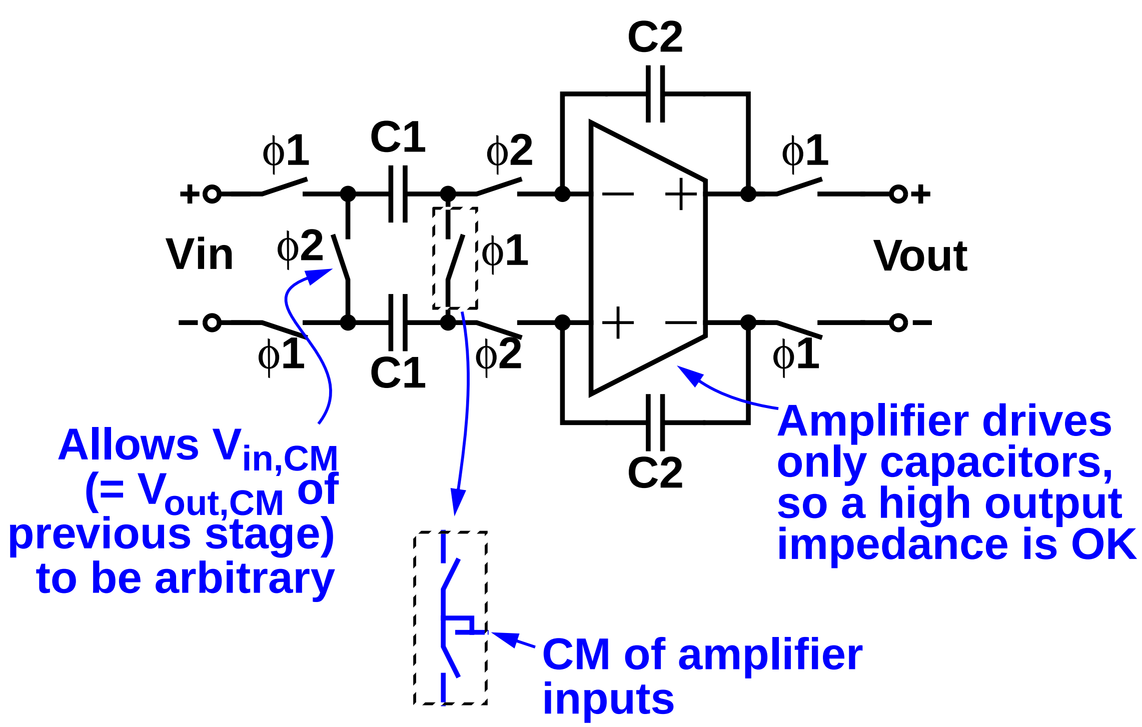
$$V_{out}(z) = \frac{\frac{C_1}{C}V_1(z) + \frac{C_2}{C}V_2(z)}{(z-1)}$$

$\Rightarrow$ **Adding an extra input branch accomplishes addition, with weighting**

1b DAC + Summation + Integration

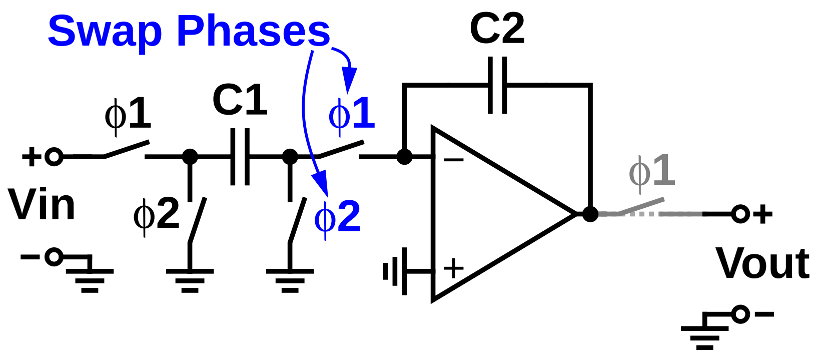


Differential Integrator

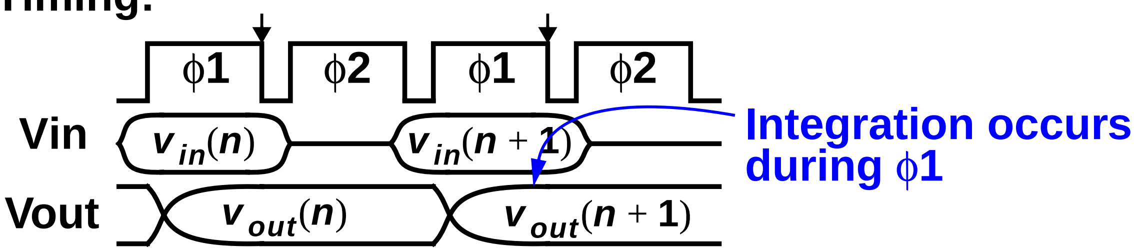


Non-Delaying Integrator

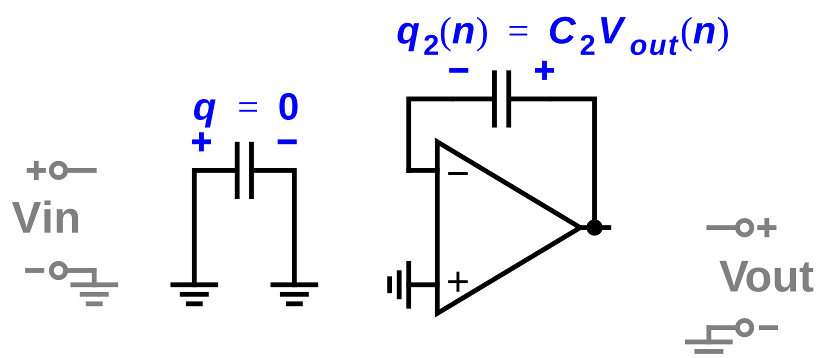
Single-ended circuit:



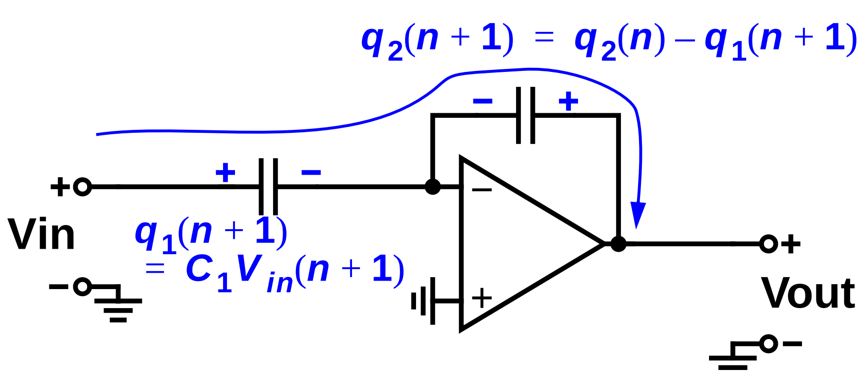
Timing:



φ2:



φ1:



$$q_2(n+1) = q_2(n) - q_1(n+1)$$

$$zQ_2(z) = Q_2(z) - zQ_1(z)$$

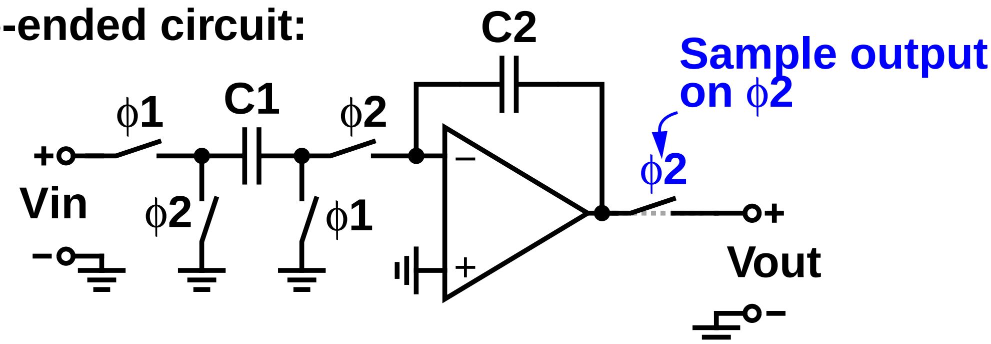
$$\frac{Q_2(z)}{Q_1(z)} = -\frac{z}{z-1}$$

$$\frac{V_{out}(z)}{V_{in}(z)} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z-1}$$

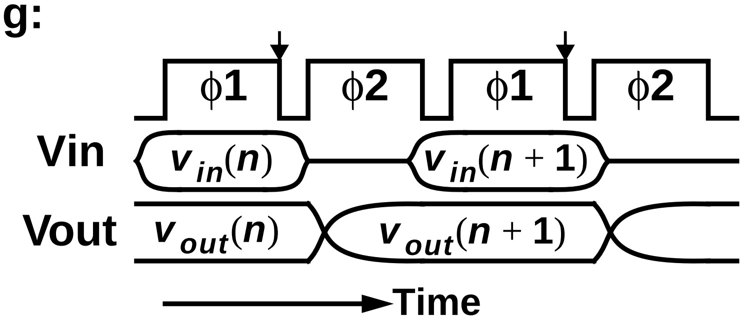
- Delaying (and inverting) integrator

"Half-Delay" Integrator

Single-ended circuit:



Timing:



Half-Delay Integrator

- Output is sampled on a different phase than the input
- Some use the notation $H(z) = \frac{z^{-1/2}}{z-1}$ to denote the shift in sampling time

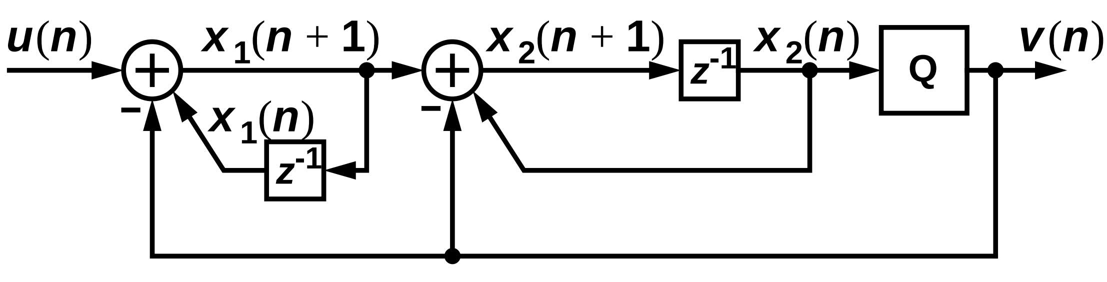
  I consider this an abuse of notation.

- An alternative method is to declare that the border between time *n* and *n*+1 occurs at the end of a specific phase, say $\phi 2$

$\Rightarrow$ A circuit which samples on $\phi 1$ and updates on $\phi 2$ is non-delaying, i.e. $H(z) = z/(z-1)$, whereas a circuit which samples on $\phi 2$ and updates on $\phi 1$ is delaying, i.e. $H(z) = 1/(z-1)$.

Timing in a ΔΣ ADC

- The safest way to deal with timing is to construct a timing diagram and verify that the circuit implements the desired difference equations
- E.g. MOD2:



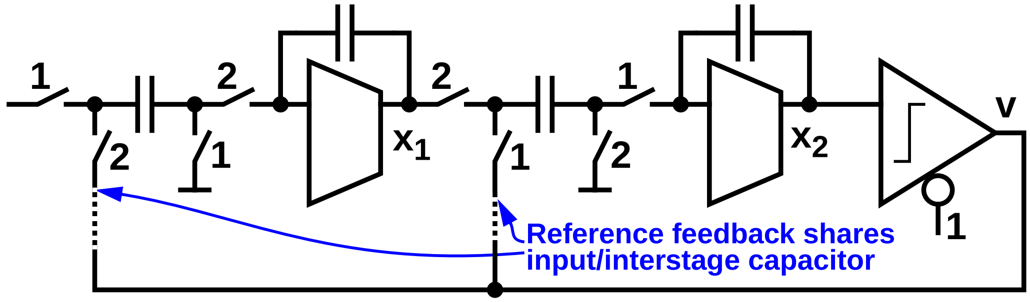
Difference Equations:

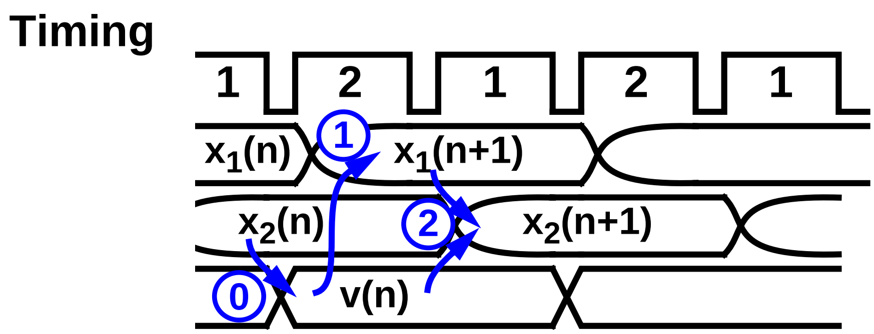
$$v(n) = Q(x_2(n)) \qquad (0)$$

$$x_1(n+1) = x_1(n) - v(n) + u(n) \qquad (1)$$

$$x_2(n+1) = x_2(n) - v(n) + x_1(n+1) \qquad (2)$$

Switched-Capacitor Realization





Timing looks OK!

Signal Swing

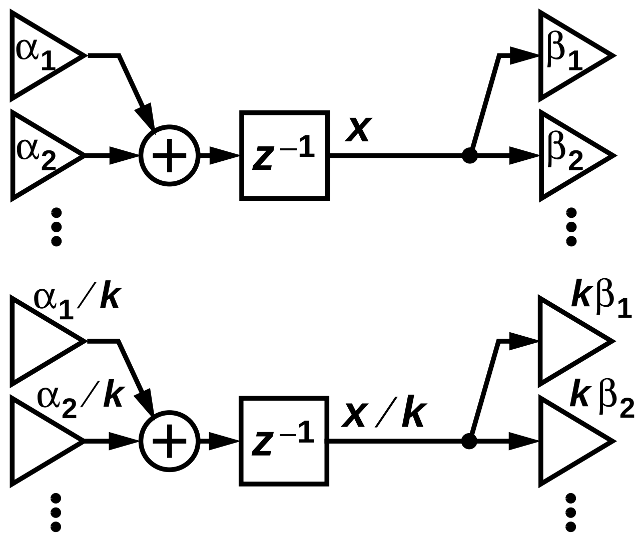
- So far, we have not paid any attention to how much swing the op amps can support, or to the magnitudes of u, V_{ref}, x_1 and x_2
- For simplicity, assume:
  the full-scale range of u is $\pm$1 V,
  the op-amp swing is also $\pm$1 V and
  V_{ref} = 1 V
- We still need to know the ranges of x_1 and x_2 in order to accomplish *dynamic-range scaling*

Dynamic-Range Scaling

- **In a linear system with known state bounds, the states can be scaled to occupy any desired range**

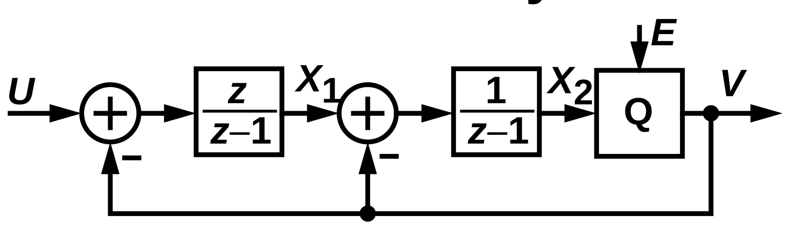
e.g. one state of original system:

state scaled by 1/*k*:



State Swings in MOD2

Linear Theory



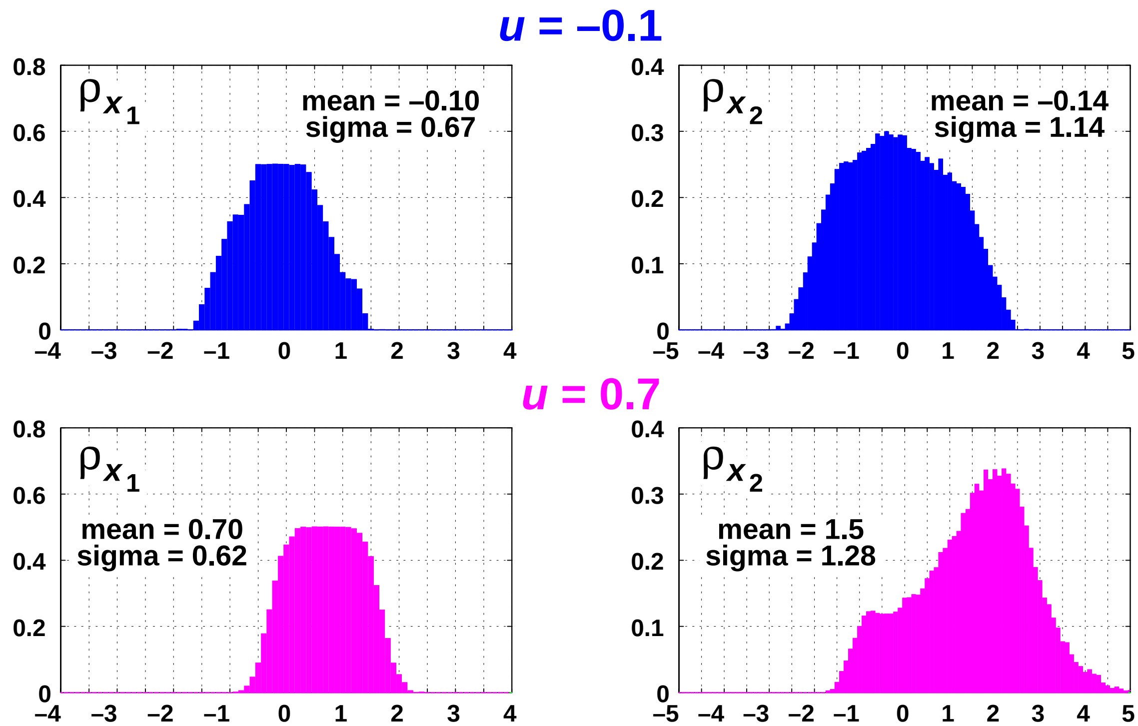
$$V = z^{-1}U + (1 - z^{-1})^2 E$$

$$X_1 = \frac{z}{z-1}(U - V) = U - (1 - z^{-1})E$$

$$X_2 = V - E = z^{-1}U + (-2z^{-1} + z^{-2})E$$

- **If u is constant and e is white with power $\sigma_e^2 = 1/3$, then $\bar{x}_1 = u$, $\sigma_{x_1}^2 = 2\sigma_e^2 = 2/3$, $\bar{x}_2 = u$ and $\sigma_{x_2}^2 = 5\sigma_e^2 = 5/3$**

Simulated Histograms



Observations

- **The match between simulations and our linear theory is fair for x_1, but poor for x_2**

  x_1's mean and standard deviation match theory, although x_1's distribution does not have the triangular form that would result if *e* were white and uniformly-distributed in [–1,1].

  x_2's mean is 50-100% high, its standard deviation is ~25% low, and the distribution is weird.

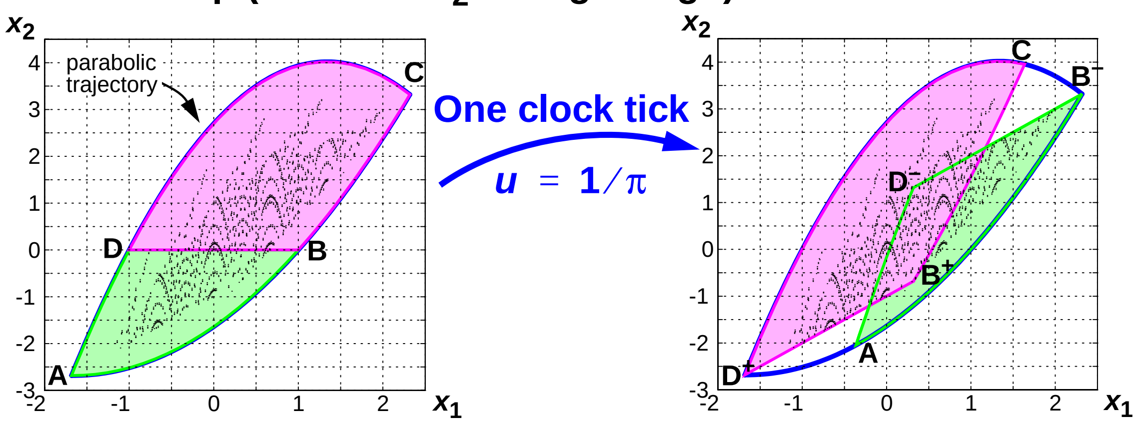
$\Rightarrow$ **Our linear theory is not adequate for determining signal swings in MOD2**

  No real surprise. Linear theory does not handle overload, i.e. where $x_1, x_2 \to \infty$ when $u > 1$.

- **Is there a better theory?**

MOD2's Dynamics

- **Second-order DT system with a step nonlinearity**
  - **For a constant input, $(x_1(n), x_2(n))$ follow parabolic trajectories in state-space, except when crossing the step (i.e. when x_2 changes sign).**



- **If the image is inside the original, we have a *positively-invariant set***

MOD2 DC-Input State Bounds

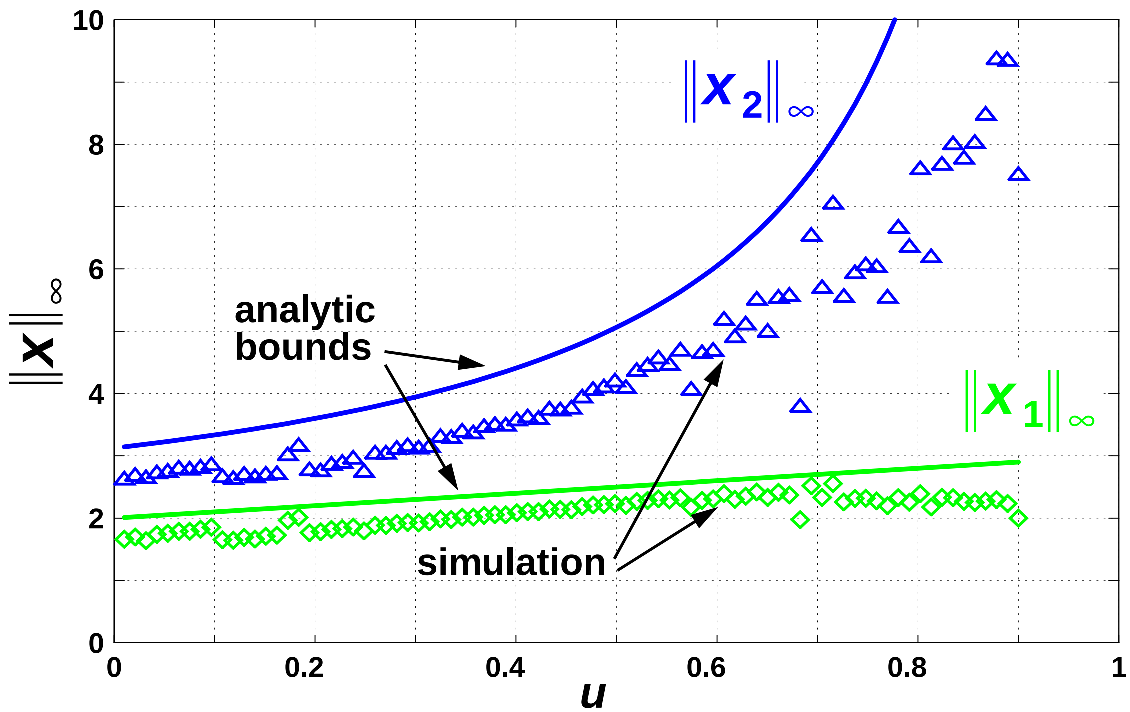
- **By computing the state-space trajectories with u as a parameter, Hein & Zakhor [ISCAS 1991] determined invariant sets analytically and thereby arrived at the following bounds for $|u| \le 1$:**

$$|x_1| \le |u| + 2$$

$$|x_2| \le \frac{(5-|u|)^2}{8(1-|u|)}$$

- **Note that the bound on $|x_2| \to \infty$ as $|u| \to 1$**
  - **In order to use this formula for dynamic-range scaling, we need to restrict the u to a fraction of full-scale.**

Comparison with Simulation



State Bounds for MOD2

Nonlinear Theory

So we do have some better theory, but it

1. **Appears to be conservative**

   Especially for u close to FS.

2. **Predicts that x_2 can be arbitrarily large**

   Simulations indicate that x_2 does get big as $|u| \to 1$, but not quite as big as the theory predicts.

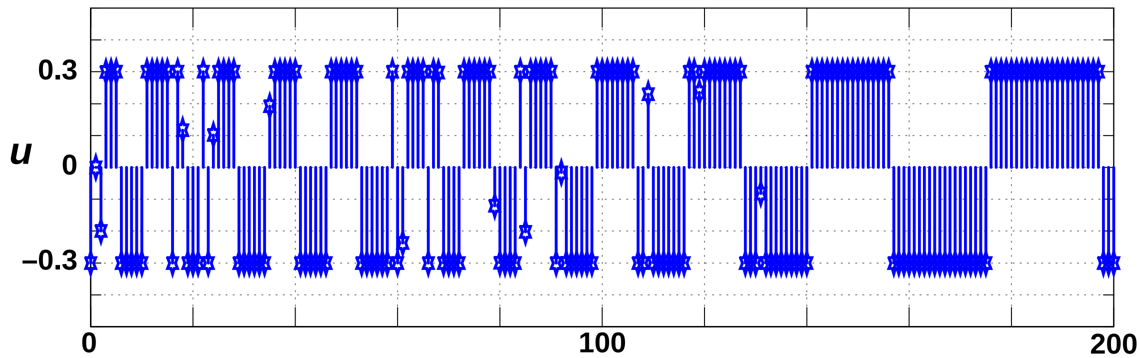
3. **Assumes the input is constant**

   Attempts to generalize the method for arbitrary inputs could only prove stability for $\|u\|_\infty < 0.1$.

   Inputs with $\|u\|_\infty = 0.3$ have been constructed which drive MOD2 unstable!

Example Hostile Input

$\|u\|_\infty = 0.3$



- **Input signal chosen to cause the comparator in MOD2 to make bad decisions**

  Requires knowledge of MOD2's internal state.

- **Inputs like this are unlikely to occur in practice**

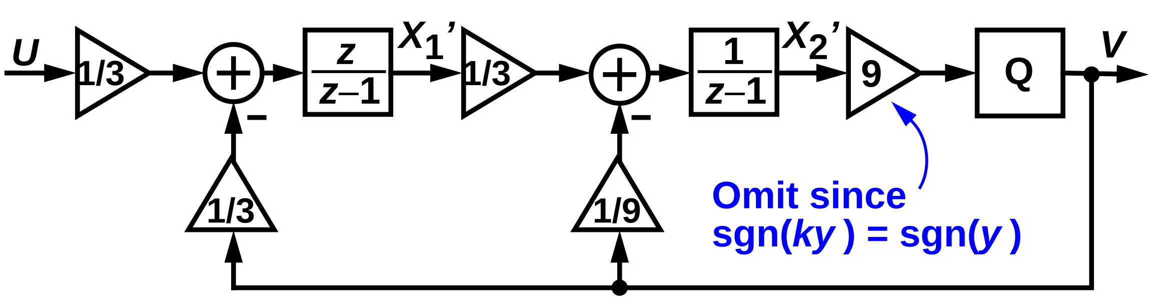
Scaled MOD2

- **Take $\|x_1\|_\infty = 3$ and $\|x_2\|_\infty = 9$**

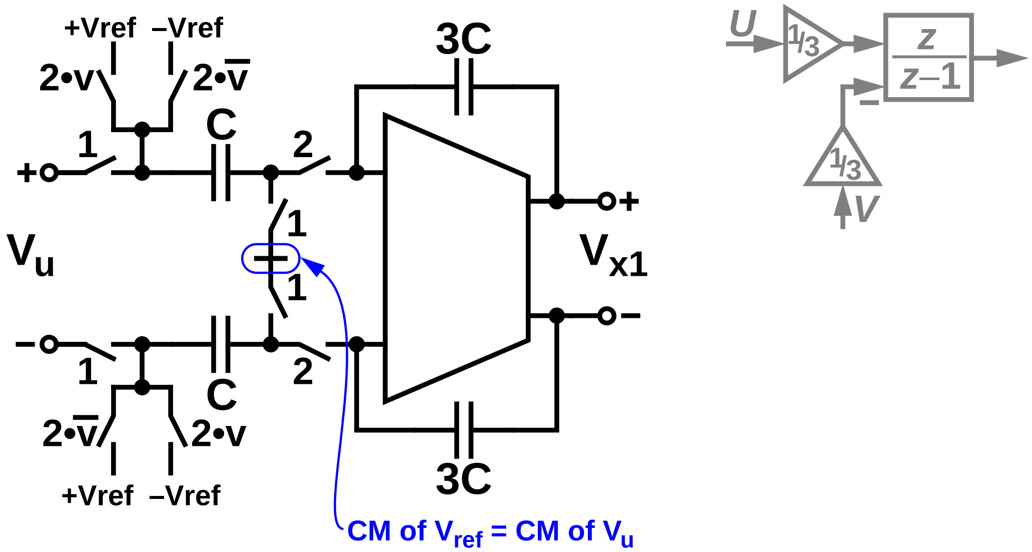
  The first integrator should not saturate.

  The second integrator will not saturate for dc inputs up to –3 dBFS and possibly as high as –1 dBFS.

- **Our scaled version of MOD2 is then**

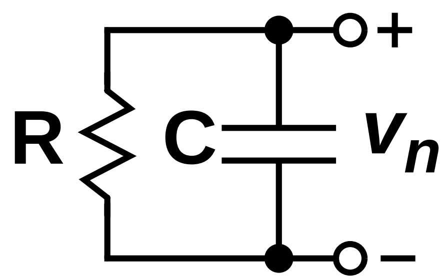


First Integrator (INT1)
Shared Input/Reference Caps



- **How do we determine C?**

kT/C Noise



- **Fact: Regardless of the value of *R*, the mean-square value of the voltage on *C* is**

$$\overline{v_n^2} = \frac{kT}{C}$$

where *k* = 1.38 $\times 10^{-23}$ J/K is *Boltzmann's constant* and *T* is the temperature in Kelvin

The ms noise charge is $\overline{q_n^2} = C^2\overline{v_n^2} = kTC$.

Derivation of kT/C Noise

- *Equipartition of Energy* physical principle: "In a system at thermal equilibrium, the average energy associated with any degree of freedom is $\frac{1}{2}$kT."

  This applies to the kinetic energy of atoms (along each axis of motion), vibrational energy in molecules and to the potential energy in electrical components.

- Fact: The energy stored in a capacitor is $\frac{1}{2}CV^2$

- So, according to equipartition, $\frac{1}{2}\overline{CV^2} = \frac{1}{2}kT$, or

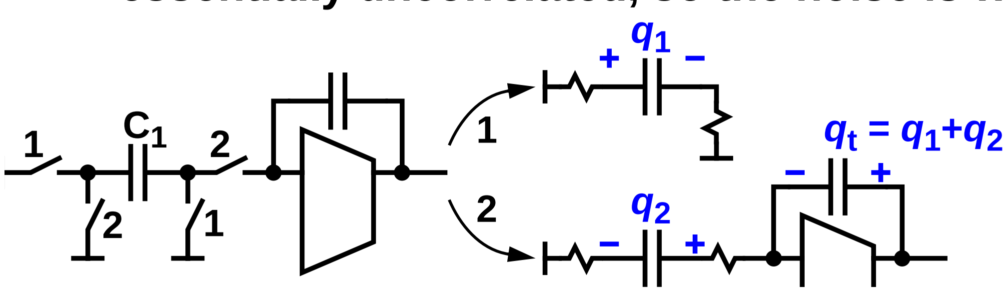
$$\overline{V^2} = \frac{kT}{C}$$

Implications for an SC Integrator

- Each charge/discharge operation has a random component

  The amplifier plays a role during phase 2, but we'll assume that the noise in both phases is just kT/C. We'll revisit this assumption in Lecture 10.

- For a given cap, these random components are essentially uncorrelated, so the noise is white

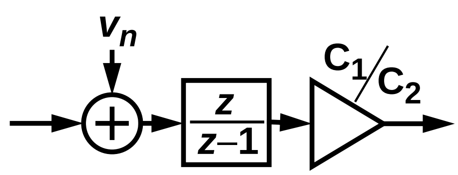


$$\overline{q_1^2} = \overline{q_2^2} = kTC_1$$

$$\overline{q_t^2} = \overline{q_1^2} + \overline{q_2^2} = 2kTC_1$$

Integrator Implications (cont'd)

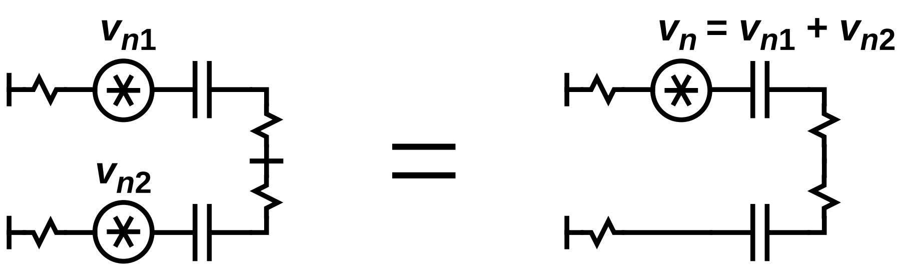
- **This noise charge is equivalent to a noise voltage with ms value $\overline{v_n^2} = 2kT/C_1$ added to the input of the integrator:**



- **This noise power is spread uniformly over all frequencies from 0 to $f_s/2$**

$\Rightarrow$ **The power in the band $[0, f_B]$ is v_n^2/OSR**

Differential Noise



$$\overline{v_n^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2}$$

- **Twice as many switched caps**
  $\Rightarrow$ twice as much noise power
- **The input-referred noise power in our differential integrator is**

$$\overline{v_n^2} = 4kT/C_1$$

INT1 Absolute Capacitor Sizes

For SNR = 100 dB @ –3-dBFS input

- The signal power is

$$\overline{v_s^2} = \underbrace{\frac{1}{2}}_{-3\text{ dBFS}} \bullet \underbrace{\frac{(1\text{ V})^2}{2}}_{\frac{A^2}{2}} = 0.25\text{ V}^2$$

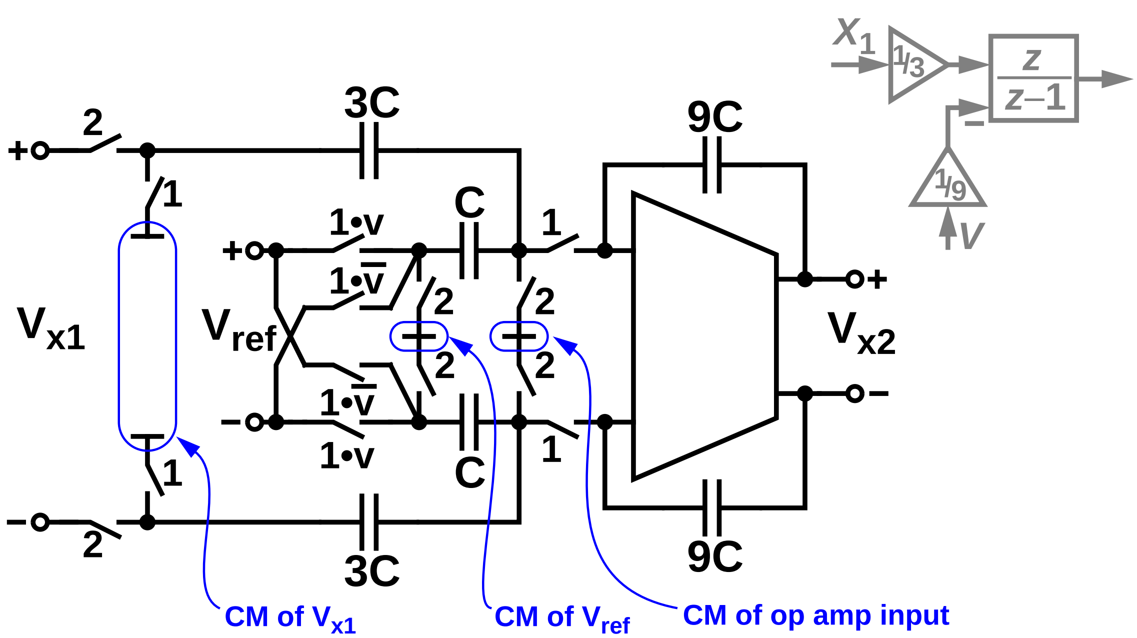
- Therefore we want $\overline{v_{n,\text{ in-band}}^2} = 0.25 \times 10^{-10}\text{ V}^2$
- Since $\overline{v_{n,\text{ in-band}}^2} = \overline{v_n^2}/OSR$

$$C_1 = \frac{4kT}{\overline{v_n^2}} = 1.33\text{ pF}$$

- If we want 10 dB more SNR, we need 10x caps

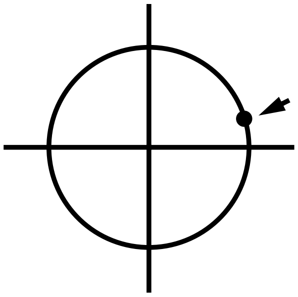
Second Integrator (INT2)

Separate Input and Feedback Caps



INT2 Absolute Capacitor Sizes

- **In-band noise of second integrator is greatly attenuated**



$\omega_B = \dfrac{\pi}{OSR}$

INT1 gain @ pb edge: $A = \dfrac{1/3}{\omega_B} = \dfrac{OSR}{3\pi}$

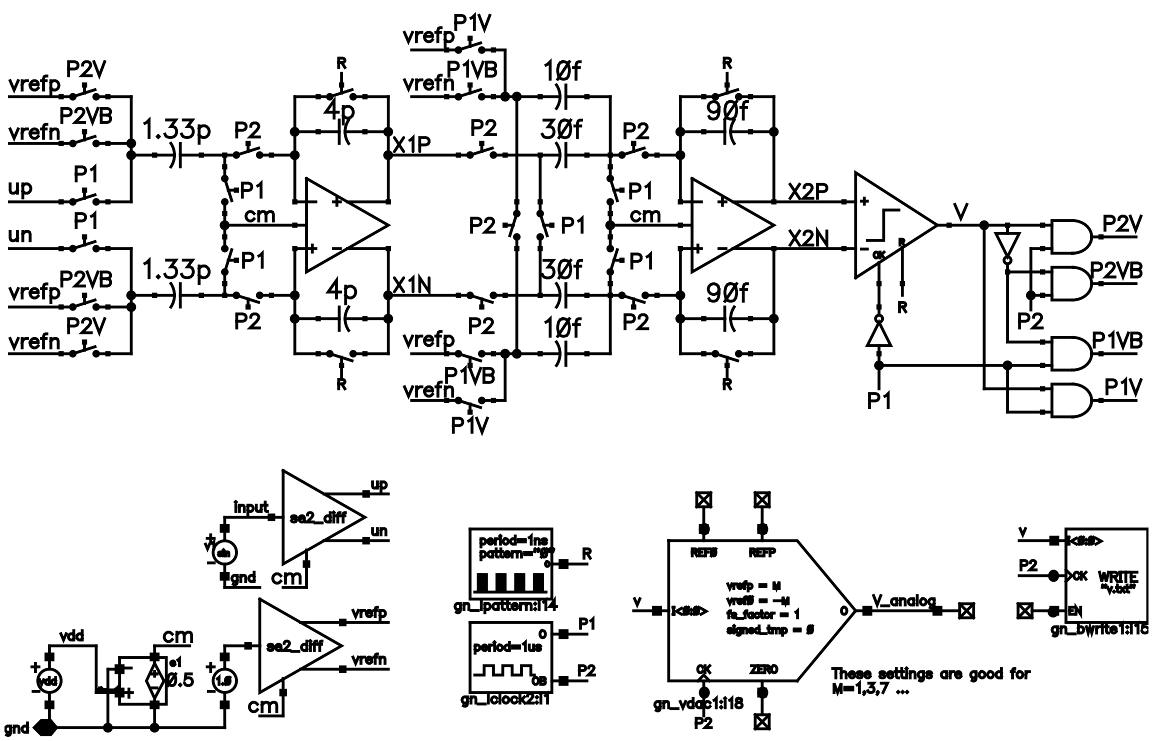
INT2 noise attenuation: $> OSR \cdot A^2 \approx 10^6$

$\Rightarrow$ **Capacitor sizes not dictated by thermal noise**

- **Charge injection errors and desired ratio accuracy set absolute size**

  A reasonable size for a small cap is currently ~10 fF.

Behavioral Schematic



Verification

Open-loop verification

1 Loop filter

2 Comparator

Since MOD2 is a 1-bit system, all that can go wrong is the polarity and the timing. Usually the timing is checked by (1), so this verification step is not needed.

Closed-loop verification

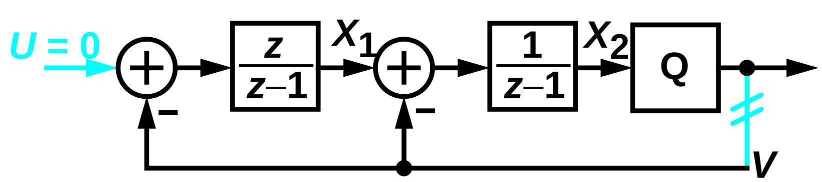
3 Swing of internal states

4 Spectrum: SQNR, STF gain

5 Sensitivity, start-up, overload recovery, …

Loop-Filter Check— Theory

- Open the feedback loop, set $u = 0$ and drive an impulse through the feedback path



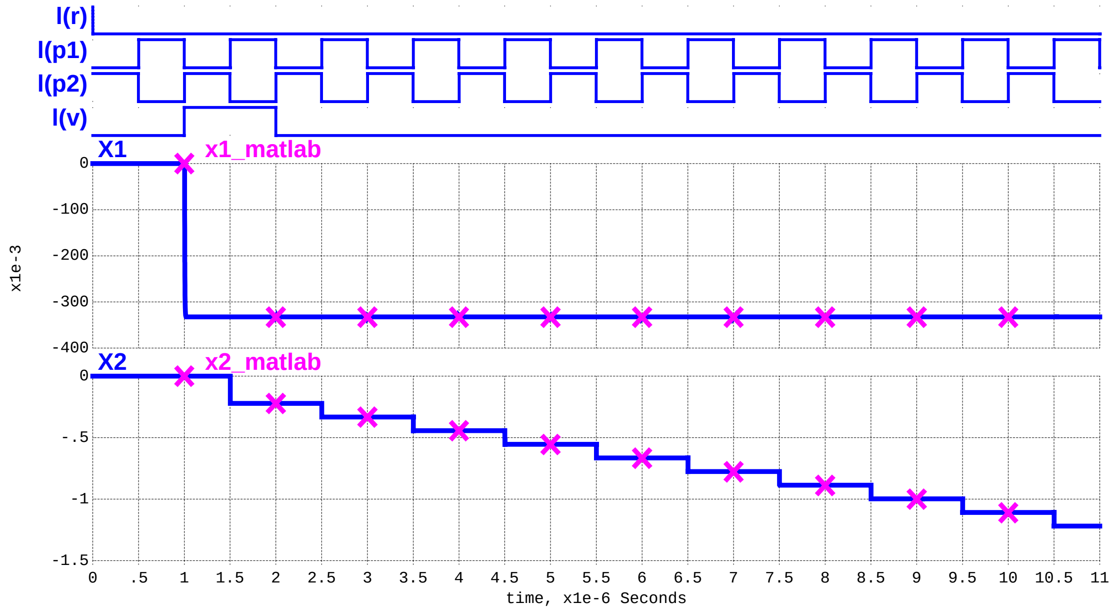
$$X_2 = \frac{-1}{z-1}\left(1 + \frac{z}{z-1}\right)Y$$

$$\therefore y(n) = \{1, 0, 0, \ldots\} \Rightarrow x_2(n) = \{-2, -3, -4, \ldots\}$$

- If x_2 is as predicted then the loop filter is correct

At least for the feedback signal, which implies that the NTF will be as designed.

Loop Filter Check— Practice*



*. "In theory there is no difference between theory and practice.
But in practice there is."

Hey! You Cheated!

- **An impulse is {1,0,0,…}, but a binary DAC can only output ±1, i.e. it cannot produce a 0**

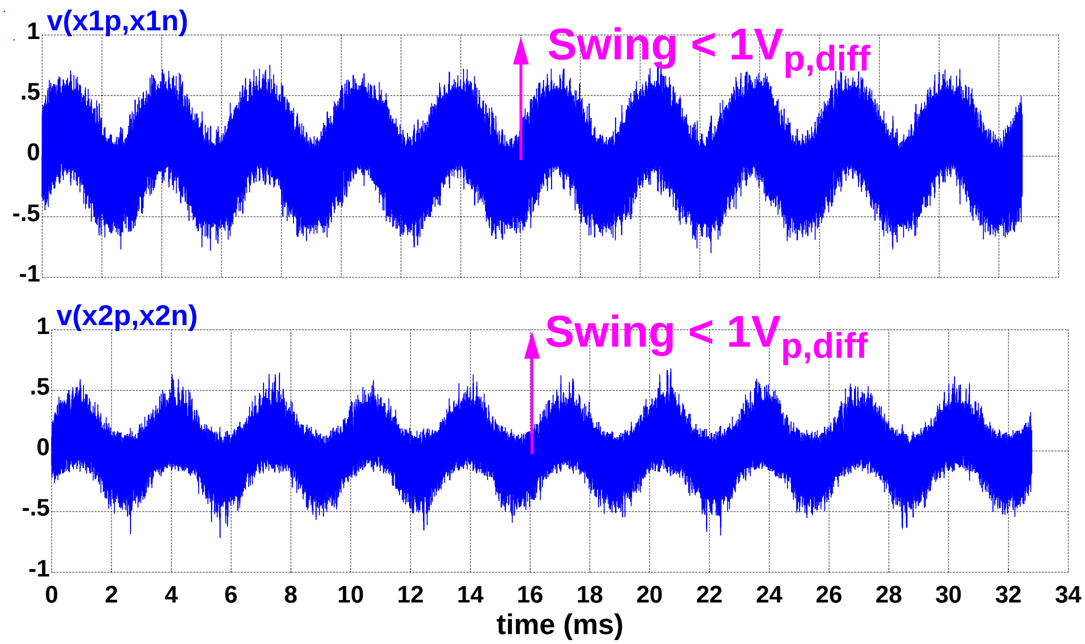
Q: So how can we determine the impulse response of the loop filter through simulation?

**A: Do two simulations: one with v = {–1,–1,–1,…} and one with v = {+1,–1,–1,…}.
Then take the difference.
According to superposition, the result is the response to v = {2,0,0,…}, so divide by 2.**

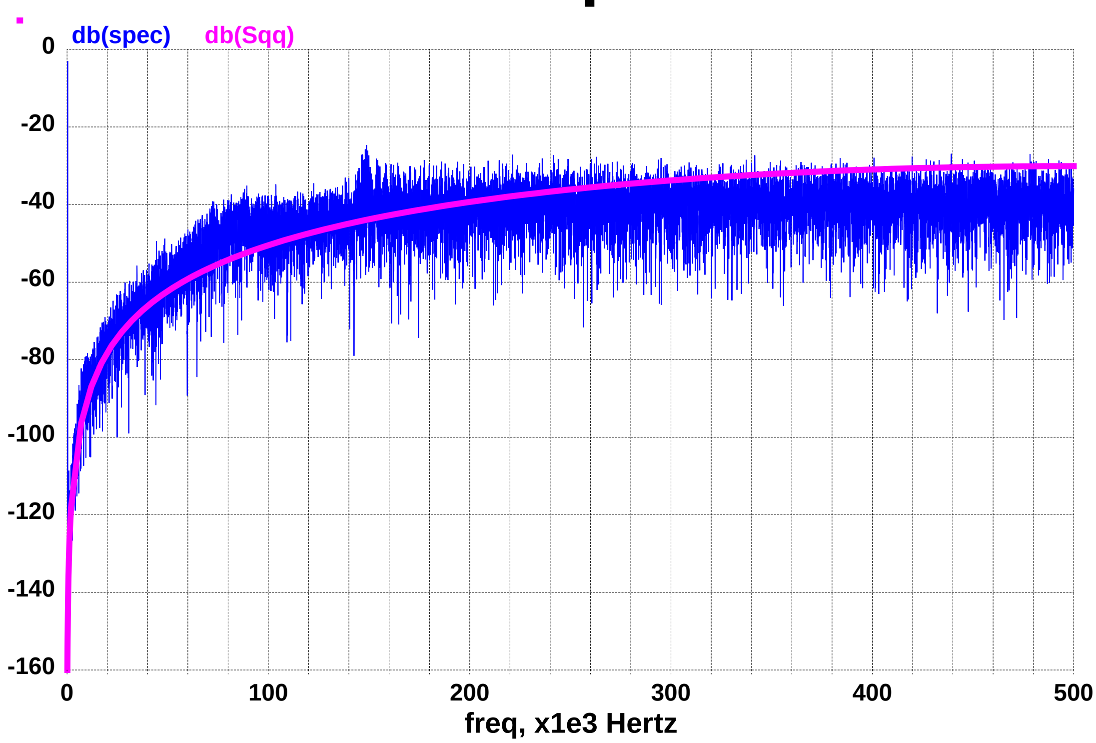
To keep the integrator states from growing too quickly, you could also use v = {–1,–1,+1,–1,…} and then v = {+1,–1,+1,–1,…}.

Simulated State Swings

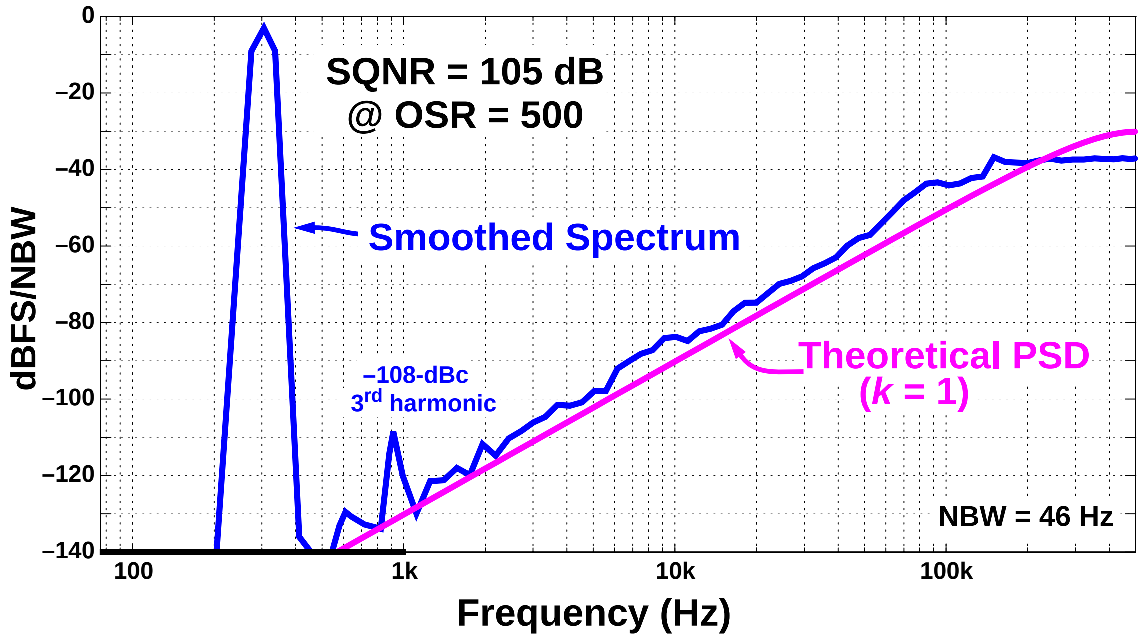
–3-dBFS ~300-Hz sine wave



Unclear Spectrum



Professional Spectrum



- SQNR dominated by –109-dBFS 3rd harmonic

Implementation Summary

1. Choose a viable SC topology and manually verify timing
2. Do dynamic-range scaling

   You now have a set of capacitor ratios.

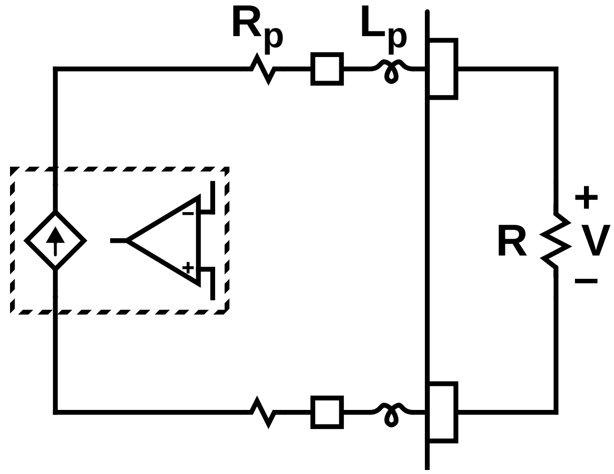
   Verify operation: loop filter, timing, swing, spectrum.
3. Determine absolute capacitor sizes

   Verify noise.
4. Determine op-amp specs and construct a transistor-level schematic

   Verify everything.
5. Layout, fab, debug, document, get customers, sell by the millions, go public, …

NLCOTD: Kelvin Connection

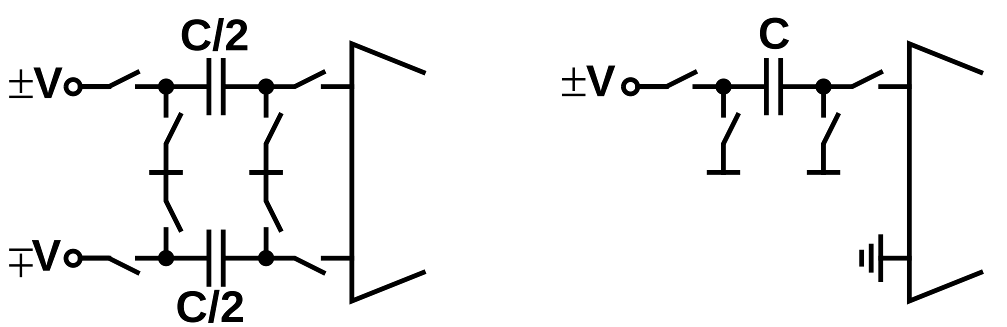
- **How to measure *V* accurately when $R_p + \omega L_p$ is a significant fraction of *R*?**



- **Use dedicated wires for sensing**
  Also called a "4-wire," "Force/Sense" or "Current/ Potential" connection. Common in power supplies.

Differential vs. Single-Ended

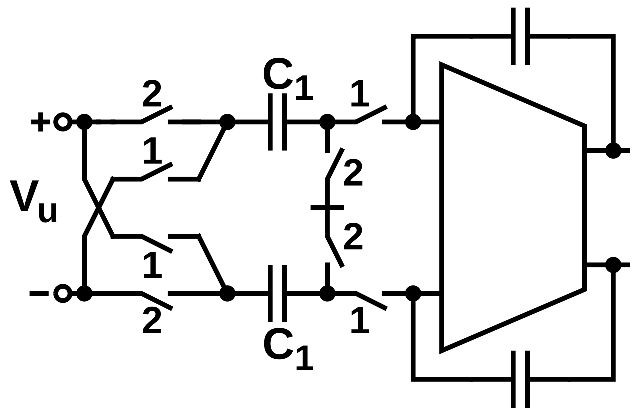
- **Differential is more complicated and has more caps and more noise $\Rightarrow$ single-ended is better?**



$$SNR = \frac{(2V)^2/2}{4kT/(C/2)} = \frac{CV^2}{4kT} \qquad SNR = \frac{V^2/2}{2kT/C} = \frac{CV^2}{4kT}$$

- **Same capacitor area $\Rightarrow$ same SNR**
  Differential is generally preferred due to rejection of even-order distortion and common-mode noise/ interference.

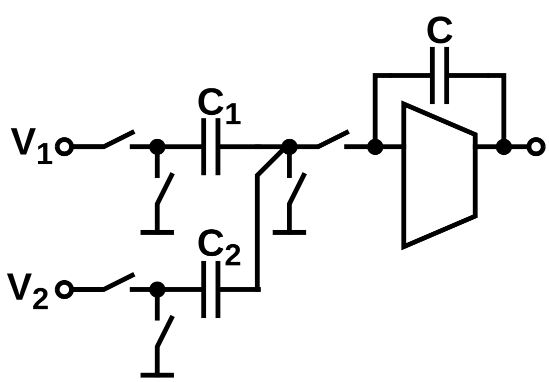
Double-Sampled Input



- Doubles the effective input signal
- Allows C_1 to be $1/4$ the size for the same SNR
- Doubles the sampling rate of the signal, thereby easing AAF further

Shared vs. Separate Input Caps

- Separate caps $\Rightarrow$ More noise:



V_1 input: $\overline{v_{n1}^2} = 2kT/C_1$

V_2 input: $\overline{v_{n2}^2} = 2kT/C_2$

V_2 gain / V_1 gain: C_2/C_1

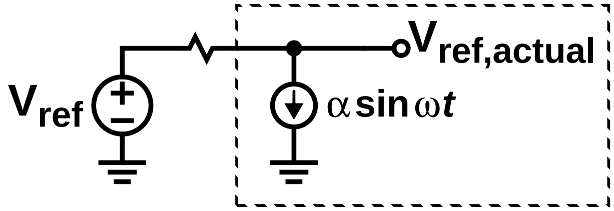
v_{n2} referred to V_1: $v_{n2}C_2/C_1$

Total noise referred to V_1:
$(2kT/C_1)(1 + C_2/C_1)$

- But using separate caps allows input CM to be different from reference CM, and so is often preferred in a general-purpose ADC

Signal-Dependent Ref. Loading

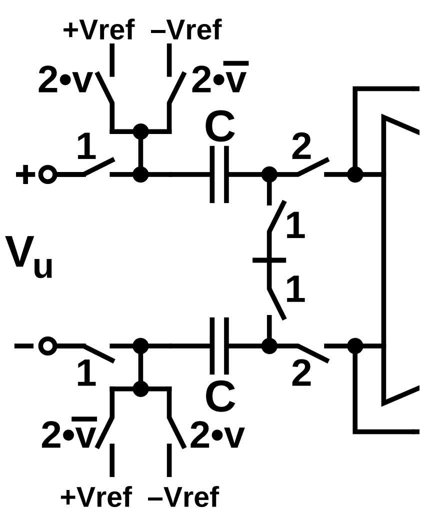
- **Another practical concern is the current draw from the reference**

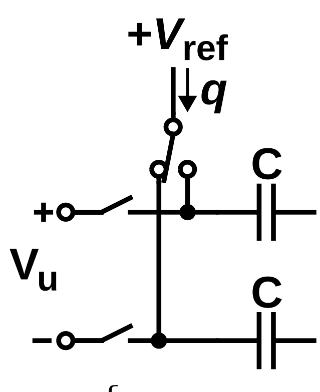


$$\text{ADC Output} \propto \frac{V_{in}}{V_{ref}(1-\varepsilon\sin\omega t)} \approx \frac{V_{in}}{V_{ref}}(1+\varepsilon\sin\omega t)$$

- **If the reference current is signal-related, harmonic distortion can result**

Shared Caps and Ref. Loading





$$q = \begin{cases} C(V_{ref} - V_u/2)\ ,\ v = +1 \\ C(V_{ref} + V_u/2)\ ,\ v = -1 \end{cases}$$

Thus

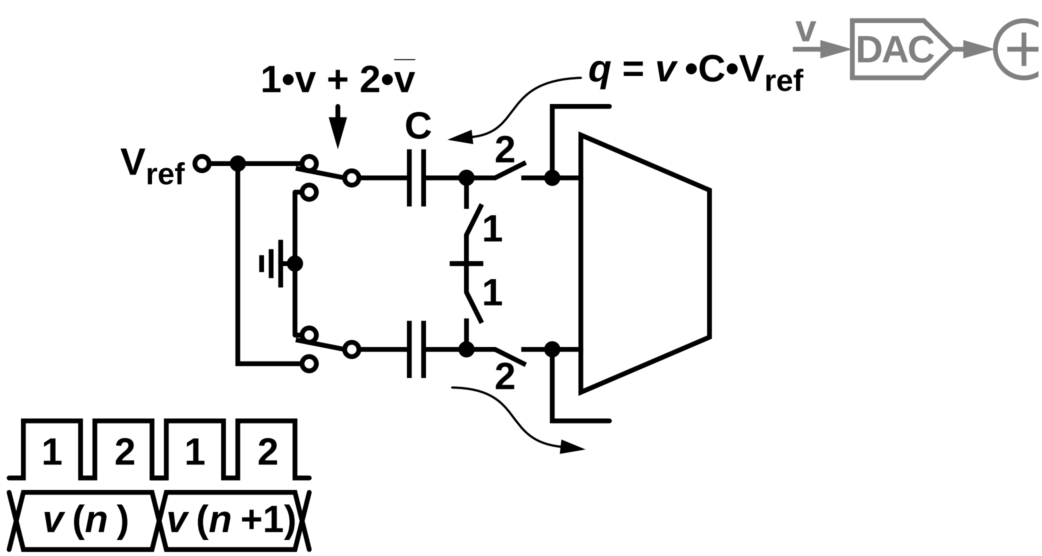
$$\bar{I} = \frac{C}{T}(V_{ref} - v \cdot V_u / 2)$$

- If $u = A\sin\omega_u t$, then $v = u + error$ also contains a component at ω_u and thus I contains a component at $\omega = 2\omega_u$.
- Since ADC Output $\propto V_{in}(1 + \varepsilon\sin\omega t)$, the signal-dependent reference current in our circuit can produce 3rd-harmonic distortion

  Also, the load presented to the driving circuit is dependent on *v* and this noisy load can cause trouble.
- With separate caps, the reference current is signal-independent

  Yet another reason for using separate caps.

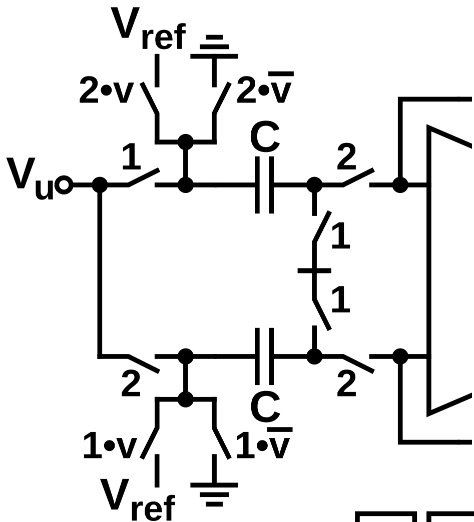
Unipolar Reference

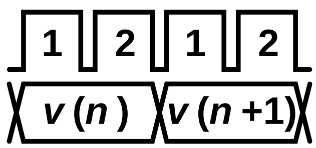


- Be careful of the timing of *v* relative to the integration phase!

Single-Ended Input

Shared Caps





Full-scale range of V_u is $[0,V_{ref}]$.

Homework #2

Construct a differential switched-capacitor implementation of MOD2 using ideal elements and verify it. Your circuit should accept a single-ended input and use a unipolar 1-V reference.

Scale the circuit such that [0,2] V is the half-scale input range ([–1,3] V would be the full-scale input range) and such that the op amp swing is 0.5 $V_{p,diff}$ at –6 dBFS.

Choose capacitor values such that the SNR with a –6 dBFS input should be ~90 dB when OSR = 256.

What You Learned Today

And what the homework should solidify

1 MOD2 implementation

2 Switched-capacitor integrator

SC summer & DAC too

3 Dynamic-range scaling

4 kT/C noise

5 Some MOD2 nonlinear theory

6 Verification strategy

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