ECE1371 Advanced Analog Circuits
Lecture 7

EXAMPLE DESIGN– PART 2

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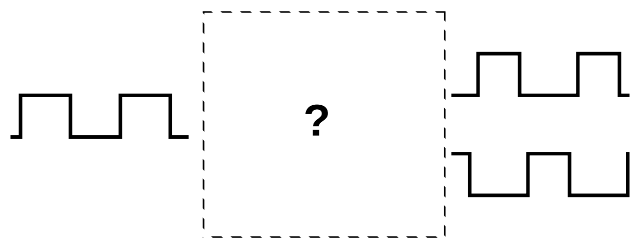
Course Goals

- **Deepen understanding of CMOS analog circuit design through a top-down study of a modern analog system— a delta-sigma ADC**
- **Develop circuit insight through brief peeks at some nifty little circuits**
  The circuit world is filled with many little gems that every competent designer ought to know.

Date			Lecture	Ref	Homework
2012-01-12	RS	1	Introduction: MOD1	ST 2, A	1: MOD1 in Matlab
2012-01-19	RS	2	MOD2 & MOD*N*	ST 3, 4, B	2: MOD2 in Matlab
2012-01-26	RS	3	Example Design: Part 1	ST 9.1, CCJM 14	3: Sw.-level MOD2
2012-02-02	TC	4	SC Circuits	R 12, CCJM 14	4: SC Integrator
2012-02-09	TC	5	Amplifier Design		
2012-02-16	TC	6	Amplifier Design		5: SC Int w/ Amp
2012-02-23	Reading Week + ISSCC– No Lecture				
2012-03-01	RS	7	Example Design: Part 2	CCJM 18	Start Project
2012-03-08	RS	8	Comparator & Flash ADC	CCJM 10	
2012-03-15	TC	9	Noise in SC Circuits	ST C	
2012-03-22	TC	10	Matching & MM-Shaping	ST 6.3-6.5, +	
2012-03-29	RS	11	Advanced $\Delta\Sigma$	ST 6.6, 9.4	
2012-04-05	TC	12	Pipeline and SAR ADCs	CCJM 15, 17	
2012-04-12	No Lecture				
2012-04-19	Project Presentation				

NLCOTD: Non-Overlapping Clock Generator

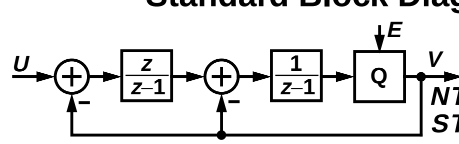
- **Our SC circuits require two non-overlapping clocks. How do we generate them?**



Highlights
(i.e. What you will learn today)

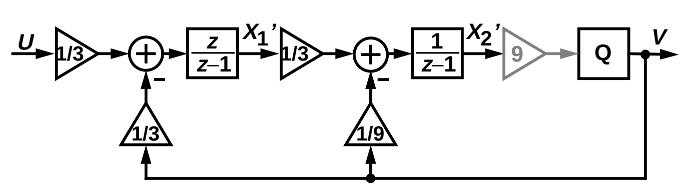
1. **Transistor-level implementation of MOD2**
   op-amp, SC CMFB, comparator, clock generator
2. **MOD2 variants**
3. **Variable quantizer gain**

Review: MOD2
Standard Block Diagram

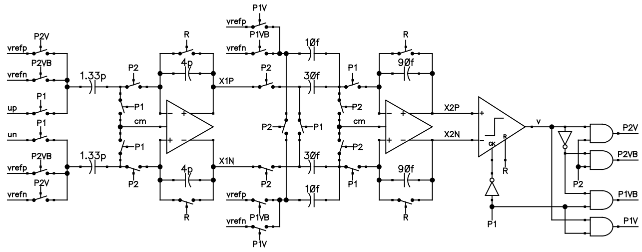


$$NTF(z) = (1 - z^{-1})^2$$
$$STF(z) = z^{-1}$$

Scaled Block Diagram

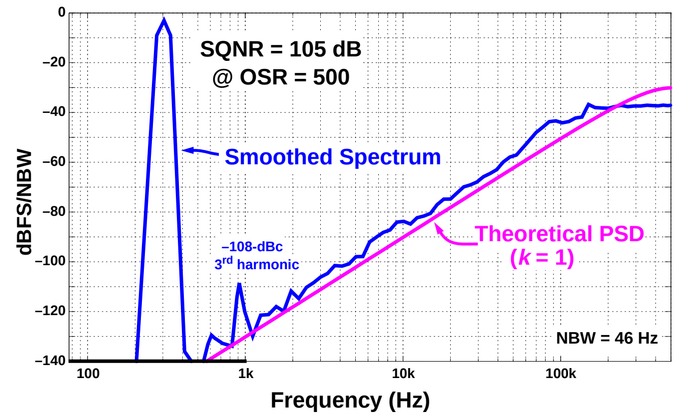


Review: Schematic



- 1^{st}-stage capacitor sizes set for SNR = 100 dB @ OSR = 500 and –3-dBFS input
  - V_{ref} = 1V and the full-scale input range is ±1 V.
- 2^{nd}-stage capacitor sizes set by minimum allowable capacitance

Review: Simulated Spectrum



Review: Implementation Summary

✓ 1 Choose a viable SC topology and manually verify timing

✓ 2 Do dynamic-range scaling
   - You now have a set of capacitor ratios.
   - Verify operation.

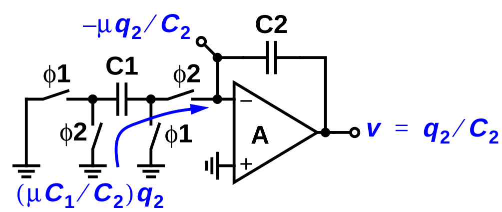
✓ 3 Determine absolute capacitor sizes
   - Verify noise.

➤➤ 4 Determine op-amp specs and construct a transistor-level schematic
   - Verify.

5 Layout, fab, debug, document, get customers, sell by the millions, go public, …

Effect of Finite Op Amp Gain
Linear Theory

- Suppose that the amplifier has finite DC gain A. Define $\mu = 1/A$.
- To determine the effect on the integrator pole, let's look at our SC integrator with zero input:



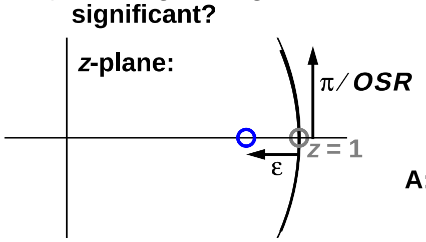
- A fraction of q_2 leaks away each clock cycle:

$$q_2(n+1) = (1-\varepsilon)q_2(n),$$

$$\text{where } \varepsilon = \mu C_1/C_2$$

- Thus, the integrator is lossy, with a pole at $z = 1-\varepsilon$

Q: How big can ε get before the effect becomes significant?



A: $\varepsilon \approx \pi/OSR$

Op Amp Gain Requirement
Linear Theory

- According to the linear theory, finite op amp gain should not degrade the noise significantly as long as

$$A > (C_1/C_2)(OSR/\pi)$$

- For our implementation of MOD2, in which $C_1/C_2 = 1/4$ and $OSR = 500$, this leads to

$$A > 40 = 32 \text{ dB},$$

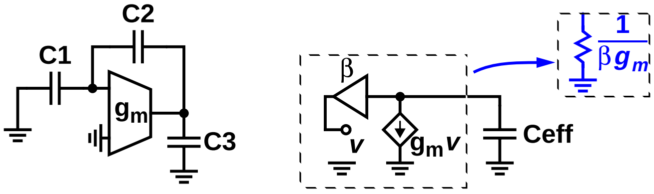
which is quite a lax requirement!

- As OSR is decreased, the gain requirement goes down

Op Amp Transconductance

Settling time

- Model the op amp as a simple g_m:



$$\beta = C_2/(C_1 + C_2)$$
$$C_{eff} = C_3 + C_1C_2/(C_1 + C_2)$$

- This is a single-time-constant-circuit with $\tau = C_{eff}/(\beta g_m)$

Settling Requirements

- If g_m is linear, incomplete settling has the same effect as a coefficient error and thus g_m can be very low
- In practice, the g_m is not linear and we need to ensure nearly complete settling
- As a worst case scenario, let's require transients to settle to 1 part in 10^5

  This should be more than enough for –100 dBc distortion.

Settling Requirements (cont'd)

- If linear settling is allocated 1/4 of a clock period, we want $\exp\left(-\frac{T/4}{\tau}\right) = 10^{-5}$, or $\tau = \frac{T}{4\ln 10^5} = 20$ ns

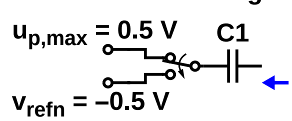
  and thus $g_m = \frac{C_{eff}}{\beta\tau} = \frac{C_{eff}}{\beta} 4 f_s \ln 10^5$
- For INT1 of our MOD2:

$$C_{eff} = 0.5\left(\frac{4\text{p} \cdot 1.33\text{p}}{4\text{p} + 1.33\text{p}} + 30\text{f}\right) = 0.5\ \text{pF}^{*}$$
$$\beta = 3/4$$
$$f_s = 1\ \text{MHz}$$
$$\Rightarrow\ g_m = 30\ \mu\text{A/V}$$

*. 0.5 comes from the single-ended to differential translation.

Slewing

- The maximum charge transferred through C1 is

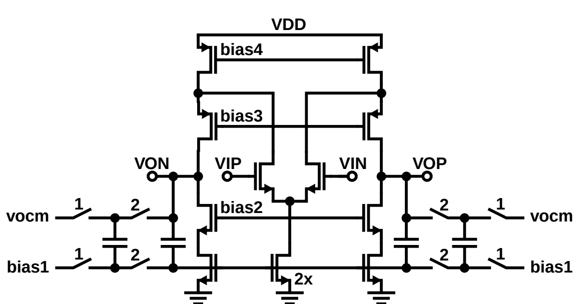


$$q_{max} = C_1 \cdot 1\text{V} = 1.33\ \text{pC}$$

- If we require the slew current to be enough to transfer q_{max} in 1/4 of a clock period, then

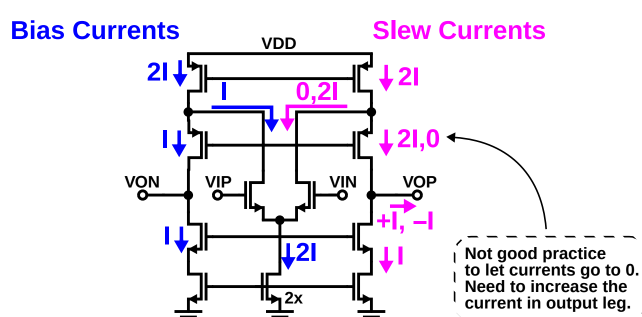
$$I_{slew} = \frac{q_{max}}{T/4} \approx 5\ \mu\text{A}$$

Building Block– Op Amp



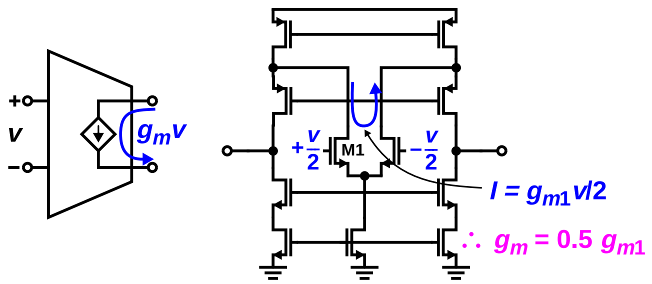
- Folded-cascode op-amp with switched-capacitor common-mode feedback

Op-Amp Design— Bias Current



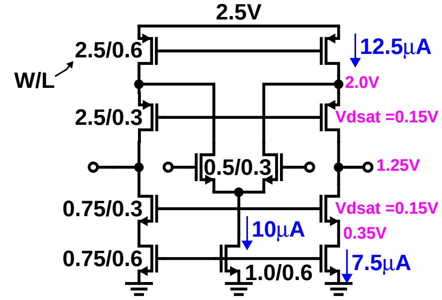
- Slew constraint dictates I >5 µA

Op-Amp Design— gm



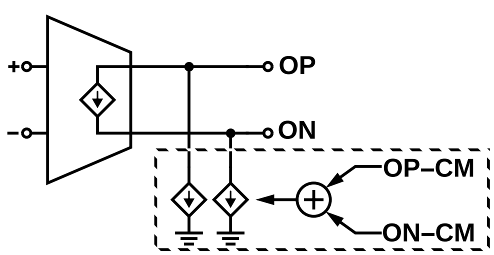
- Square-law MOSFET model: $g_{m1} = (2I_D)/(\Delta V)$
- $I_D = 5\ \mu A$, $g_m \geq 30\ \mu A/V \Rightarrow \Delta V \leq 0.33\ V$
  Usually $\Delta V \approx 200$ mV, so we should be able to get high enough g_m.

Transistor Sizes & Bias Point



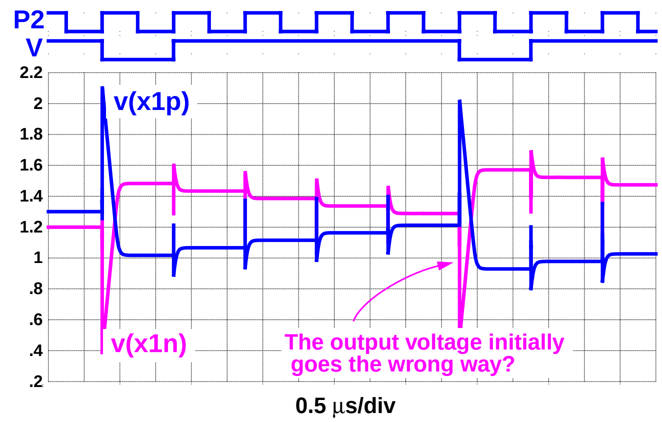
- Allowable swing is +0.6 V, –0.75 V
- Simulated g_m = 36 µA/V, A = 48 dB
  g_m is high enough and the gain is 6× required.

Ideal Common-Mode Feedback

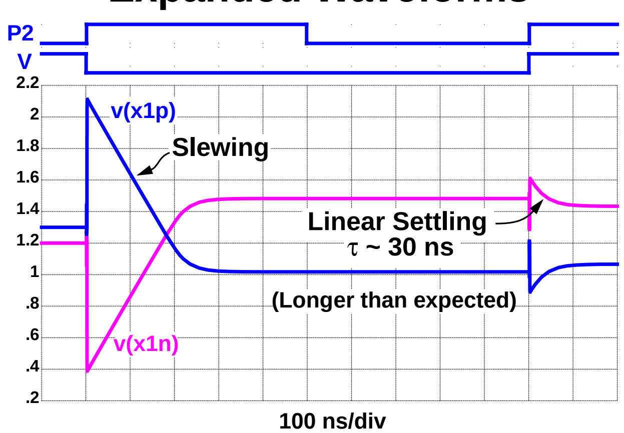


- Can use this circuit to speed up the simulation

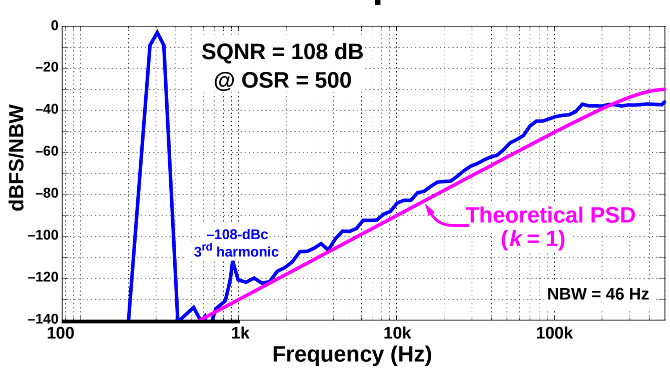
Simulated Waveforms



Expanded Waveforms



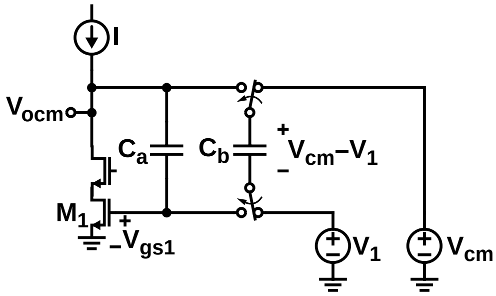
Simulated Spectrum



- This was too easy!
  Although this one simulation *did* take an hour.

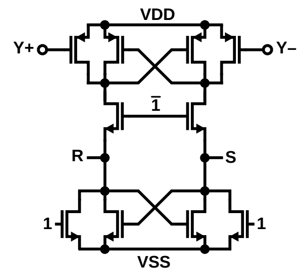
SC Common-Mode Feedback

Common-Mode 1/2-Circuit

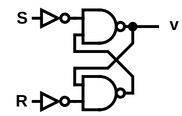


- $V_{ocm} = V_{cm} + V_{gs1} - V_1$
  If $V_1 = V_{gs1}$, then $V_{ocm} = V_{cm}$.

Latched Comparator



Set/Reset Latch:

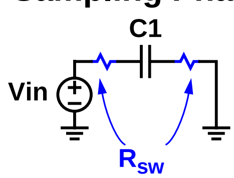


Inverter thresholds are chosen so that the inverters respond only after R/S have resolved.

- **Falling phase 1 initiates regenerative action**
  S and R connected to a Set/Reset latch.

Switch Resistance

Sampling Phase



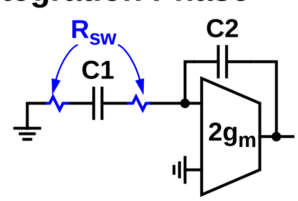
- If R_{SW} is constant, its has only a filtering (linear) effect, which is benign
- Unfortunately, the on-resistance of MOS switches varies with V_{gs} (and hence V_{in})

⇒ Must make MOS switches large enough

Switch Resistance

Integration Phase

Differential Half-Circuit:

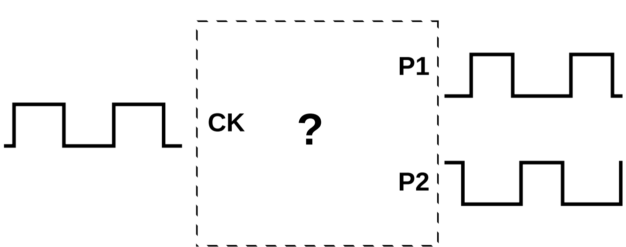


- R_{sw} increases the settling time by a factor of $1 + 4g_m R_{sw}$

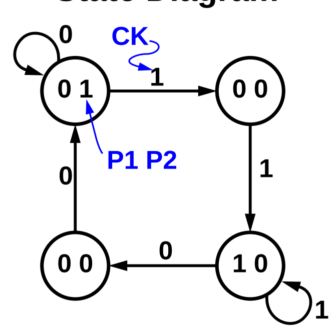
⇒ Set $R_{sw} \leq \dfrac{1}{40 g_m}$ to make the increase in τ small

- So in our MOD2, we want $R_{sw} \leq 0.75$ kΩ.
  BTW, my simulation used R_{sw} = 1 kΩ and was OK.

NLCOTD: Non-Overlapping Clock Generator



State Diagram



Truth Table

CK	P1	P2	P1’	P2’
0	0	1	0	1
1	0	1	0	0
1	0	0	1	0
1	1	0	1	0
0	1	0	0	0
0	0	0	0	1

Karnaugh Maps

P1':

CK \ P1P2	00	01	11	10
0	0	0	X	0
1	1	0	X	1

$P1' = CK \cdot \overline{P2}$

$= \overline{\overline{CK}+P2}$

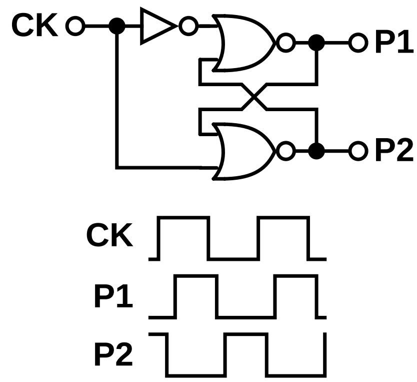
P2':

CK \ P1P2	00	01	11	10
0	1	1	X	0
1	0	0	X	0

$P2' = \overline{CK} \cdot \overline{P1}$

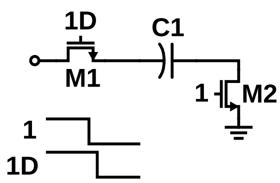
$= \overline{CK+P1}$

Non-Overlapping Clock Generator



- Non-overlap time set by NOR's t_{PLH}

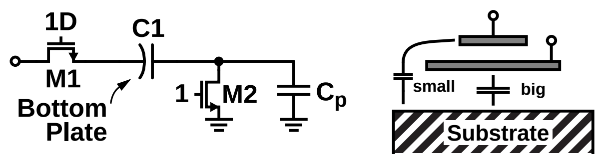
Clocking Details— Early/Late Phases



- Charge injected via M1 is (non-linearly) signal-dependent, whereas charge injection from M2 is signal-independent

⇒ Open M2 (early) then open M1 (late) so that charge injected from C_{gs1} cannot enter C1

Clocking Details— Bottom-plate sampling



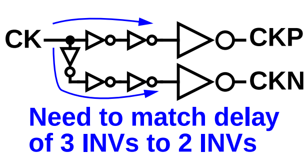
- Parasitic capacitance on the right terminal of C1 degrades the effectiveness of early/late clocking
- C_p for the top plate is smaller, so use the top plate for the right terminal and the bottom plate for the left

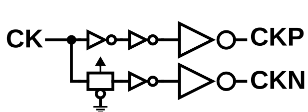
Complementary Clock Alignment

- We need complementary clocks if transmission gates are used for the switches

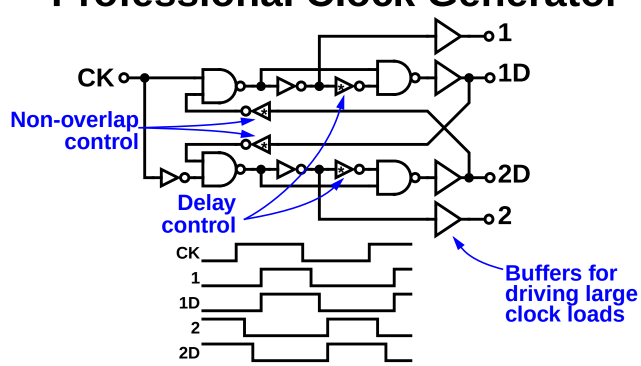
Q: How do we align them?

A: Carefully size the inverters relative to their capacitive loads, or use a transmission gate to mimic an inverter delay:





Professional Clock Generator

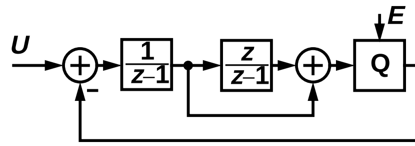


- To maximize the time available for settling, make the early and late phases start at the same time

Review: Implementation Summary

- ✓ 1 **Choose a viable SC topology and manually verify timing**
- ✓ 2 **Do dynamic-range scaling**
- ✓ 3 **Determine absolute capacitor sizes**
- ✓ 4 **Determine op-amp specs and construct a transistor-level schematic**
  - **Verify. Verify. Verify.**
- 5 **Layout, fab, debug, document, get customers, sell by the millions, go public, …**
  - **This last step is an "exercise for the reader."**

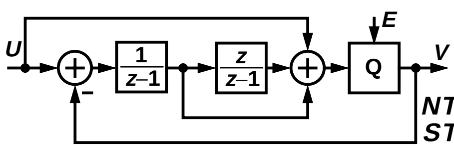
Topological Variant– Feed-Forward



$NTF(z) = (1 - z^{-1})^2$
$STF(z) = 2z^{-1} - z^{-2}$

- \+ **Output of first integrator has no DC component**
  - **Dynamic range requirements of this integrator are relaxed.**
- – **Although $|STF| \approx 1$ near $\omega = 0$, $|STF| = 3$ for $\omega = \pi$**
  - **Instability is more likely.**

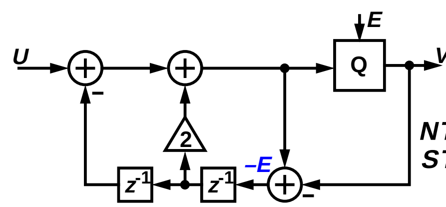
Topological Variant– Feed-Forward with Extra Feed-In



$NTF(z) = (1 - z^{-1})^2$
$STF(z) = 1$

- \+ **No DC component in either integrator's output**
  - **Reduced dynamic range requirements in both integrators, esp. for multi-bit modulators.**
- \+ **Perfectly flat STF**
  - **No increased risk of instability.**
- – **Timing is tricky**

Topological Variant– Error Feedback



$NTF(z) = (1 - z^{-1})^2$
$STF(z) = 1$

- \+ **Simple**
- – **Very sensitive to gain errors**
  - **Only suitable for digital implementations.**

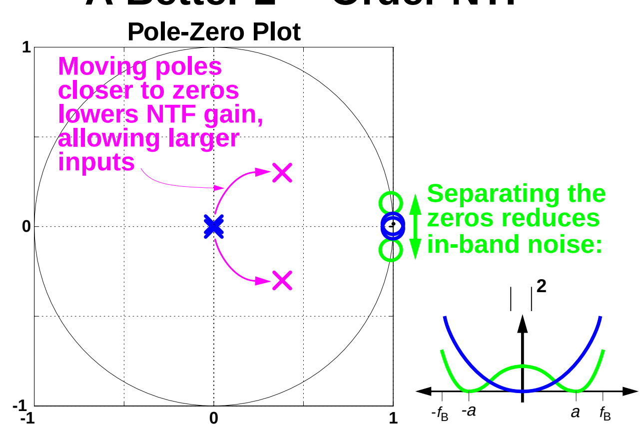
Is MOD2 The Only 2^{nd}-Order Modulator?

- **Except for the filtering provided by the STF, any modulator with the same NTF as MOD2 has the same input-output behavior as MOD2**
  - **SQNR curve is the same.**
  - **Tonality of the quantization noise is unchanged.**
- **Internal states, sensitivity, thermal noise etc. can differ from realization to realization**

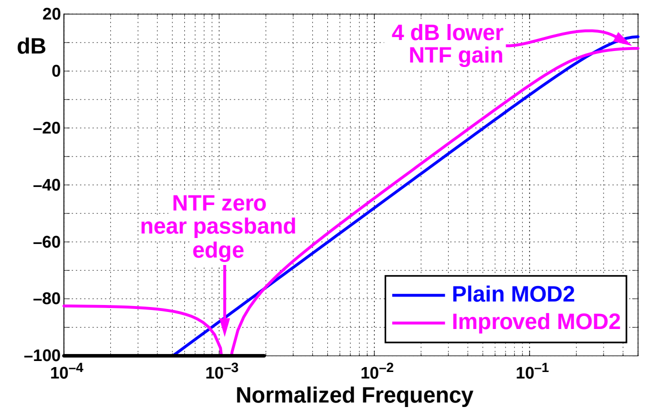
BUT, in terms of input-output behavior,

- **A 2^{nd}-order modulator is truly different only if it possesses a truly different (2^{nd}-order) NTF**

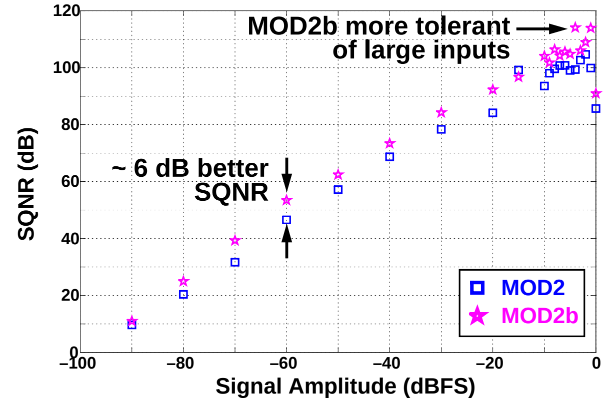
A Better 2^{nd}-Order NTF



NTF Comparison

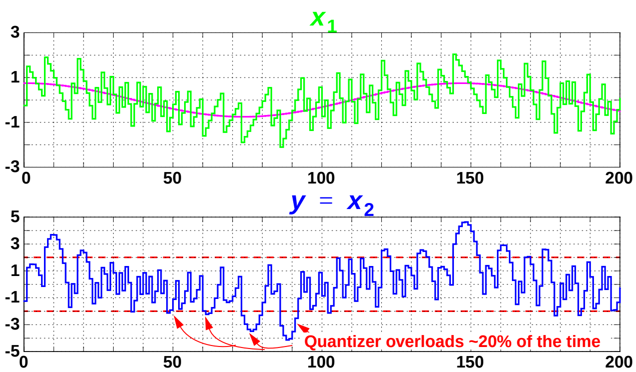


SNR vs. Amp Comparison



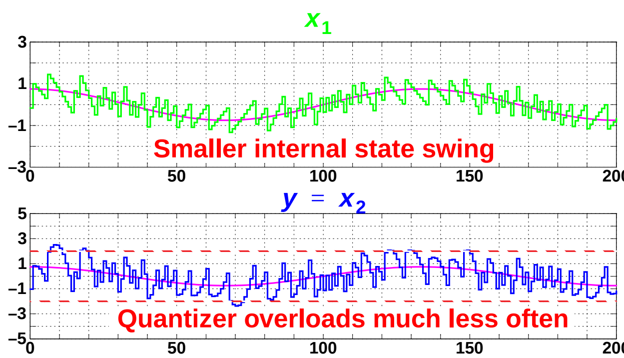
MOD2 Internal Waveforms

Input @ 75% of FS

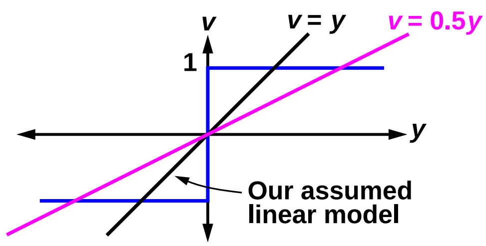


MOD2b Internal Waveforms

Input @ 75% of FS



Gain of a Binary Quantizer



- The effective gain of a binary quantizer is not known a priori
- The gain (k) depends on the statistics of the quantizer's input

  Halving the signal doubles the gain.

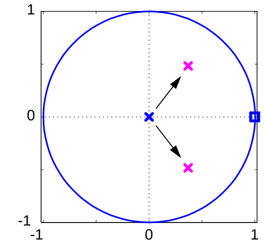
Gain of the Quantizer in MOD2

- The effective gain of a binary quantizer can be computed from the simulation data using

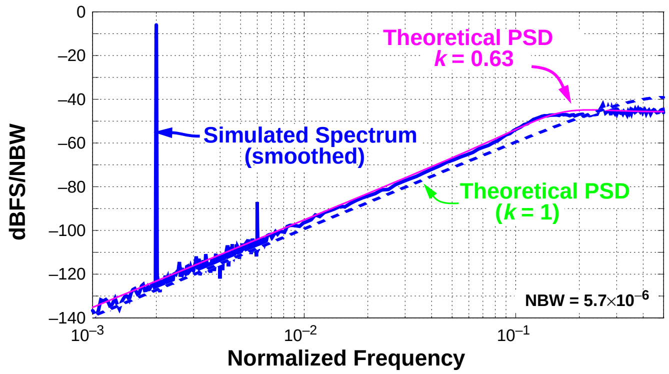
$$k = \frac{E[|y|]}{E[y^2]} \text{ [S\&T Eq. 2.5]}$$

- For the simulation of 2-14, $k = 0.63$
- $k \neq 1$ alters the NTF:

$$NTF_k(z) = \frac{NTF_1(z)}{k + (1-k)NTF_1(z)}$$



Revised PSD Prediction



- Agreement is now excellent

Variable Quantizer Gain

- When the input is small (below –12 dBFS), the effective gain of MOD2's quantizer is $k = 0.75$
- MOD2's "small-signal NTF" is thus

$$NTF(z) = \frac{(z-1)^2}{z^2 - 0.5z + 0.25}$$

- This NTF has 2.5 dB less quantization noise suppression than the $(1 - z^{-1})^2$ NTF derived from the assumption that $k = 1$

  Thus the SQNR should be about 2.5 dB lower than ⚹.

- As the input signal increases, k decreases and the suppression of quantization noise degrades

  SQNR increases less quickly than the signal power. Eventually the SQNR saturates and then decreases as the signal power reaches full-scale.

What You Learned Today

1. Transistor-level implementation of MOD2

   op-amp, SC CMFB, comparator, clock generator

2. MOD2 variants
3. Variable quantizer gain

Op Amp Gain Requirement

Nonlinear Theory 1

- MOD2 has a "deadband" around $u = 0$ whose width is approximately

$$\frac{0.5(a_1 c_1) + a_2}{A^2} = \frac{0.5((1/3)\cdot(1/3)) + (1/9)}{A^2} = \frac{1}{6A^2}$$

- To make the deadband less than 1 "LSB" wide,

$$\frac{1}{6A^2} < \text{undbv}(-100) = 10^{-5},$$

$$\text{or } A > 400 = 52 \text{ dB}$$

- Since we didn't need so much gain to get excellent AC performance, this calculation looks like it is conservative

Op Amp Gain Requirements

Nonlinear Theory 2

- Finite DC gain ⇒ incomplete charge transfer
- The gain is a nonlinear function, so the residual charge is nonlinearly related to the output voltage of the amplifier

  The residual charge is akin to noise.

- However, if the amplifier output contains signal components, then nonlinear gain can result in harmonic distortion

  The feedforward topology is known to yield low distortion even when the amplifier gain is low.

- The effects are difficult to quantify analytically, and so we typically rely on simulations