

ECE1371 Advanced Analog Circuits

Lecture 8

COMPARATOR & FLASH ADC DESIGN

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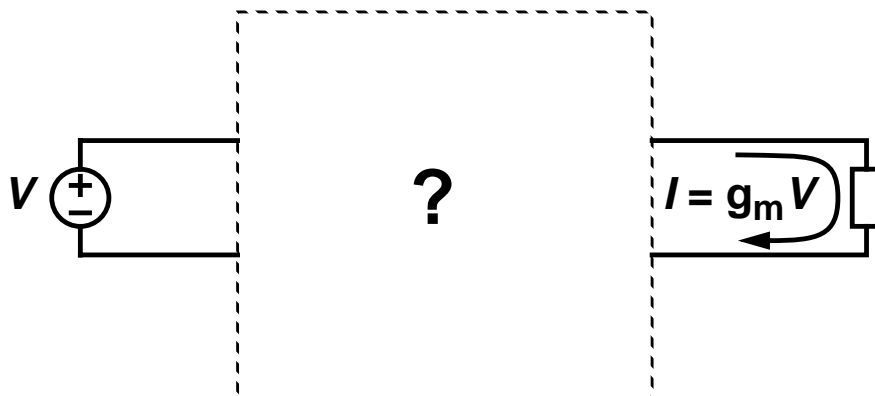
Course Goals

- **Deepen understanding of CMOS analog circuit design through a top-down study of a modern analog system— a delta-sigma ADC**
- **Develop circuit insight through brief peeks at some nifty little circuits**

The circuit world is filled with many little gems that every competent designer ought to know.

Date	Lecture			Ref	Homework
2012-01-12	RS	1	Introduction: MOD1	ST 2, A	1: MOD1 in Matlab
2012-01-19	RS	2	MOD2 & MODN	ST 3, 4, B	2: MOD2 in Matlab
2012-01-26	RS	3	Example Design: Part 1	ST 9.1, CCJM 14	3: Sw.-level MOD2
2012-02-02	TC	4	SC Circuits	R 12, CCJM 14	4: SC Integrator
2012-02-09	TC	5	Amplifier Design		
2012-02-16	TC	6	Amplifier Design		5: SC Int w/ Amp
2012-02-23	Reading Week + ISSCC– No Lecture				
2012-03-01	RS	7	Example Design: Part 2	CCJM 18	Start Project
2012-03-08	RS	8	Comparator & Flash ADC	CCJM 10	
2012-03-15	TC	9	Noise in SC Circuits	ST C	
2012-03-22	TC	10	Matching & MM-Shaping	ST 6.3-6.5, +	
2012-03-29	RS	11	Advanced $\Delta\Sigma$	ST 6.6, 9.4	
2012-04-05	TC	12	Pipeline and SAR ADCs	CCJM 15, 17	
2012-04-12	No Lecture				
2012-04-19	Project Presentation				

NLCOTD: Linear Transconductor



- Useful in
 - 1 gm-C filter
 - 2 LNA
 - 3 mixer
 - 4 CT $\Delta\Sigma$ ADC

Highlights

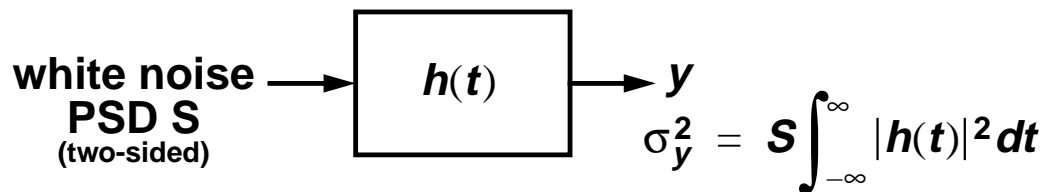
(i.e. What you will learn today)

- 1 Operation of Example Comparator Circuit
- 2 Regeneration Time Constant
- 3 Metastability, Probability of Error
- 4 Dynamic Offset
- 5 Other Comparator Circuits
- 6 A Bunch of Transconductor Circuits

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Background: Filtered White Noise



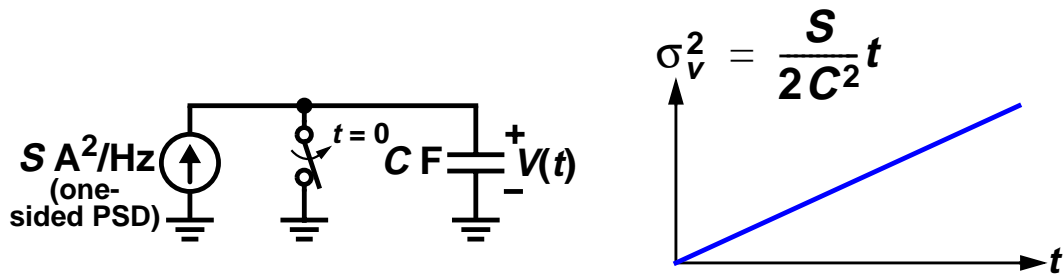
- The power of the output is the product of the PSD and the power gain of the filter
- Example: $h(t) = \begin{cases} 1 & 0 \leq t \leq T \\ 0 & \text{otherwise} \end{cases}$

$$\Rightarrow \sigma_y^2 = ST$$

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Circuits Application: Integrated White Noise



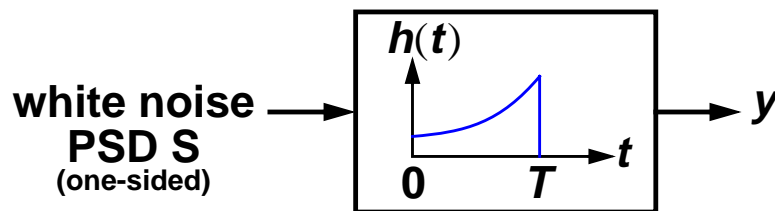
- Variance of V increases linearly with time
- “Random Walk” or “Brownian Motion”
For any given increment of time Δt , the change in V is a random variable with constant variance

$$\delta(t) \equiv V(t) - V(t - \Delta t) \Rightarrow \sigma_{\delta}^2 = \text{constant}$$

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Today's Application



$$h(t) = \begin{cases} e^{t/\tau} & 0 \leq t \leq T \\ 0 & \text{otherwise} \end{cases}$$

$$\sigma_y^2 = \frac{S\tau}{4} \left(e^{\frac{2T}{\tau}} - 1 \right)$$

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Background: PDF of a Sum

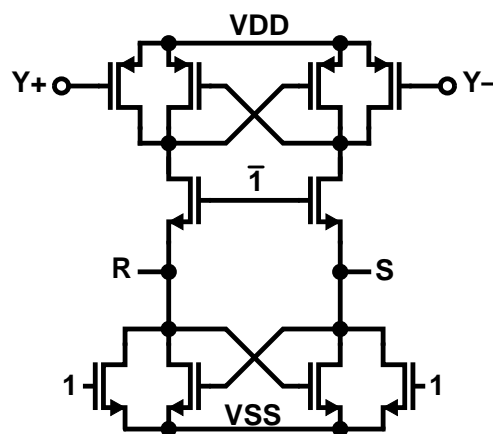
- Suppose x and y are two independent random variables with probability density functions (PDFs) $\rho_x(x)$ and $\rho_y(y)$
- Then the PDF of their sum is the convolution of the individual PDFs

$$z = x + y \Rightarrow \rho_z(z) = \int_{-\infty}^{\infty} \rho_x(x) \rho_y(z - x) dx$$

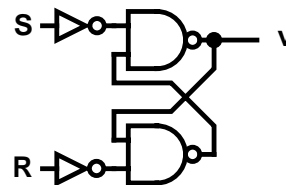
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Review: Latched Comparator From Lecture #7's 1-MHz MOD2



Set/Reset Latch:



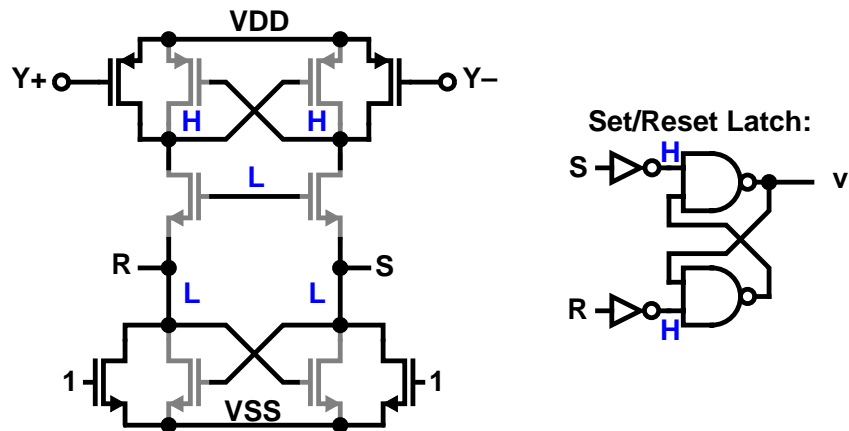
Inverter thresholds are chosen so that the inverters respond only after R/S have resolved.

- Falling phase 1 initiates regenerative action
S and R connected to a Set/Reset latch.

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Phase 1 = High: “Reset” Mode

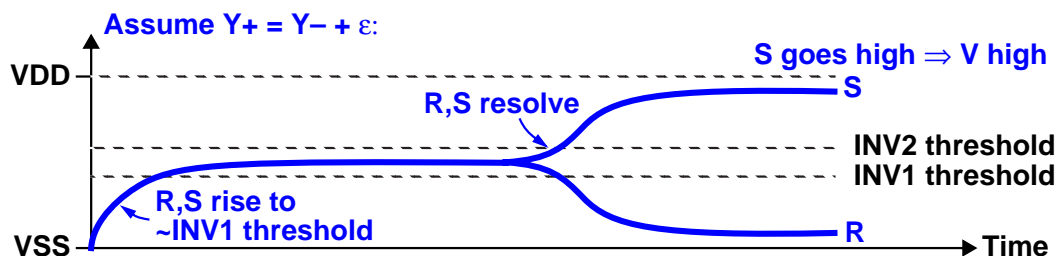
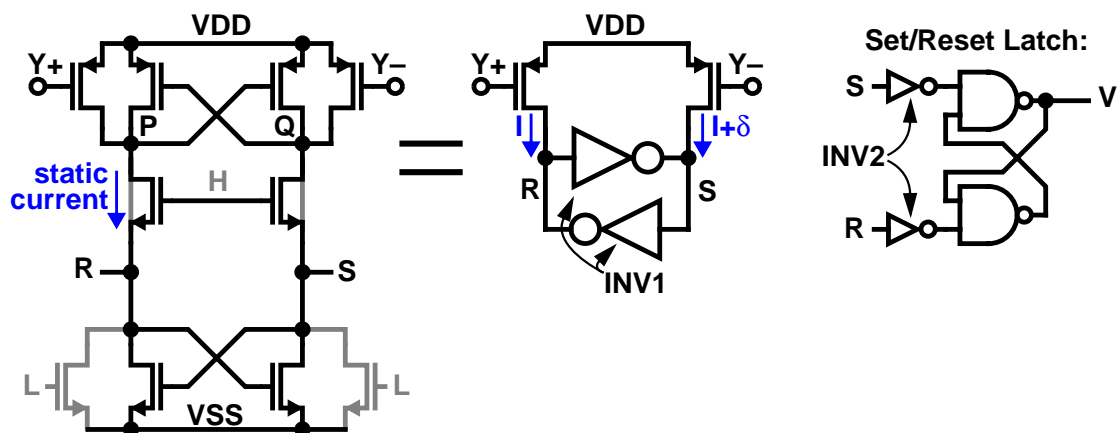


- Grayed-out devices are off
⇒ the active part of the comparator is reset
- R and S are low ⇒ the SR latch is in hold mode

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Phase 1 Goes Low: “Latch” Mode

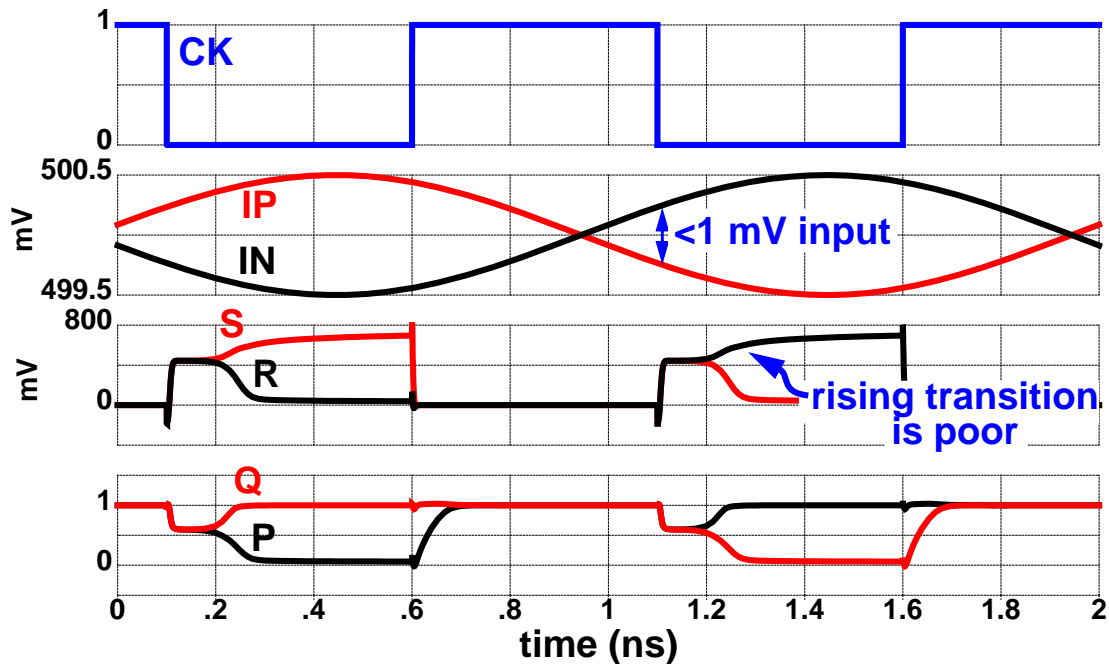


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Example Waveforms

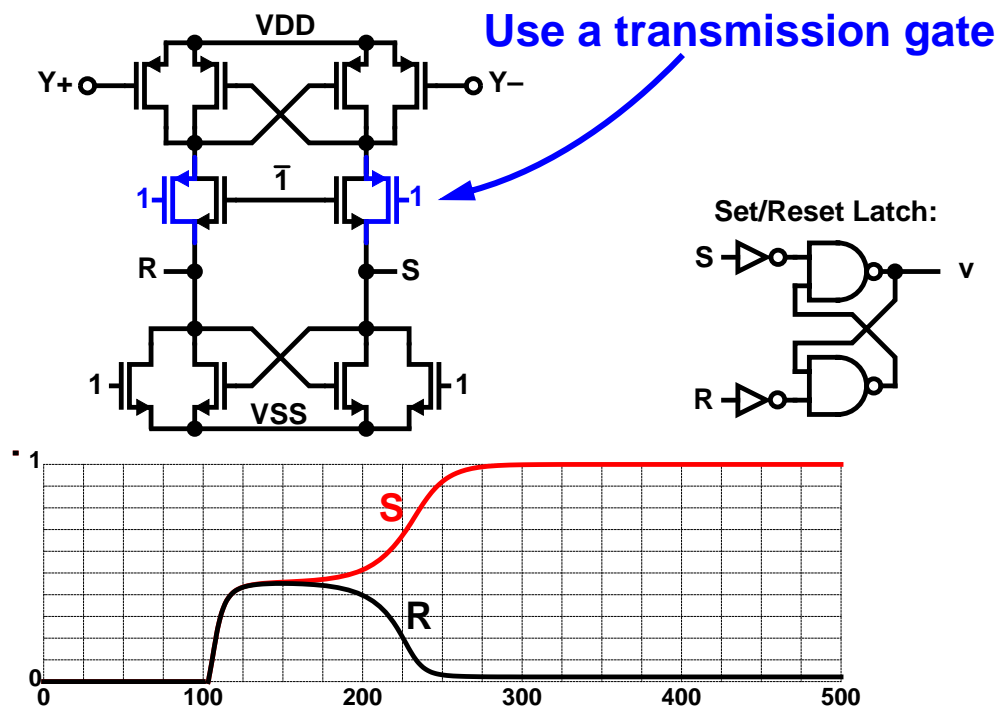
Quick Design in 65nm (VDD = 1V)



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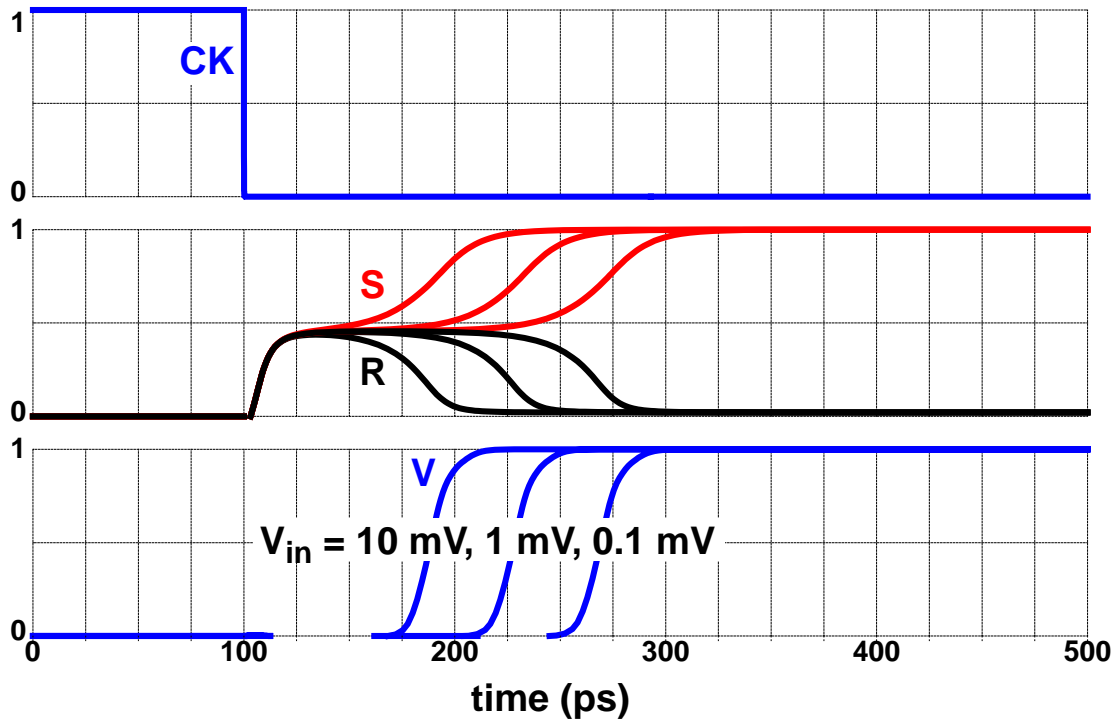
Better Design



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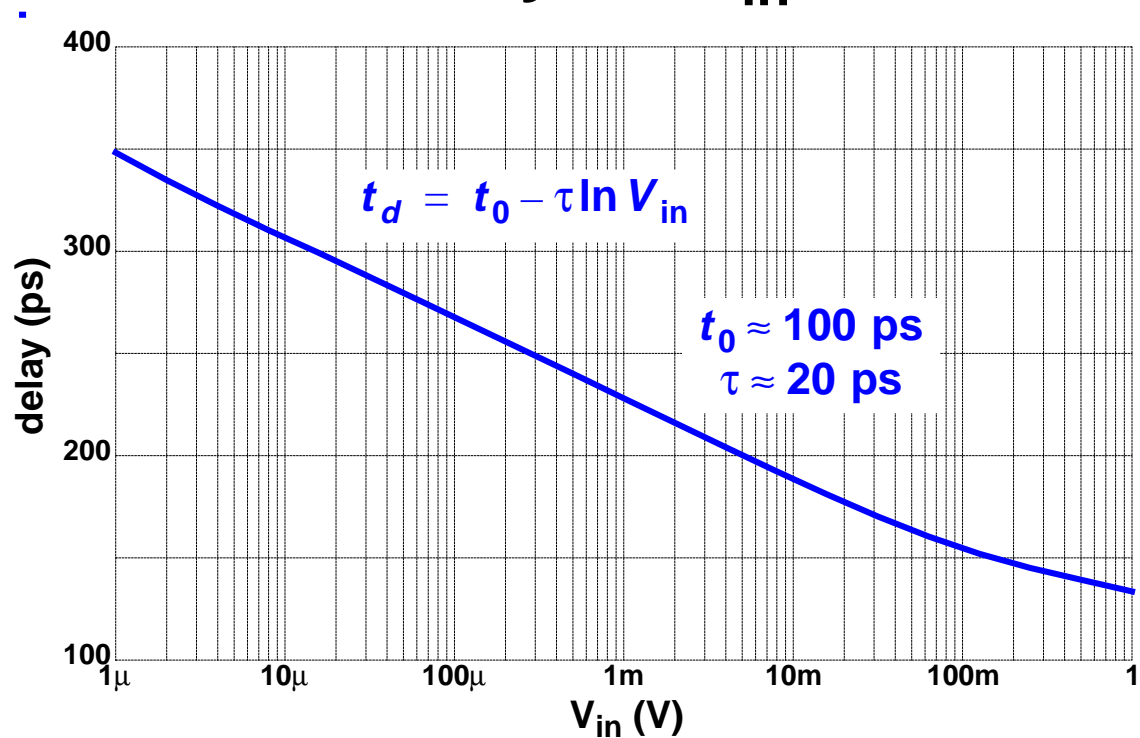
Responses for Various V_{in}



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Delay vs. V_{in}



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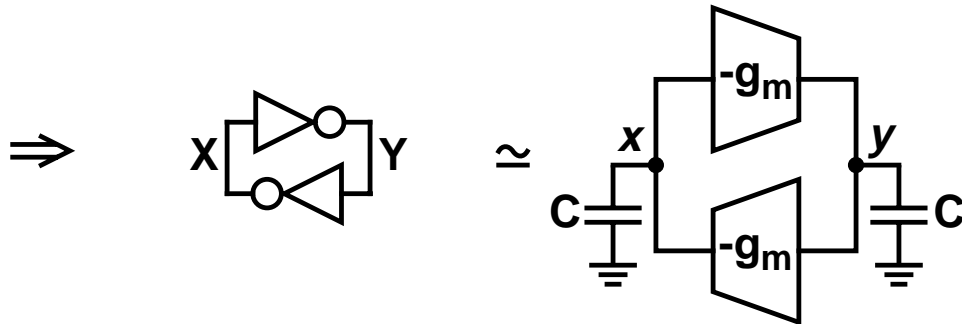
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Latch Mode Dynamics

- For V_{in} near the trip point, an inverter is essentially just a transconductor:



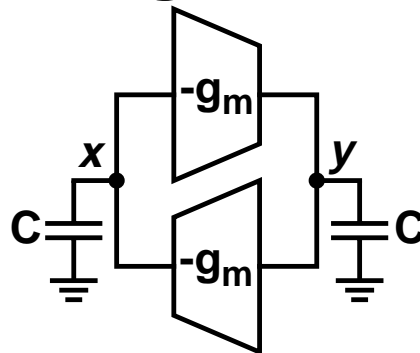
- So near balance the comparator looks like this:



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Small-Signal Analysis



$$C\dot{x} = -g_m y$$

$$C\dot{y} = -g_m x$$

$$v_d = x - y$$

$$v_{cm} = \frac{x + y}{2}$$

$$C\dot{v}_d = g_m v_d$$

$$v_d(t) = v_{d0} e^{t/\tau}$$

$$C\dot{v}_{cm} = -g_m v_{cm}$$

$$v_{cm}(t) = v_{cm0} e^{-t/\tau}$$

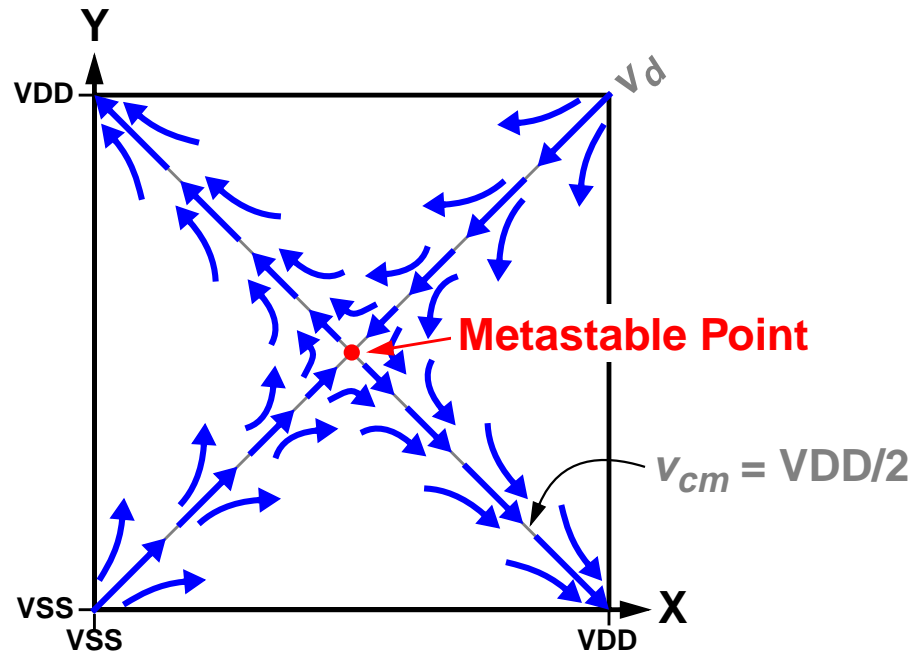
$$\tau = \frac{C}{g_m}$$

- Differential component grows exponentially
- CM component decays exponentially

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State-Space



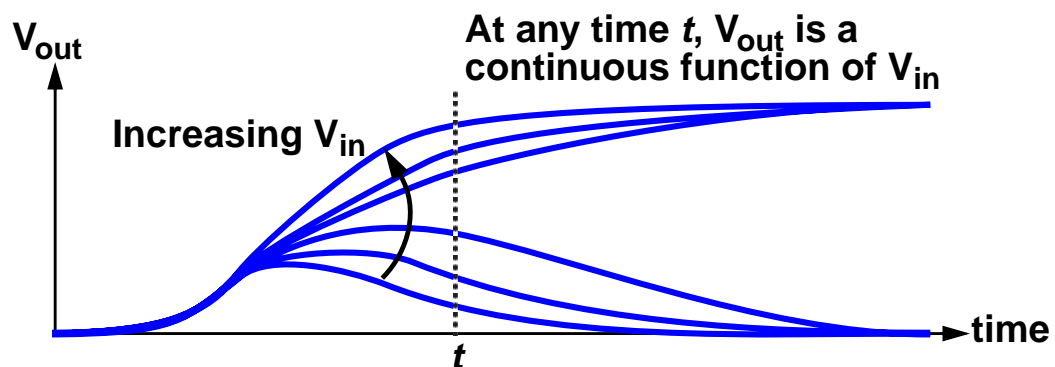
- $v_{cm} \rightarrow VDD/2, v_d \rightarrow \pm VDD$

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Metastability

- Metastability is fundamentally unavoidable
- Assuming the universe is continuous and deterministic, a comparator can be unresolved for any length of time



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Probability of Error, P_E

$$P_E = P\{\text{not resolved by time } t\}$$
$$= P\left\{V_{in} < \exp\left(-\frac{t-t_0}{\tau}\right)\right\}$$

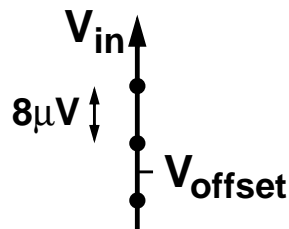
- Take $t_0 = 100$ ps and $\tau = 20$ ps
- Then for $t = 500$ ps (1 GHz clock with a half-cycle between the comparator's clock and the clock of the subsequent latch),

$$P_E = P\{|V_{in}| < 2 \text{ nV}\}$$

- Assuming V_{in} is uniformly distributed in $[-0.5, +0.5]$ V, $P_E = 2 \times 10^{-9}$
Metastability occurs twice a second!

Quantized Charge Helps?

- If $C = 20$ fF, then 1 electron yields $8 \mu\text{V}$
- $V_{in} = 2$ nV and hence metastability impossible?



- + Unless V_{offset} is within 2 nV of one of the discrete V_{in} levels, metastability can't happen
- But if V_{offset} is within 2 nV of an allowed V_{in} level, metastability will be abnormally frequent
- Offset drift will tend to make metastability appear/disappear sporadically (?)

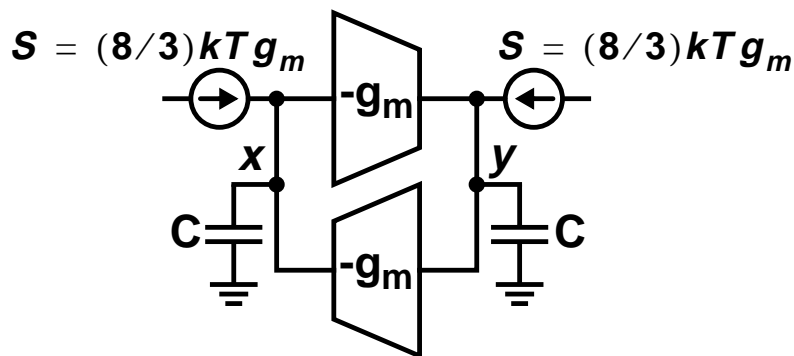
Noise Helps?

- $kT/C = 500 \mu\text{V}$, so it is impossible to guarantee that metastability will result even if $V_{\text{in}} = 0$
- + Noise does help a comparator resolve if it is metastable
- But for any given noise (random initial condition), there is always an input which results in metastability
- Noise makes it hard to set initial conditions that will result in metastability, but does not reduce the probability of error

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What About Noise During Regeneration?

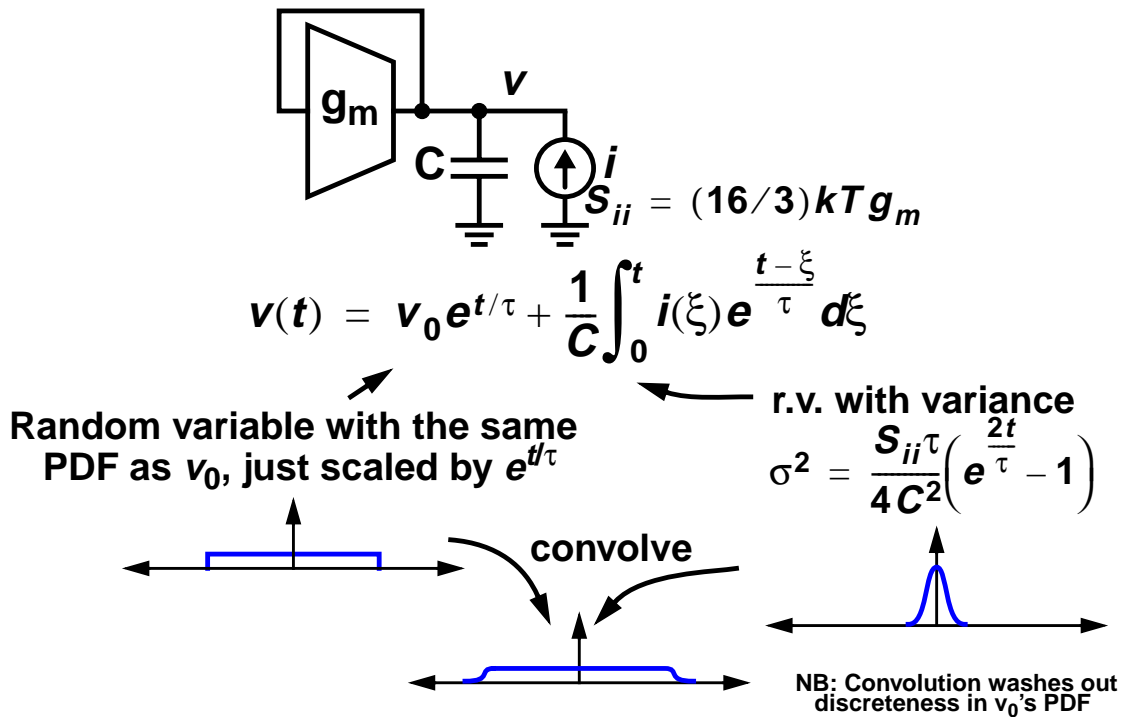


- Noise from the g_m s prevents metastability?

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Differential Circuit



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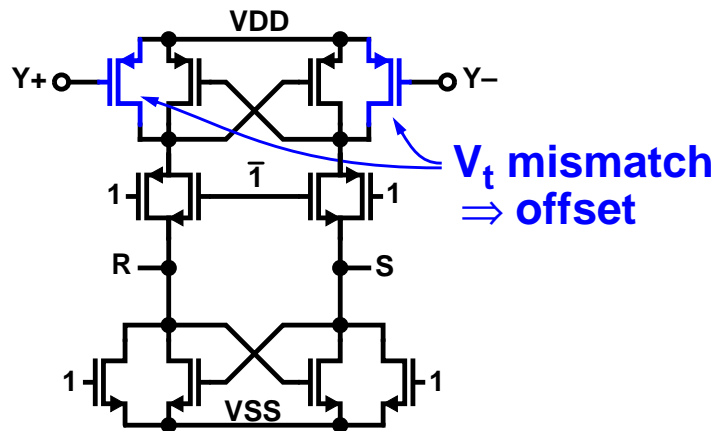
Let's "Make Numbers"

- Assume $g_m = 1 \text{ mA/V}$, $C = 20 \text{ fF}$, $t = 400 \text{ ps}$
 $\Rightarrow \tau = 20 \text{ ps}$; 20τ to resolve
- If v_0 uniformly distributed in $[-2, +2] \text{ mV}$,
 then 1st term is uniformly distributed in $[-1, +1] \text{ MV}$
- Standard deviation of 2nd term is 250 kV
 Equivalent to a 0.5-mV initial condition
- Noise during regeneration helps when the input is known to be small, but is usually negligible compared to the exponential growth of the initial conditions

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Offset

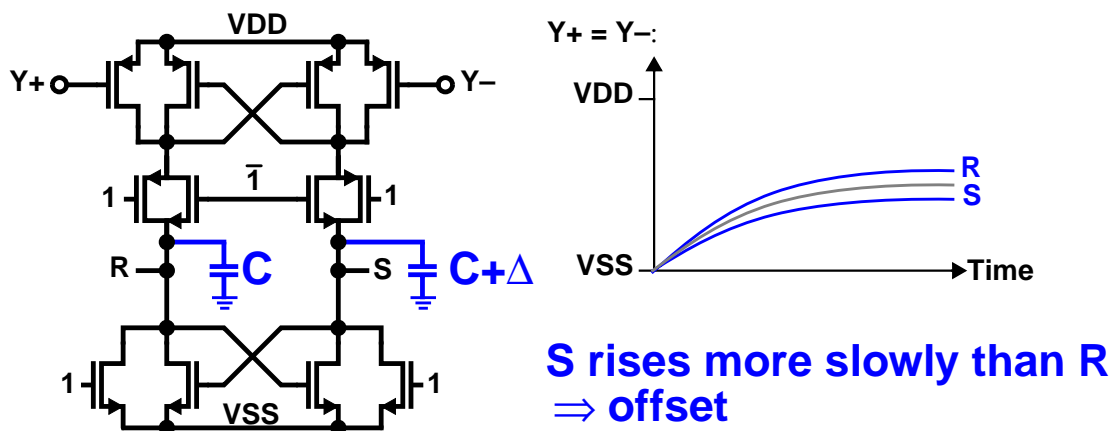


- Obvious sources of offset include mismatch in the input differential pair as well as mismatch in the regenerating devices

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Dynamic Offset



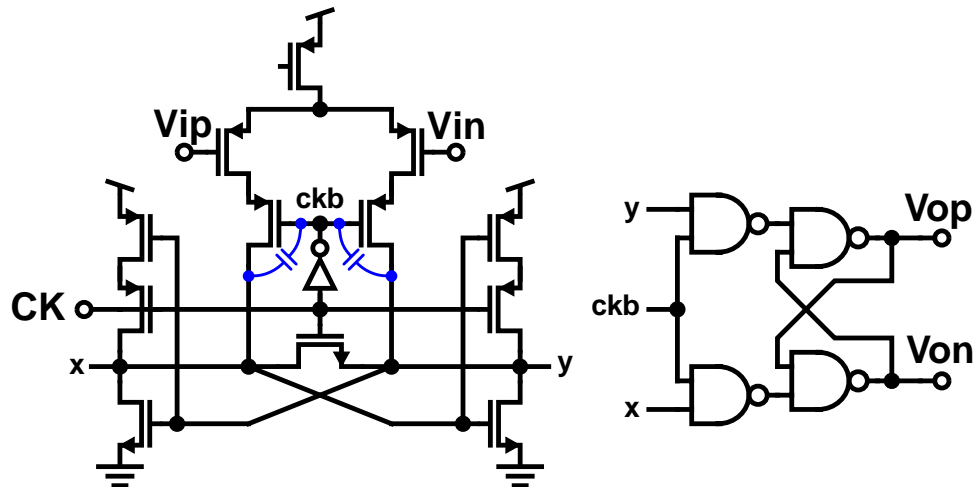
- Mismatched parasitic capacitance also causes offset
20 mV/fF for this comparator!
- Bad design– Can fix this!

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Improved Comparator

[S&T Fig. 9.36]

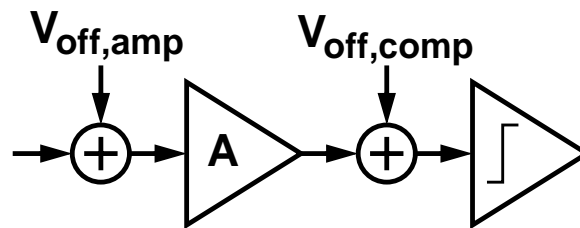


- Reset when $CK = 1$; regenerates when $CK = 0$
- x & y don't step if biased properly
Mismatch in overlap capacitance still a problem.

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Reducing Offset with a Preamp



$$V_{off,tot} = V_{off,amp} + V_{off,comp}/A$$

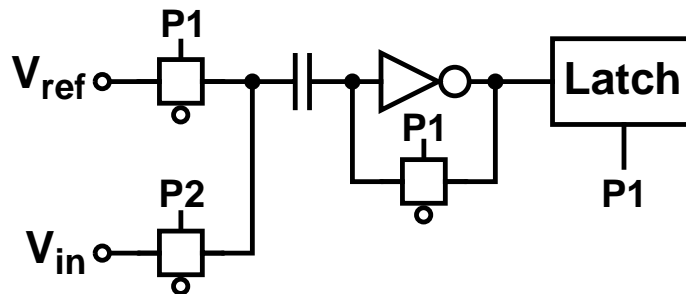
- + Comparator offset is reduced by preamp gain
Amplifier offset dominates.
- + Amplifier also isolates driving stage from
“charge kickback”
- Amplifier bandwidth limits speed, especially
recovery from overload

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Auto-zeroed SC Comparator

[J&M Fig 13.17]



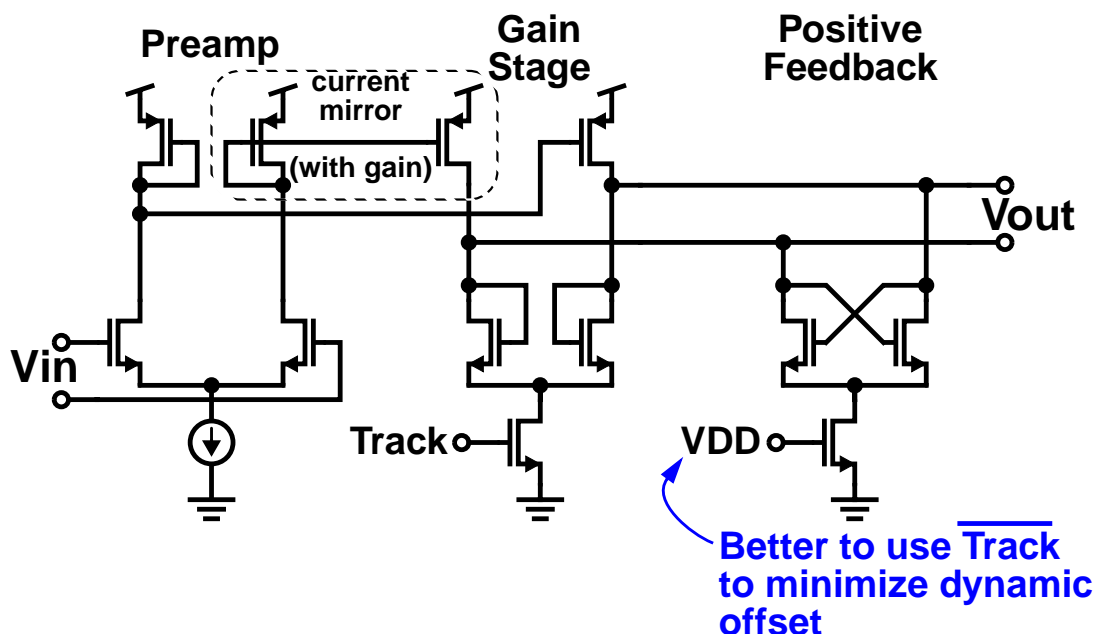
- During P1, the inverter/amplifier is biased at its threshold/offset voltage
- During P2, the difference between V_{in} and V_{ref} is amplified

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Comparator with Preamp

[J&M Fig. 7.16]

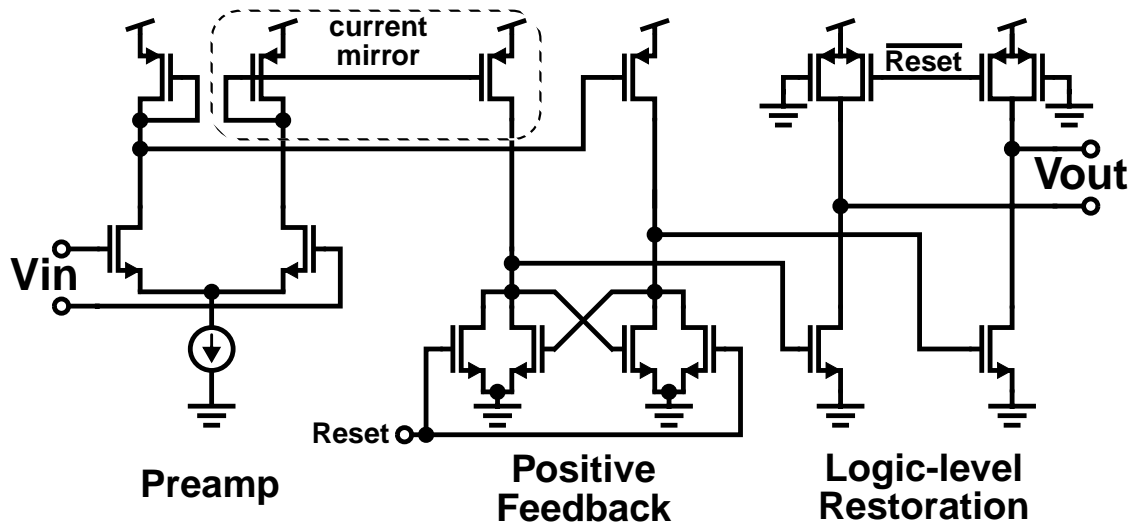


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Two-Stage Comparator

[J&M Fig 7.17]

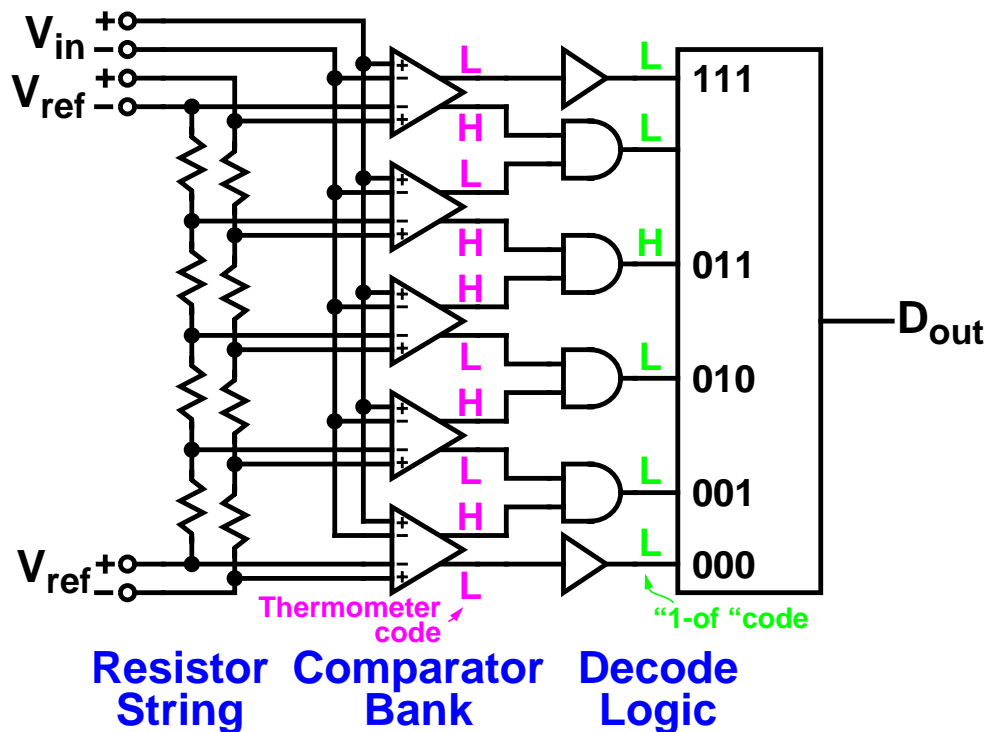


- Precharges regeneration nodes low & digital output nodes high

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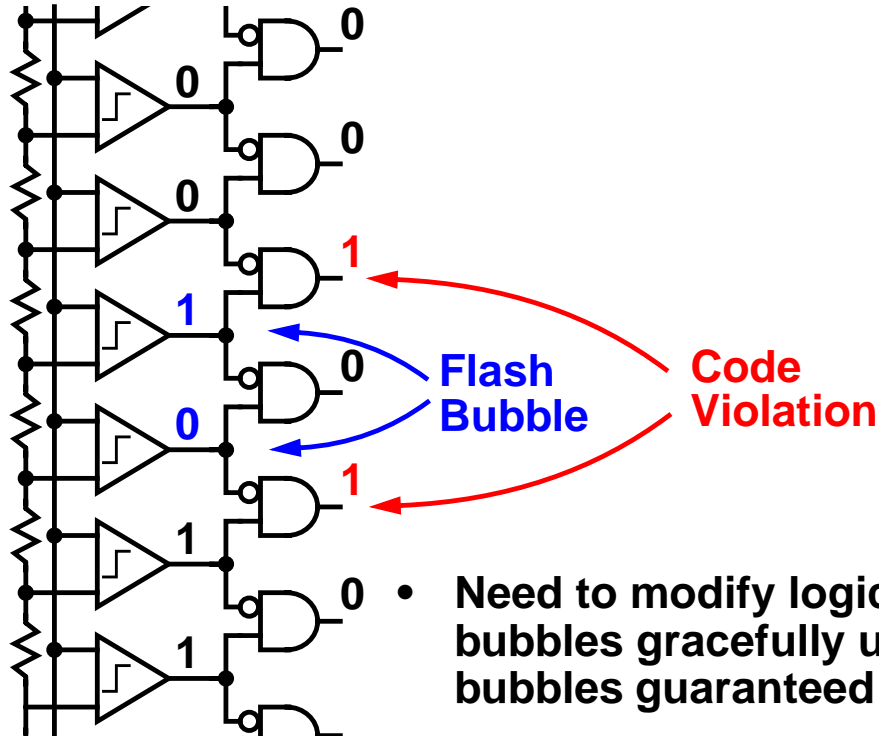
Flash ADC



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Flash Bubbles

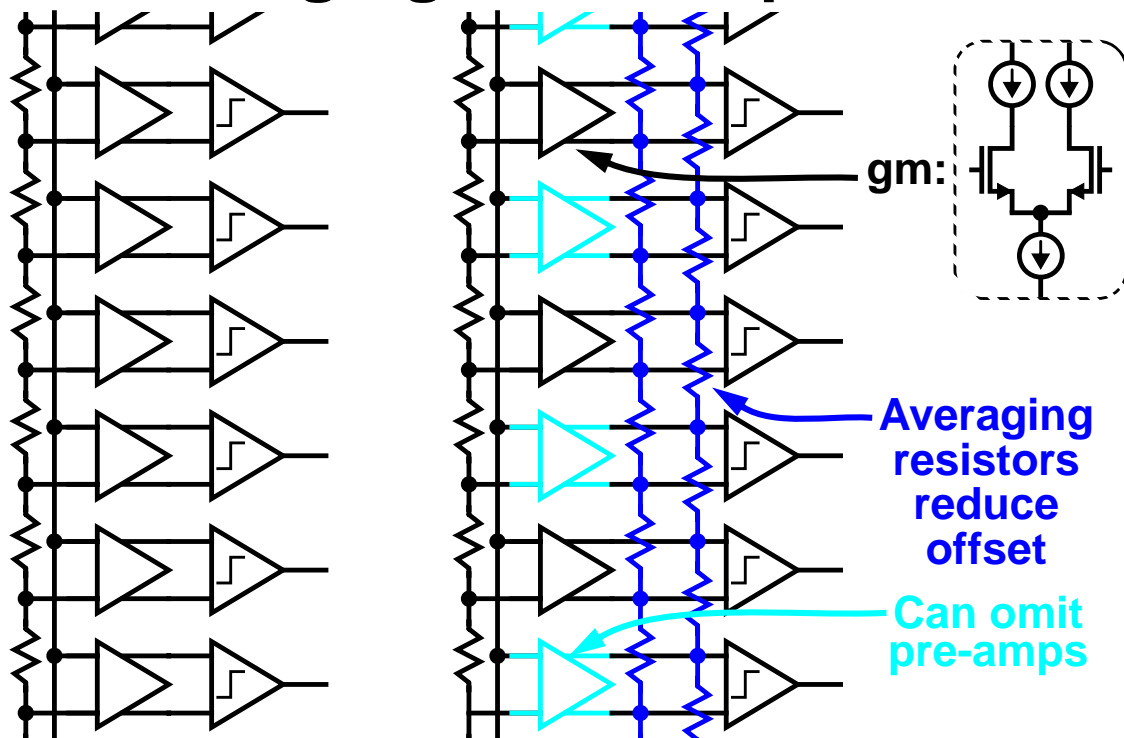


- Need to modify logic to handle bubbles gracefully unless bubbles guaranteed to not occur

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Averaging and Interpolation

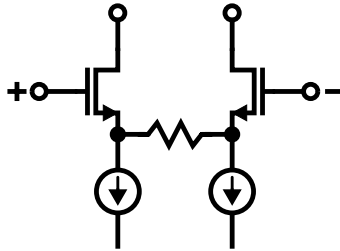


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NLCOTD: Linear Transconductors

Degenerated Differential Pair

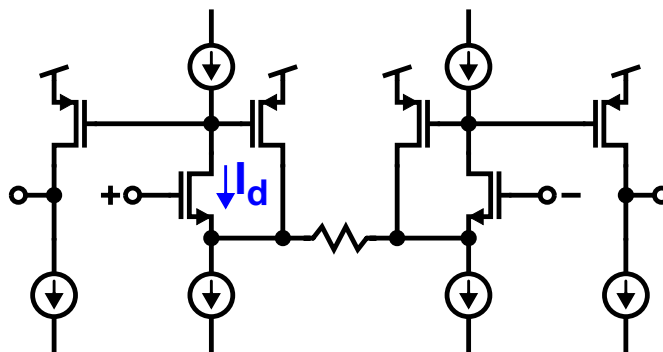


- + Simple!
- V_{gs} varies nonlinearly with $I_{out} \Rightarrow g_m$ is nonlinear

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Force Constant V_{gs}

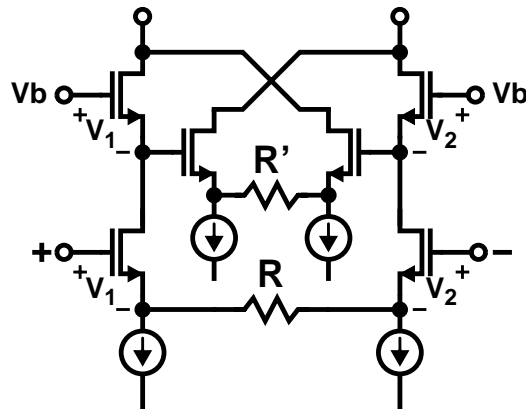


- I_d constant $\Rightarrow V_{gs}$ constant
- Linearity dependent on current-mirror linearity

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Cascomp

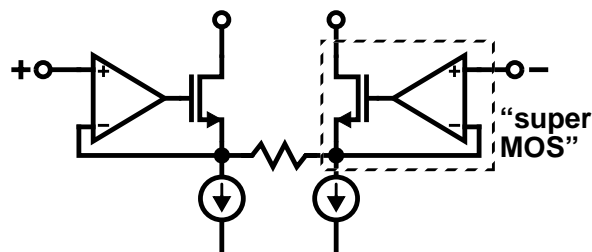


- V_{gs} of input devices replicated in cascodes and distortion-cancelling current injected into output
- + All NMOS \Rightarrow fast
- Cancellation depends on matching
Should tie bulk to source?

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Add Op Amps

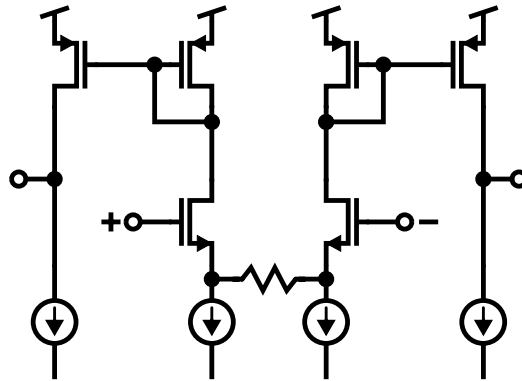


- + Linearity limited only by op amp gain and BW
- + High output resistance
- Output compliance depends on input swing

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Mirror the Output Current

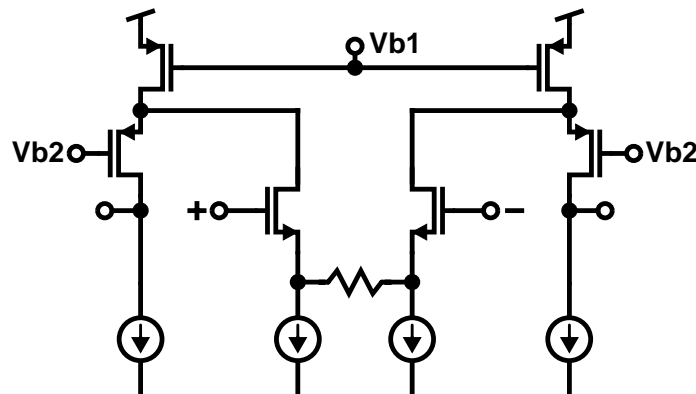


- + Output compliance is $V_{DD} - 2 V_{dsat}$
- Top of differential pair at $V_{DD} - V_{gs}$

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Fold the Output Current



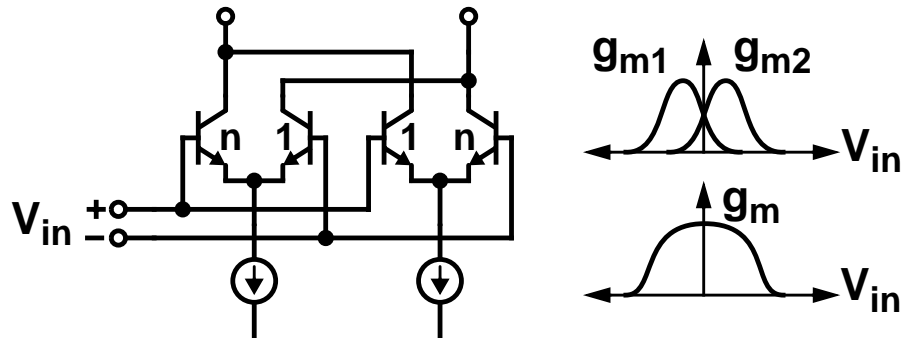
- + Increased headroom for differential pair
- + Increased output resistance

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Multi-Tanh Doublet

[Gilbert JSSC Dec. 1998]



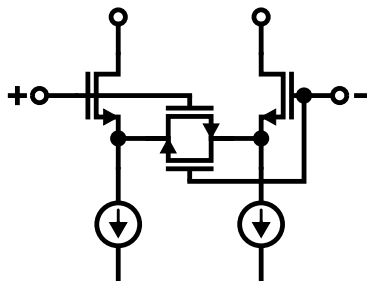
- With BJTs, ratioing the emitter areas creates a well-controlled offset
- With the right offset, the cubic term in the nonlinearity is zero!

$$n = 2 + \sqrt{3} = 3.73 \approx 15/4$$

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MOS Quad



- Supposedly can get less distortion than a degenerated differential pair by fiddling with W/L

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What You Learned Today

- 1 Operation of Example Comparator Circuit**
- 2 Regeneration Time Constant**
- 3 Metastability, Probability of Error**
- 4 Dynamic Offset**
- 5 Other Comparator Circuits**
- 6 A Bunch of Transconductor Circuits**