

ECE1371 Advanced Analog Circuits

Lecture 3

EXAMPLE DESIGN– PART 1

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Course Goals

- **Deepen understanding of CMOS analog circuit design through a top-down study of a modern analog system— a delta-sigma ADC**
- **Develop circuit insight through brief peeks at some nifty little circuits**

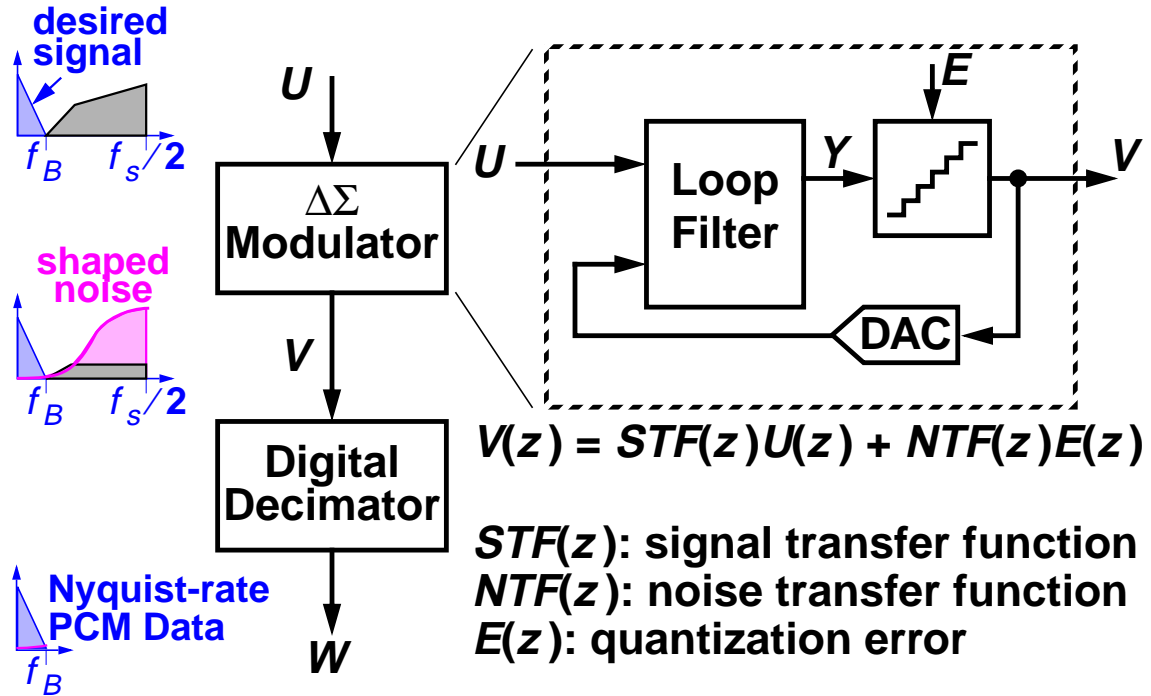
The circuit world is filled with many little gems that every competent designer ought to know.

Date	Lecture (M 13:00-15:00)		Ref	Homework	
2015-01-05	RS	1	MOD1 & MOD2	ST 2, 3, A	1: Matlab MOD1&2
2015-01-12	RS	2	MODN + $\Delta\Sigma$ Toolbox	ST 4, B	2: $\Delta\Sigma$ Toolbox
2015-01-19	RS	3	Example Design: Part 1	ST 9.1, CCJM 14	3: Sw.-level MOD2
2015-01-26	RS	4	Example Design: Part 2	CCJM 18	
2015-02-02	TC	5	SC Circuits	R 12, CCJM 14	4: SC Integrator
2015-02-09	TC	6	Amplifier Design		
2015-02-16	Reading Week– No Lecture				
2015-02-23	TC	7	Amplifier Design		5: SC Int w/ Amp
2015-03-02	RS	8	Comparator & Flash ADC	CCJM 10	Project
2015-03-09	TC	9	Noise in SC Circuits	ST C	
2015-03-16	RS	10	Advanced $\Delta\Sigma$	ST 6.6, 9.4	
2015-03-23	TC	11	Matching & MM-Shaping	ST 6.3-6.5, +	
2015-03-30	TC	12	Pipeline and SAR ADCs	CCJM 15, 17	
2015-04-06	Exam		Proj. Report Due Friday April 10		
2015-04-13	Project Presentation				

Highlights (i.e. What you will learn today)

- 1 MOD2 implementation
- 2 Switched-capacitor integrator
Switched-C summer & DAC too
- 3 Dynamic-range scaling
- 4 kT/C noise
- 5 Verification strategy

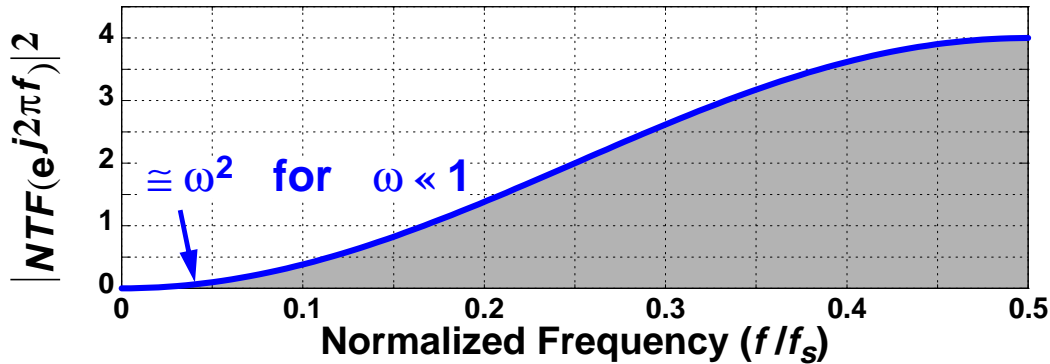
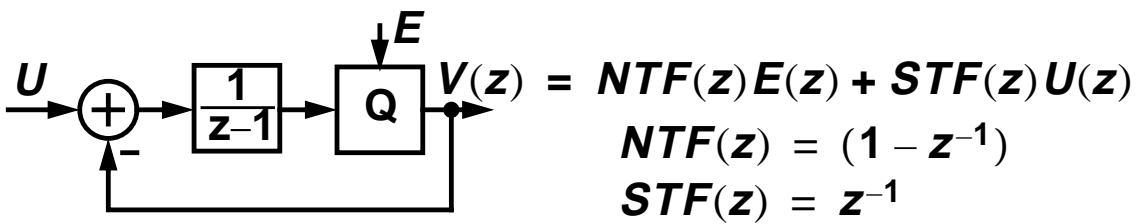
Review: A $\Delta\Sigma$ ADC System



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Review: MOD1

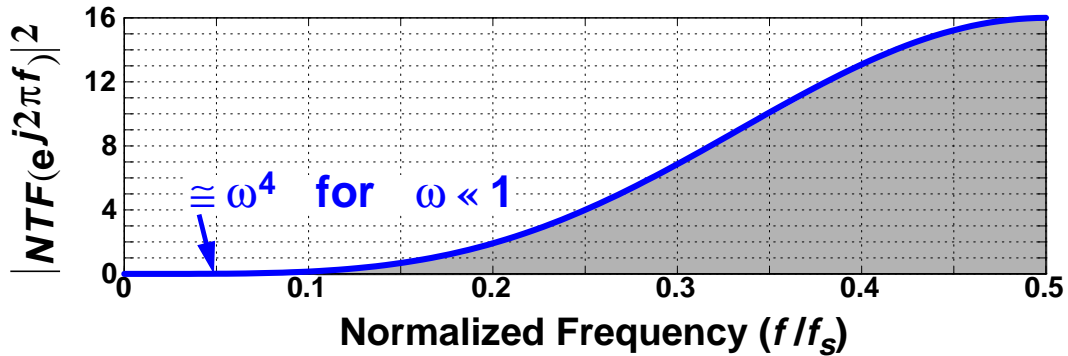
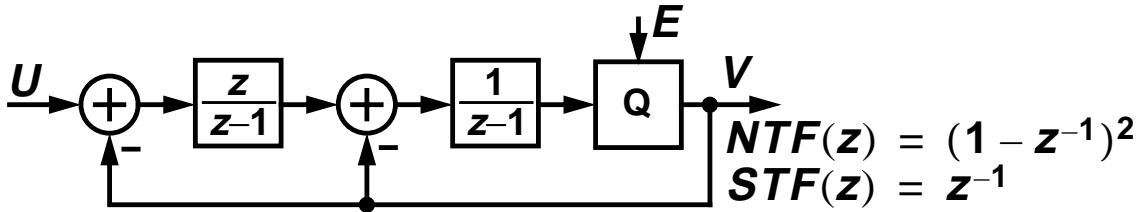


- Doubling OSR improves SQNR by 9 dB**
 Peak SQNR $\approx \text{dbp}(9 \cdot OSR^3 / (2\pi^2))$; $\text{dbp}(x) \equiv 10\log_{10}(x)$

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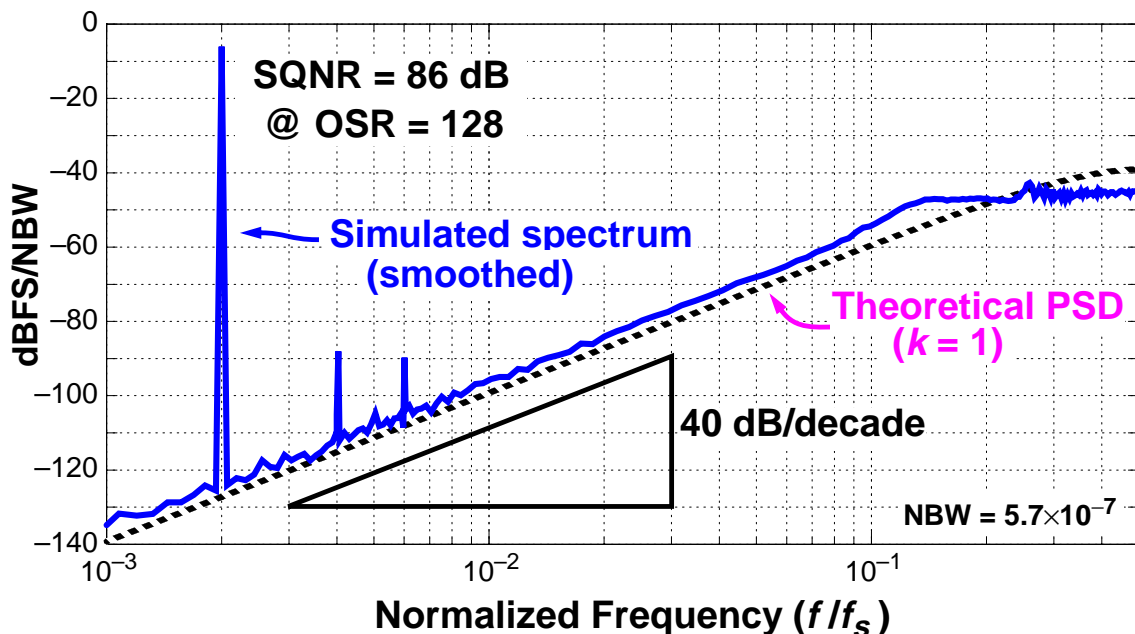
3-6

Review: MOD2



- Doubling OSR improves SQNR by 15 dB
 Peak SQNR $\approx \text{dbp}((15 \cdot OSR^5)/(4\pi^4))$

Review: Simulated MOD2 PSD Input at 50% of FullScale



Review: Advantages of $\Delta\Sigma$

- **ADC: Simplified Anti-Alias Filter**
Since the input is oversampled, only very high frequencies alias to the passband.
A simple RC section often suffices.
If a continuous-time loop filter is used, the anti-alias filter can often be eliminated altogether.
- **DAC: Simplified Reconstruction Filter**
The nearby images present in Nyquist-rate reconstruction can be removed digitally.
- + **Inherent Linearity**
Simple structures can yield very high SNR.
- + **Robust Implementation**
 $\Delta\Sigma$ tolerates sizable component errors.

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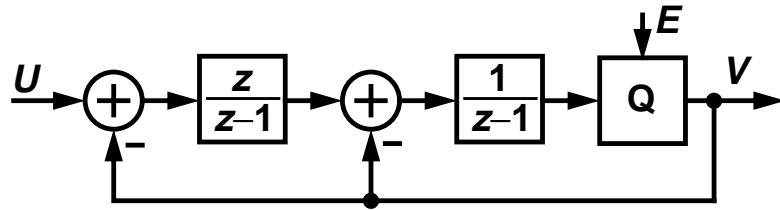
Let's Try Making One!

- **Clock at $f_s = 1$ MHz.**
Assume $BW = 1$ kHz.
- $\Rightarrow OSR = f_s / (2 \cdot BW) = 500 \approx 2^9$
- **MOD1: SQNR ≈ 9 dB/octave $\cdot 9$ octaves = 81 dB**
 - **MOD2: SQNR ≈ 15 dB/octave $\cdot 9$ octaves = 135 dB**
Actually more like 120 dB.
 - **SQNR of MOD1 is not bad, but SQNR of MOD2 is awesome!**
In addition to MOD2's SQNR advantage, MOD2 is usually preferred over MOD1 because MOD2's quantization noise is more well-behaved.

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What Do We Need?



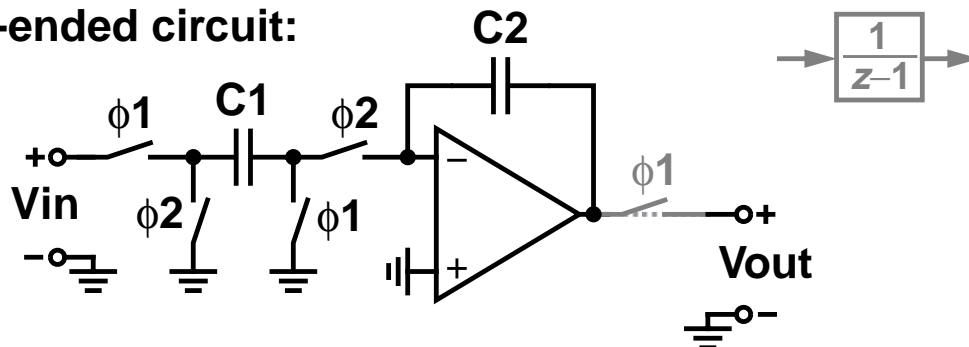
- 1 Summation blocks
- 2 Delaying and non-delaying discrete-time integrators
- 3 Quantizer (1-bit)
- 4 Feedback DACs (1-bit)
- 5 Decimation filter (not shown)
Digital and therefore “easy.”

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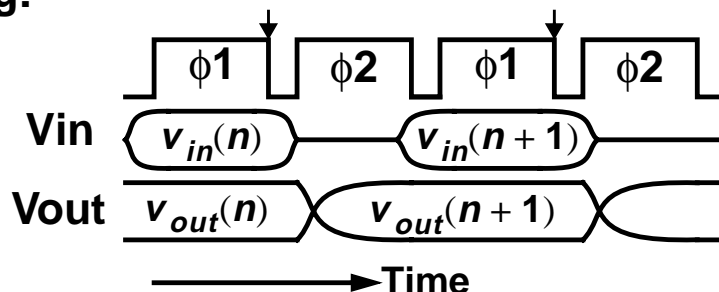
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Switched-Capacitor Integrator

Single-ended circuit:



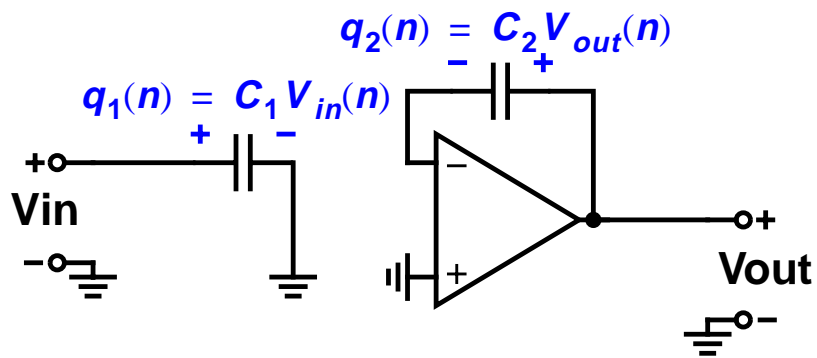
Timing:



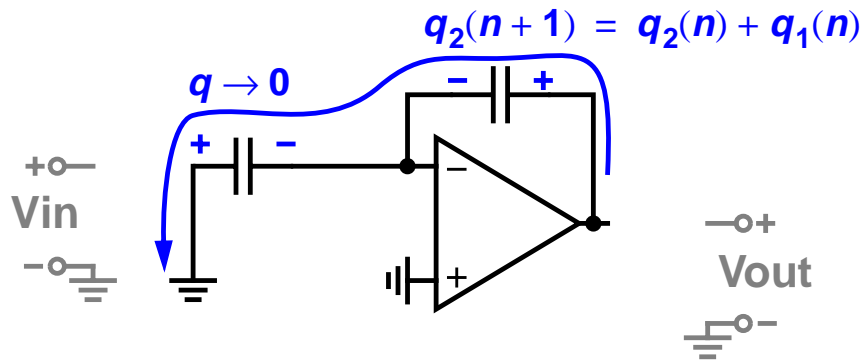
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$\phi 1:$



$\phi 2:$



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$$q_2(n+1) = q_2(n) + q_1(n)$$

$$zQ_2(z) = Q_2(z) + Q_1(z)$$

$$Q_2(z) = \frac{Q_1(z)}{z-1}$$

- This circuit integrates charge
- Since $Q_1 = C_1 V_{in}$ and $Q_2 = C_2 V_{out}$

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1/C_2}{z-1}$$

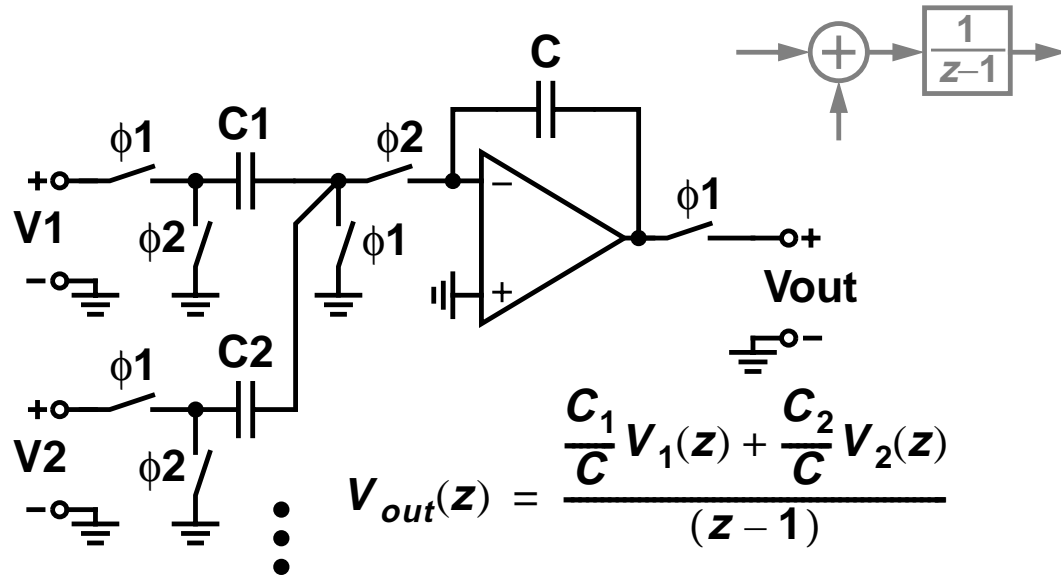
- Note that the voltage gain is controlled by a *ratio* of capacitors

With careful layout, 0.1% accuracy is possible.

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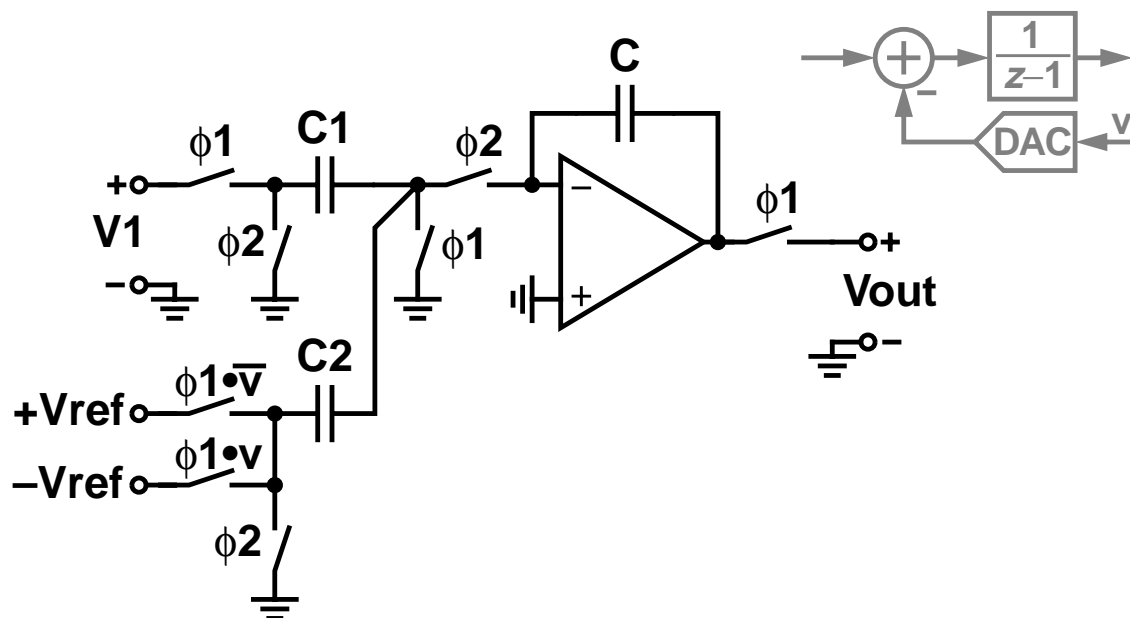
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Summation + Integration

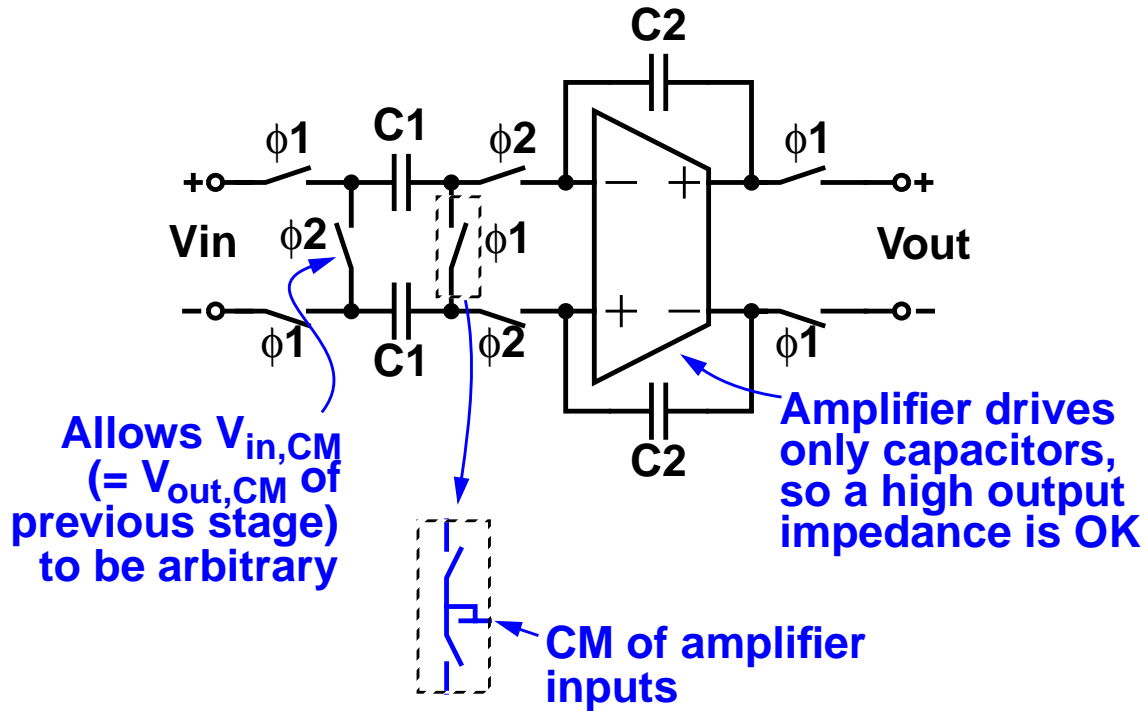


⇒ Adding an extra input branch accomplishes addition, with weighting

1b DAC + Summation + Integration



Differential Integrator

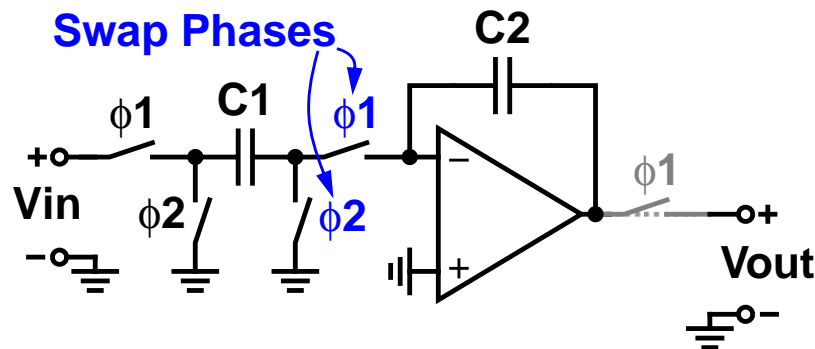


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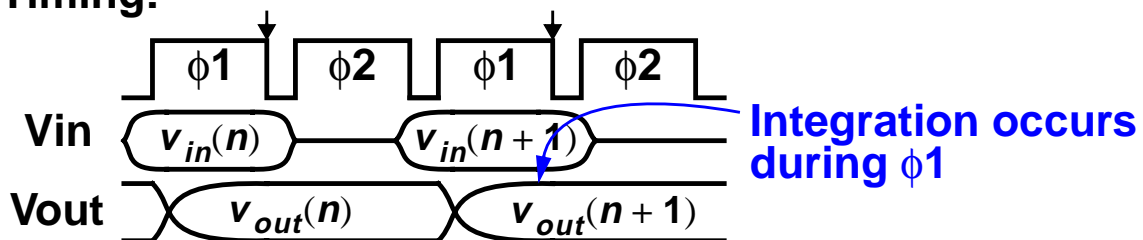
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Non-Delaying Integrator

Single-ended circuit:



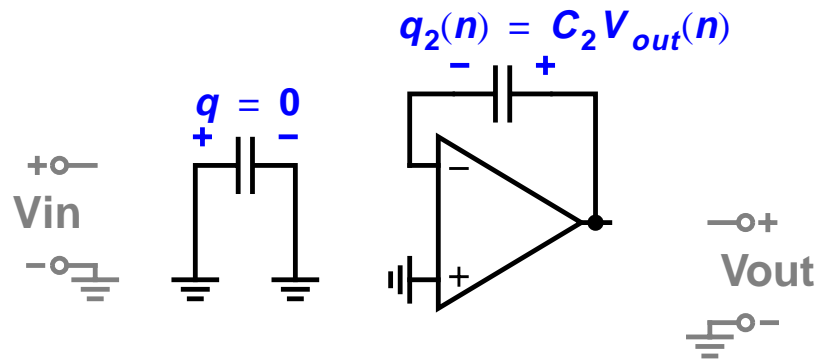
Timing:



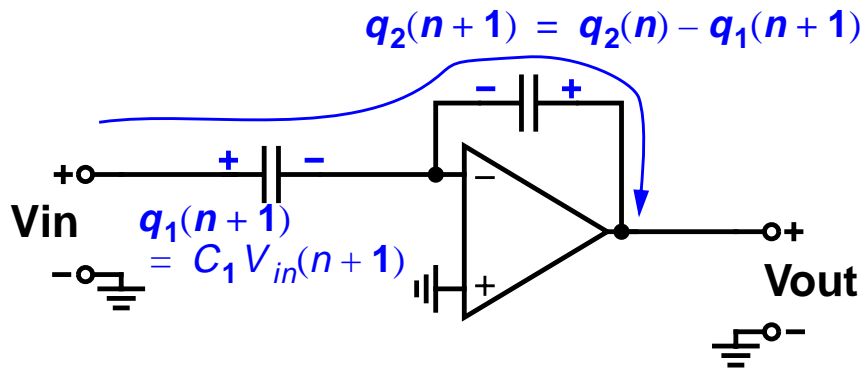
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ϕ_2 :



ϕ_1 :



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$$q_2(n+1) = q_2(n) - q_1(n+1)$$

$$zQ_2(z) = Q_2(z) - zQ_1(z)$$

$$\frac{Q_2(z)}{Q_1(z)} = -\frac{z}{z-1}$$

$$\frac{V_{out}(z)}{V_{in}(z)} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z-1}$$

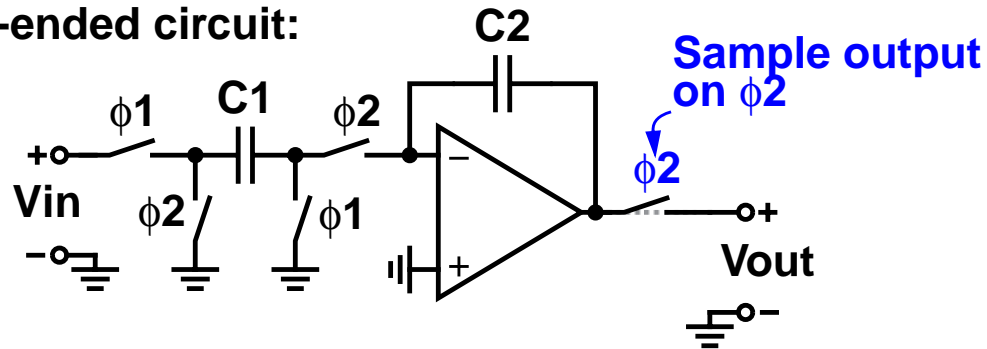
- Delay-free integrator (inverting)

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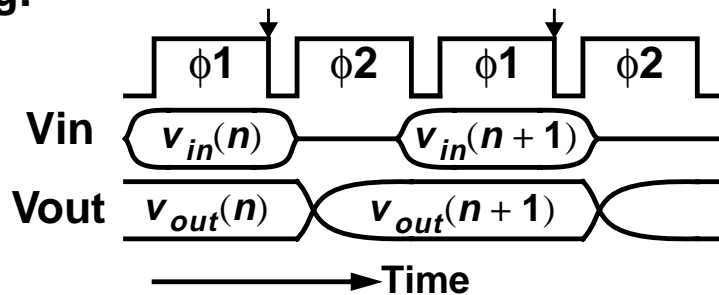
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“Half-Delay” Integrator

Single-ended circuit:



Timing:



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Half-Delay Integrator

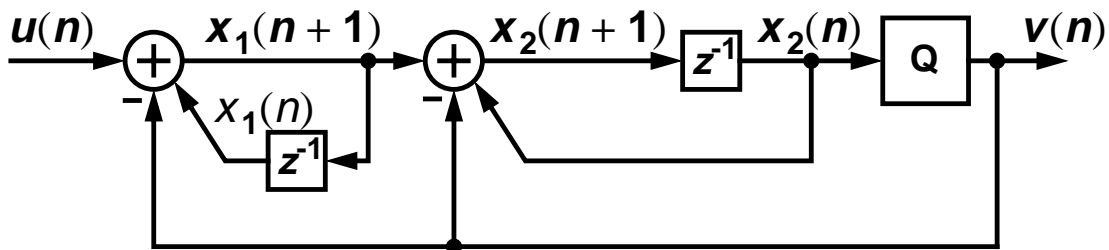
- Output is sampled on a different phase than the input
 - Some use the notation $H(z) = \frac{z^{-1/2}}{z-1}$ to denote the shift in sampling time
I consider this an abuse of notation.
 - An alternative method is to declare that the border between time n and $n+1$ occurs at the end of a specific phase, say ϕ_2
- ⇒ A circuit which samples on ϕ_1 and updates on ϕ_2 is non-delaying, i.e. $H(z) = z/(z-1)$, whereas a circuit which samples on ϕ_2 and updates on ϕ_1 is delaying, i.e. $H(z) = 1/(z-1)$.

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Timing in a $\Delta\Sigma$ ADC

- The safest way to deal with timing is to construct a timing diagram and verify that the circuit implements the desired difference equations
- E.g. MOD2:



Difference Equations:

$$v(n) = Q(x_2(n)) \quad (0)$$

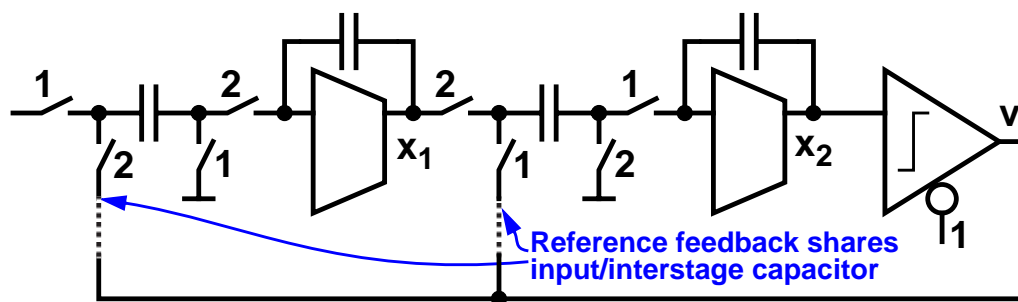
$$x_1(n+1) = x_1(n) - v(n) + u(n) \quad (1)$$

$$x_2(n+1) = x_2(n) - v(n) + x_1(n+1) \quad (2)$$

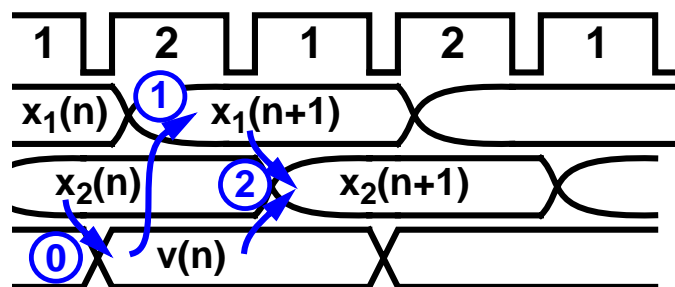
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Switched-Capacitor Realization



Timing



Timing looks OK!

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Signal Swing

- So far, we have not paid any attention to how much swing the op amps can support, or to the magnitudes of u , V_{ref} , x_1 and x_2
- For simplicity, assume:
 - the full-scale range of u is ± 1 V,
 - the op-amp swing is also ± 1 V and $V_{\text{ref}} = 1$ V
- We still need to know the ranges of x_1 and x_2 in order to accomplish *dynamic-range scaling*

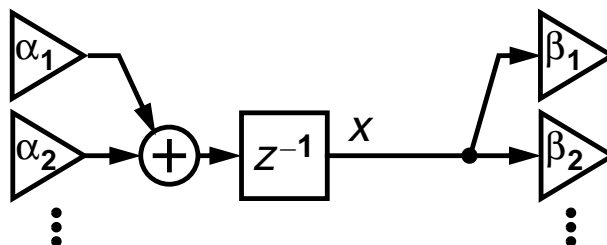
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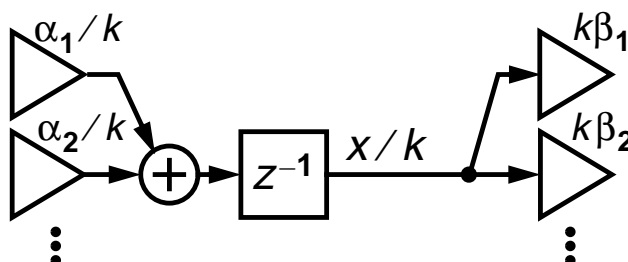
Dynamic-Range Scaling

- In a linear system with known state bounds, the states can be scaled to occupy any desired range

e.g. one state of original system:



state scaled by $1/k$:

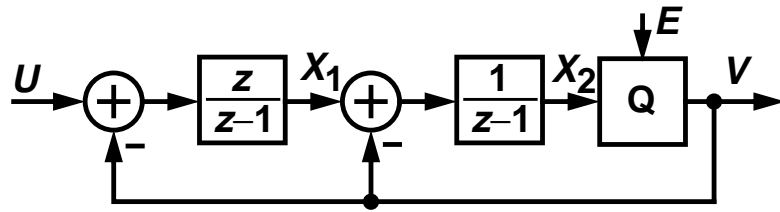


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State Swings in MOD2

Linear Theory



$$V = z^{-1}U + (1 - z^{-1})^2 E$$

$$X_1 = \frac{z}{z-1}(U - V) = U - (1 - z^{-1})E$$

$$X_2 = V - E = z^{-1}U + (-2z^{-1} + z^{-2})E$$

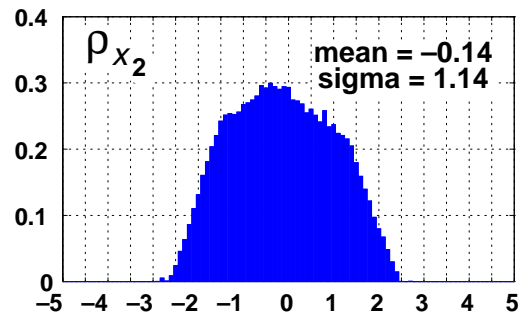
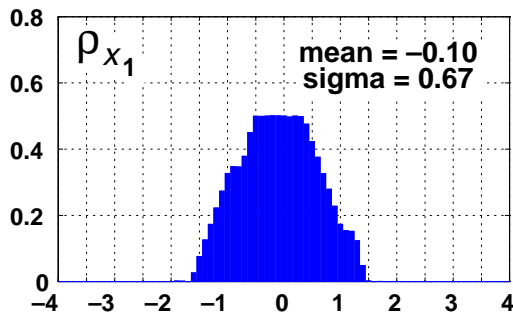
- If u is constant and e is white with power $\sigma_e^2 = 1/3$, then $x_1 = u$, $\sigma_{x_1}^2 = 2\sigma_e^2 = 2/3$, $x_2 = u$ and $\sigma_{x_2}^2 = 5\sigma_e^2 = 5/3$

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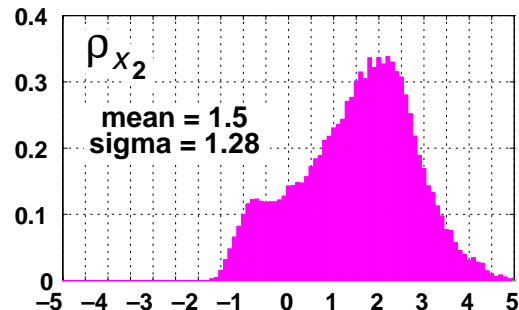
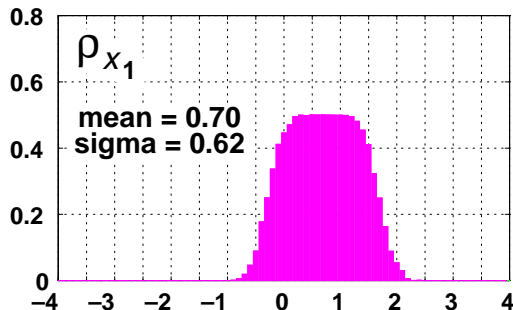
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Simulated Histograms

$u = -0.1$



$u = 0.7$



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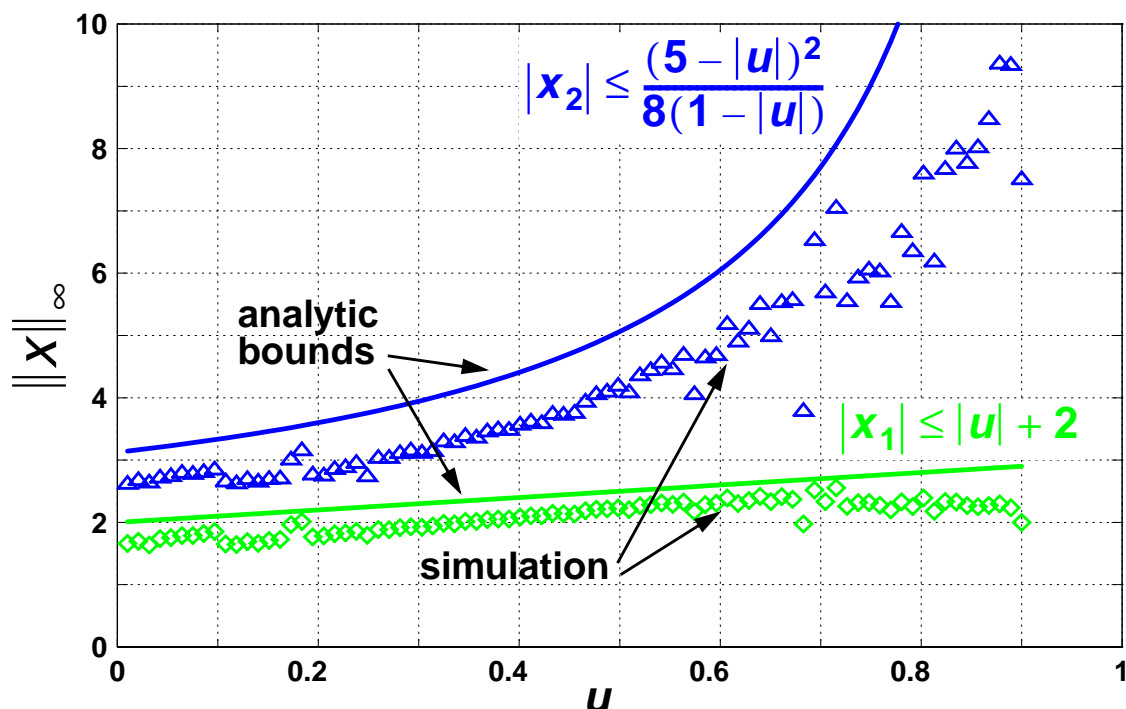
Observations

- The match between simulations and our linear theory is fair for x_1 , but poor for x_2
 - x_1 's mean and standard deviation match theory, although x_1 's distribution does not have the triangular form that would result if e were white and uniformly-distributed in $[-1,1]$.
 - x_2 's mean is 50-100% high, its standard deviation is ~25% low, and the distribution is weird.
- ⇒ Our linear theory is not adequate for determining signal swings in MOD2
- No real surprise. Linear theory does not handle overload, i.e. where $x_1, x_2 \rightarrow \infty$ when $u > 1$.
- Is there a better theory?
 - Yes, but it is complicated and gives minimal insight.

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MOD2 Simulated State Bounds

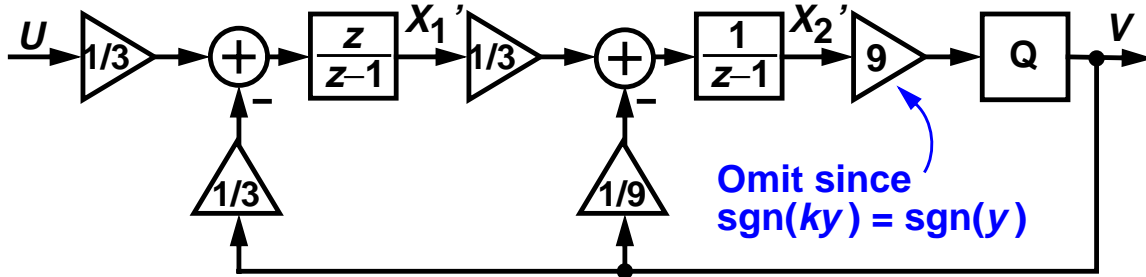


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Scaled MOD2

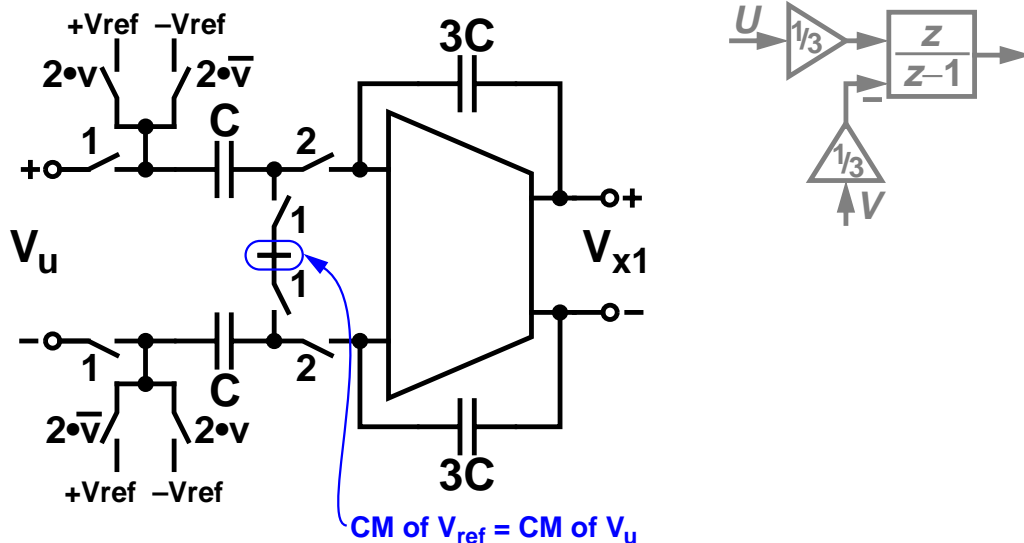
- Take $\|x_1\|_\infty = 3$ and $\|x_2\|_\infty = 9$
 The first integrator should not saturate.
 The second integrator will not saturate for dc inputs up to -3 dBFS and possibly as high as -1 dBFS.
- Our scaled version of MOD2 is thus



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First Integrator (INT1) Shared Input/Reference Caps

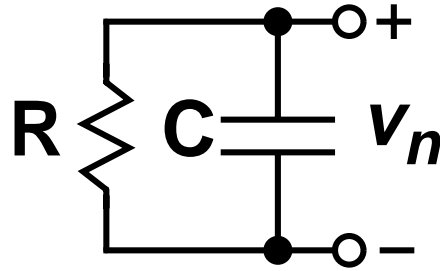


- How do we determine C?

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kT/C Noise



- **Fact:** Regardless of the value of R , the mean-square value of the voltage on C is

$$\overline{v_n^2} = \frac{kT}{C}$$

where $k = 1.38 \times 10^{-23}$ J/K is *Boltzmann's constant* and T is the temperature in Kelvin

The ms noise charge is $\overline{q_n^2} = C^2 \overline{v_n^2} = kTC$.

Derivation of kT/C Noise

- **Equipartition of Energy** physical principle: “In a system at thermal equilibrium, the average energy associated with any degree of freedom is $\frac{1}{2}kT$.”

This applies to the kinetic energy of atoms (along each axis of motion), vibrational energy in molecules and to the potential energy in electrical components.

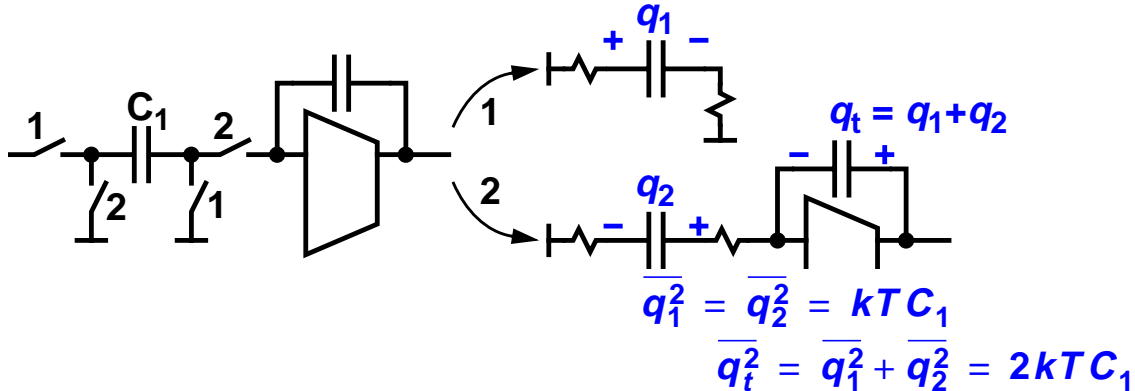
- **Fact:** The energy stored in a capacitor is $\frac{1}{2}CV^2$

- So, according to equipartition, $\frac{1}{2}\overline{CV^2} = \frac{1}{2}kT$,
or

$$\overline{V^2} = \frac{kT}{C}$$

Implications for an SC Integrator

- Each charge/discharge operation has a random component
 - The amplifier plays a role during phase 2, but we'll assume that the noise in both phases is just kT/C . Trevor will revisit this assumption in Lecture 9.
- For a given cap, these random components are essentially uncorrelated, so the noise is white

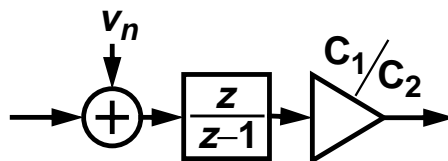


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Integrator Implications (cont'd)

- This noise charge is equivalent to a noise voltage with ms value $v_n^2 = 2kT/C_1$ added to the input of the integrator:



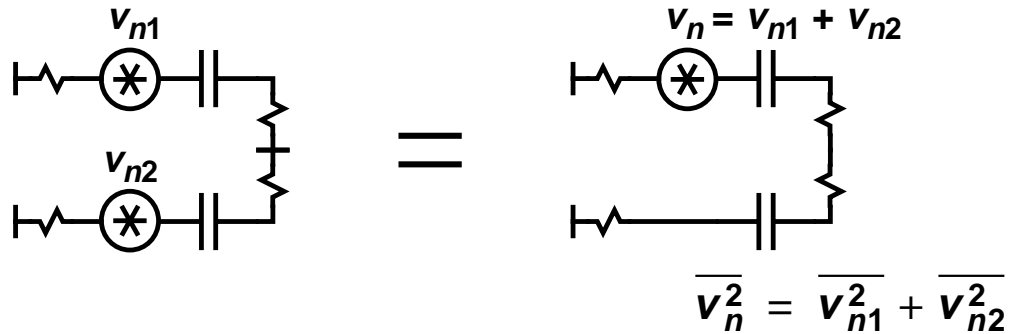
- This noise power is spread uniformly over all frequencies from 0 to $f_s/2$

⇒ The power in the band $[0, f_B]$ is v_n^2 / OSR

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Differential Noise



- Twice as many switched caps
⇒ twice as much noise power
- The input-referred noise power in our differential integrator is

$$\overline{v_n^2} = 4kT / C_1$$

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INT1 Absolute Capacitor Sizes For SNR = 100 dB @ -3-dBFS input

- The signal power is

$$\overline{v_s^2} = \underbrace{\frac{1}{2}}_{-3 \text{ dBFS}} \cdot \underbrace{\frac{(1 \text{ V})^2}{2}}_{\frac{A^2}{2}} = 0.25 \text{ V}^2$$

- Therefore we want $\overline{v_{n, \text{in-band}}^2} = 0.25 \times 10^{-10} \text{ V}^2$
- Since $\overline{v_{n, \text{in-band}}^2} = \overline{v_n^2} / \text{OSR}$

$$C_1 = \frac{4kT}{\overline{v_n^2}} = 1.33 \text{ pF}$$

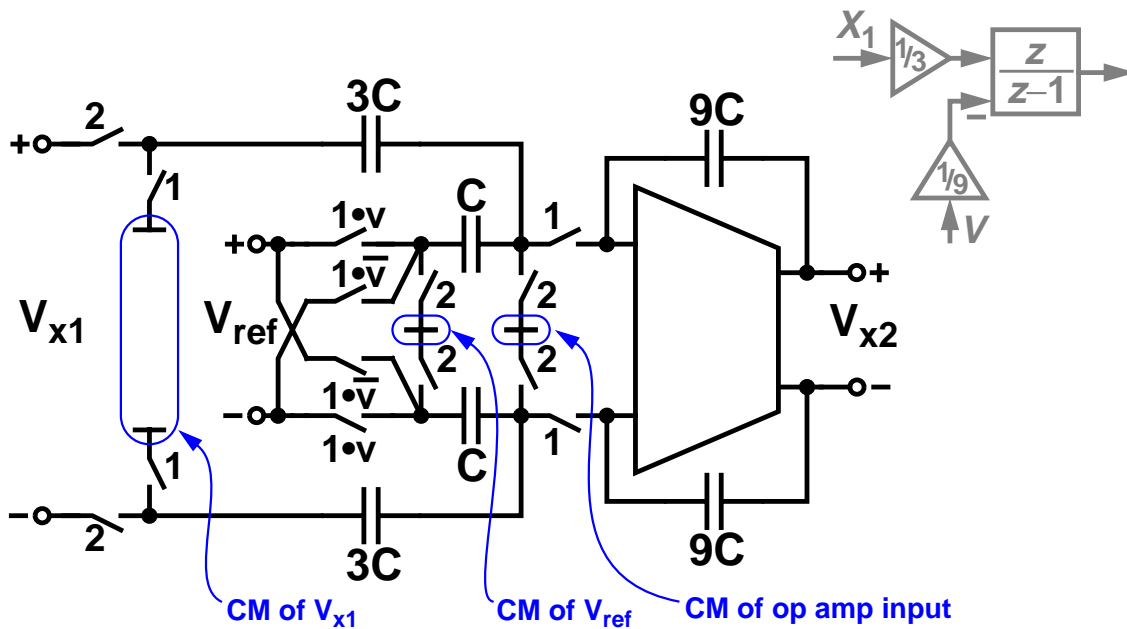
- If we want 10 dB more SNR, we need 10x caps

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Second Integrator (INT2)

Separate Input and Feedback Caps

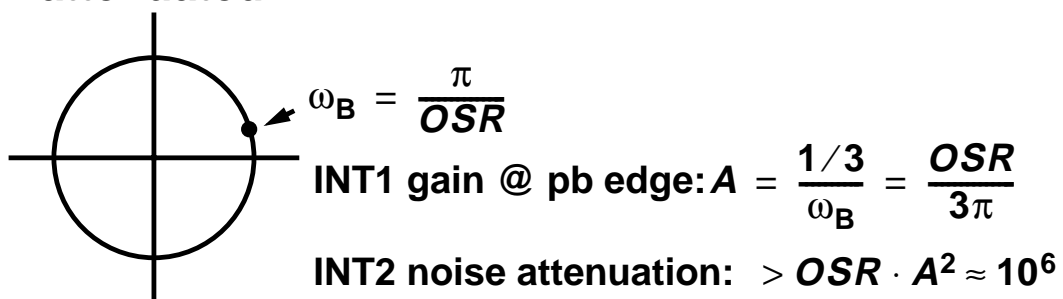


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INT2 Absolute Capacitor Sizes

- In-band noise of second integrator is greatly attenuated



⇒ Capacitor sizes not dictated by thermal noise

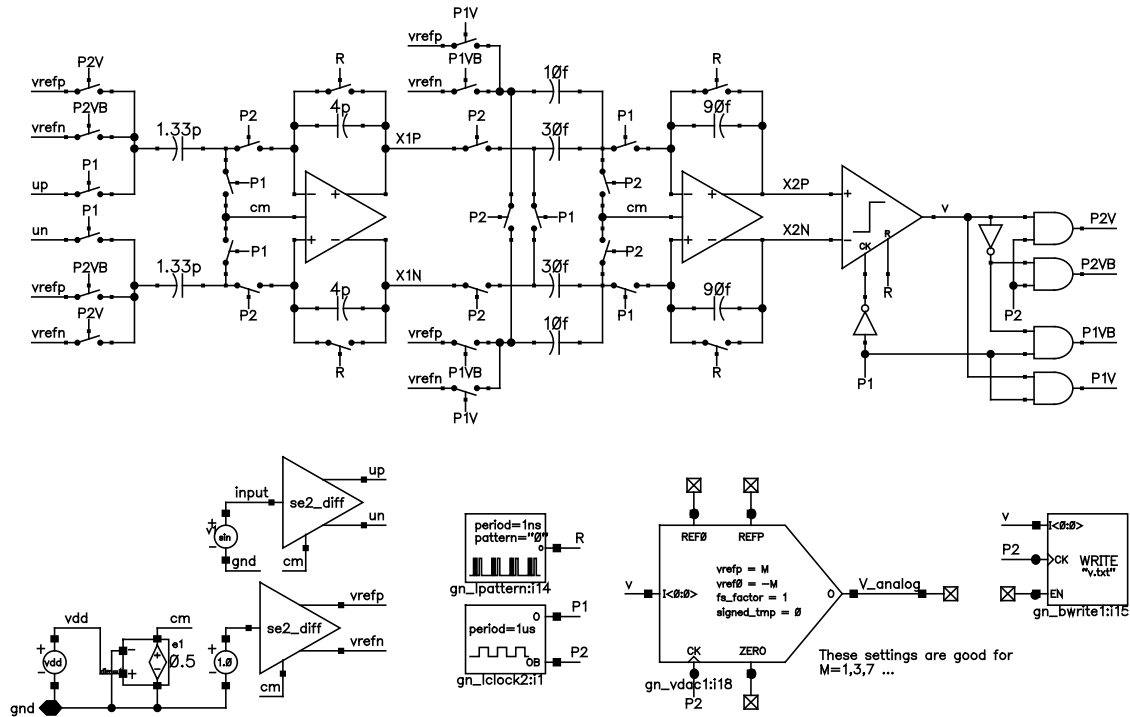
- Charge injection errors and desired ratio accuracy set absolute size

A reasonable size for a small cap is currently ~10 fF.

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Behavioral Schematic



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Verification

Open-loop verification

- 1 Loop filter
- 2 Comparator

Since MOD2 is a 1-bit system, all that can go wrong is the polarity and the timing. Usually the timing is checked by (1), so this verification step is not needed.

Closed-loop verification

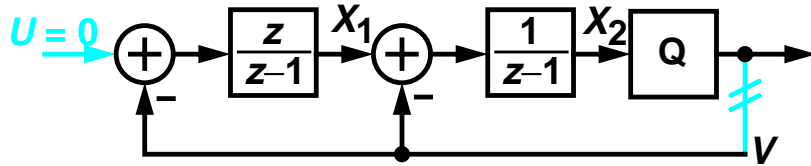
- 3 Swing of internal states
- 4 Spectrum: SQNR, STF gain
- 5 Sensitivity, start-up, overload recovery, ...

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Loop-Filter Check— Theory

- Open the feedback loop, set $u = 0$ and drive an impulse through the feedback path

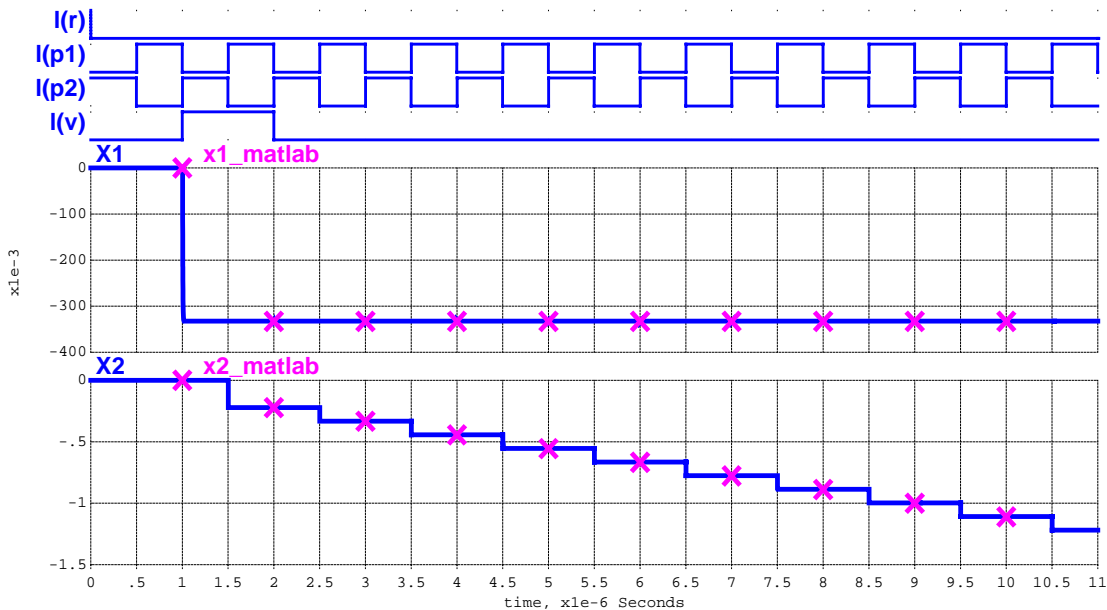


$$X_2 = \frac{-1}{z-1} \left(1 + \frac{z}{z-1} \right) Y$$

$$\therefore y(n) = \{1, 0, 0, \dots\} \Rightarrow x_2(n) = \{-2, -3, -4, \dots\}$$

- If x_2 is as predicted then the loop filter is correct
At least for the feedback signal, which implies that the NTF will be as designed.

Loop Filter Check— Practice*



*. "In theory there is no difference between theory and practice.
But in practice there is."

Hey! You Cheated!

- An impulse is $\{1,0,0,\dots\}$, but a binary DAC can only output ± 1 , i.e. it cannot produce a 0

Q: So how can we determine the impulse response of the loop filter through simulation?

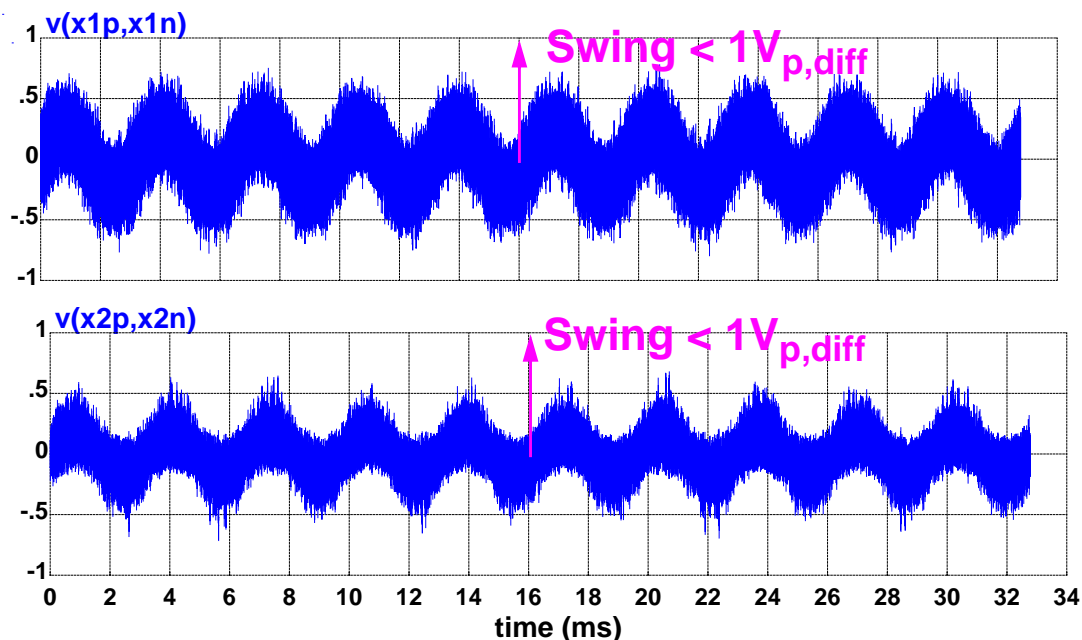
A: Do two simulations: one with $v = \{-1,-1,-1,\dots\}$ and one with $v = \{+1,-1,-1,\dots\}$.

Then take the difference.

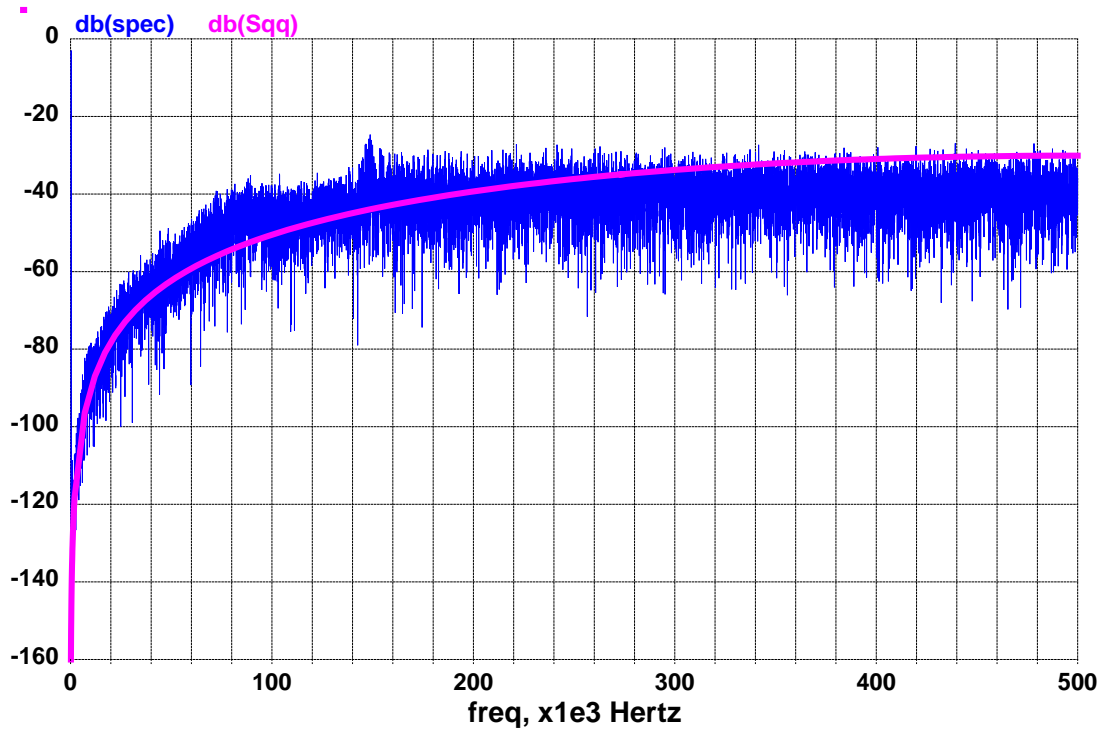
According to superposition, the result is the response to $v = \{2,0,0,\dots\}$, so divide by 2.

To keep the integrator states from growing too quickly, you could also use $v = \{-1,-1,+1,-1,\dots\}$ and then $v = \{+1,-1,+1,-1,\dots\}$.

Simulated State Swings -3-dBFS ~300-Hz sine wave



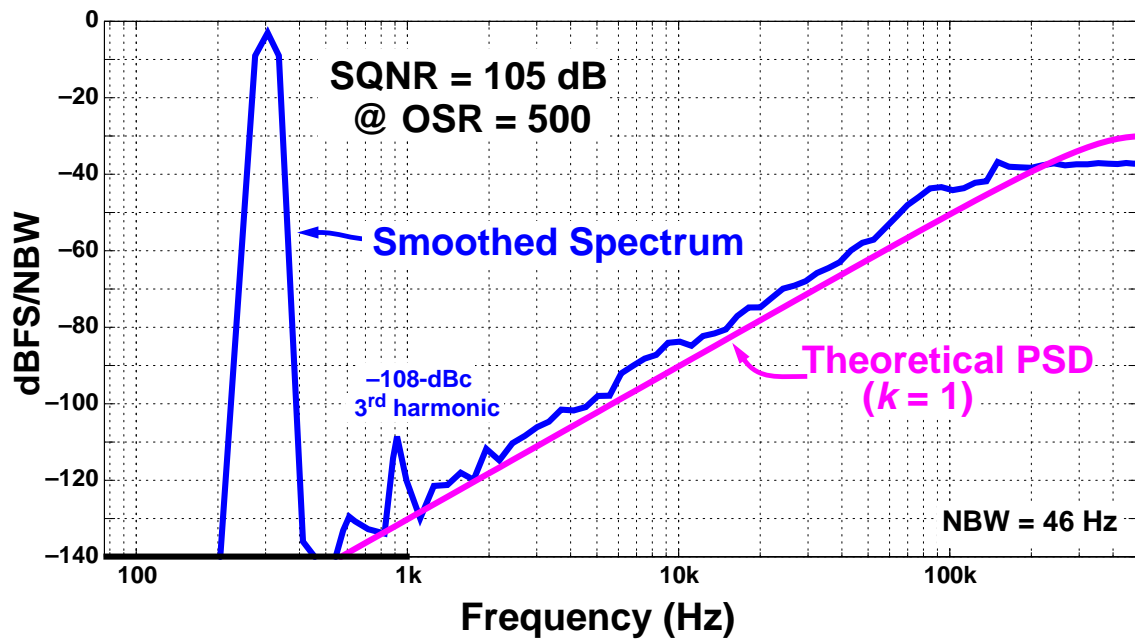
Unclear Spectrum



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Professional Spectrum



- SQNR dominated by -109-dBFS 3rd harmonic

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Implementation Summary

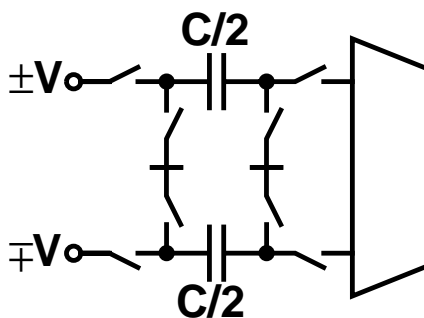
- 1 Choose a viable SC topology and manually verify timing
- 2 Do dynamic-range scaling
You now have a set of capacitor ratios.
Verify operation: loop filter, timing, swing, spectrum.
- 3 Determine absolute capacitor sizes
Verify noise.
- 4 Determine op-amp specs and construct a transistor-level schematic
Verify everything.
- 5 Layout, fab, debug, document, get customers, sell by the millions, go public, ...

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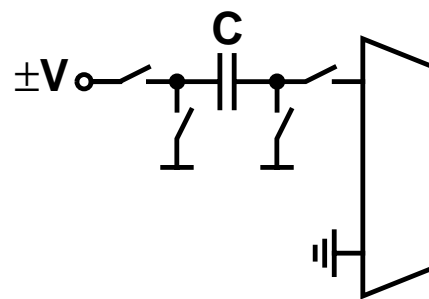
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Differential vs. Single-Ended

- Differential is more complicated and has more caps and more noise \Rightarrow single-ended is better?



$$SNR = \frac{(2V)^2/2}{4kT/(C/2)} = \frac{CV^2}{4kT}$$



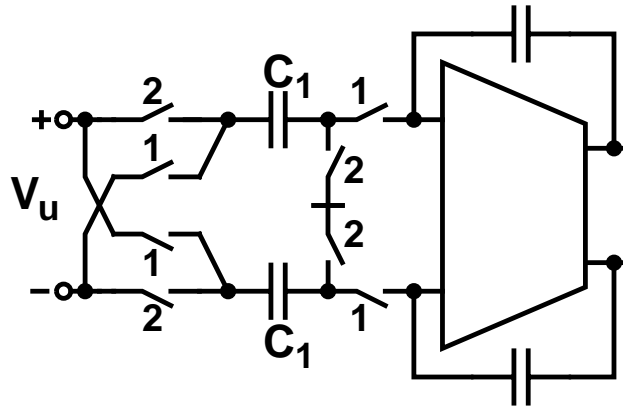
$$SNR = \frac{V^2/2}{2kT/C} = \frac{CV^2}{4kT}$$

- Same capacitor area \Rightarrow same SNR
Differential is generally preferred due to rejection of even-order distortion and common-mode noise/interference.

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Double-Sampled Input



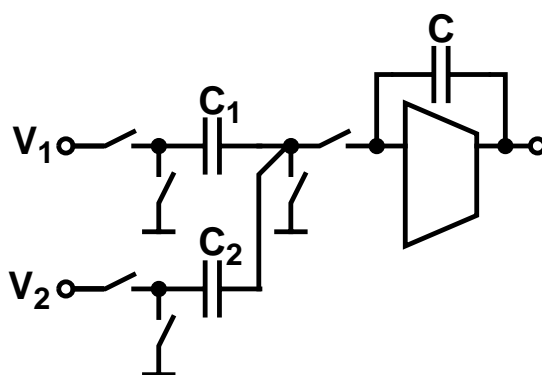
- Doubles the effective input signal
- Allows C_1 to be 1/4 the size for the same SNR
- Doubles the sampling rate of the signal, thereby easing AAF further

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Shared vs. Separate Input Caps

- Separate caps \Rightarrow More noise:



$$V_1 \text{ input: } \overline{v_{n1}^2} = 2kT/C_1$$

$$V_2 \text{ input: } \overline{v_{n2}^2} = 2kT/C_2$$

$$V_2 \text{ gain / } V_1 \text{ gain: } C_2/C_1$$

$$v_{n2} \text{ referred to } V_1: v_{n2} C_2/C_1$$

$$\text{Total noise referred to } V_1: (2kT/C_1)(1 + C_2/C_1)$$

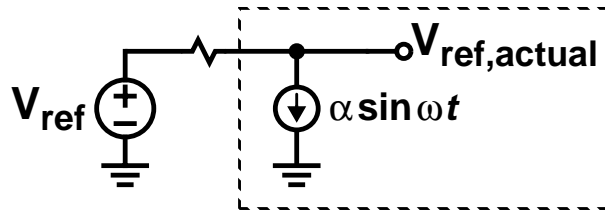
- But using separate caps allows input CM to be different from reference CM, and so is often preferred in a general-purpose ADC

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Signal-Dependent Ref. Loading

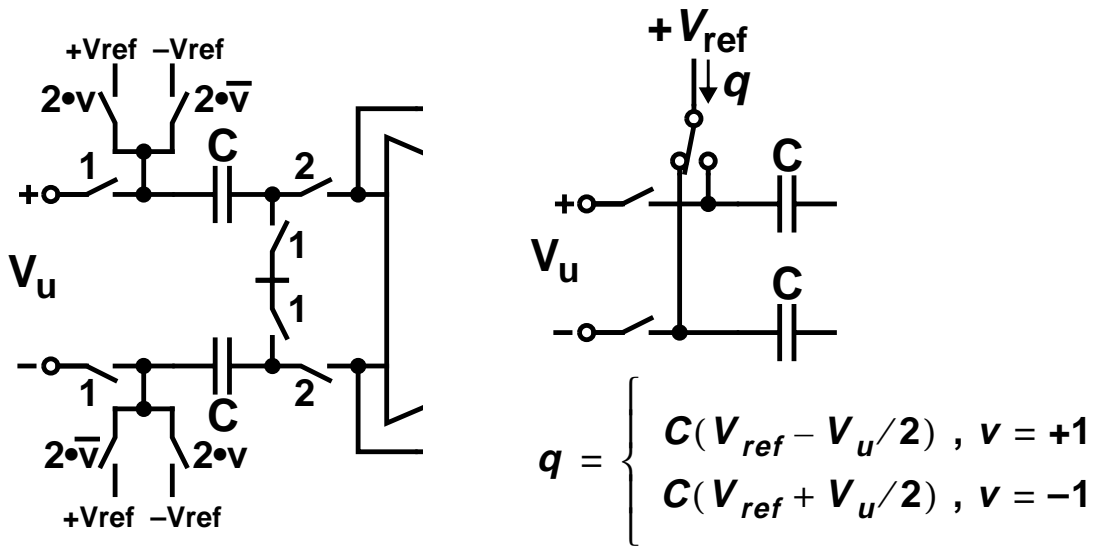
- Another practical concern is the current draw from the reference



$$\text{ADC Output} \propto \frac{V_{in}}{V_{ref}(1 - \epsilon \sin \omega t)} \approx \frac{V_{in}}{V_{ref}} (1 + \epsilon \sin \omega t)$$

- If the reference current is signal-related, harmonic distortion can result

Shared Caps and Ref. Loading



Thus

$$\bar{i} = \frac{C}{T}(V_{ref} - v \cdot V_u/2)$$

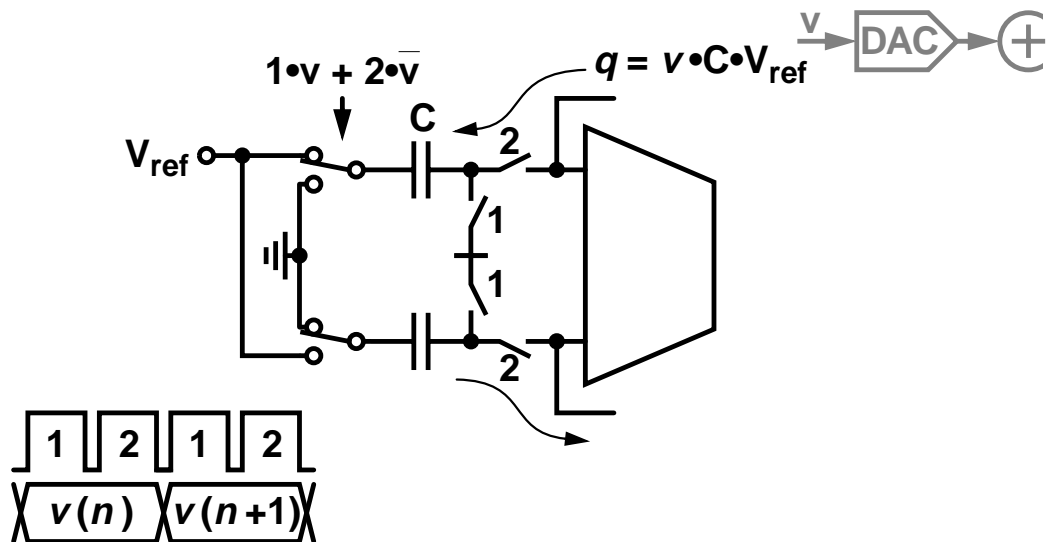
- If $u = A\sin\omega_u t$, then $v = u + \text{error}$ also contains a component at ω_u and thus I contains a component at $\omega = 2\omega_u$.
- Since ADC Output $\propto V_{in}(1 + \varepsilon \sin\omega t)$, the signal-dependent reference current in our circuit can produce 3rd-harmonic distortion

Also, the load presented to the driving circuit is dependent on v and this noisy load can cause trouble.

- With separate caps, the reference current is signal-independent

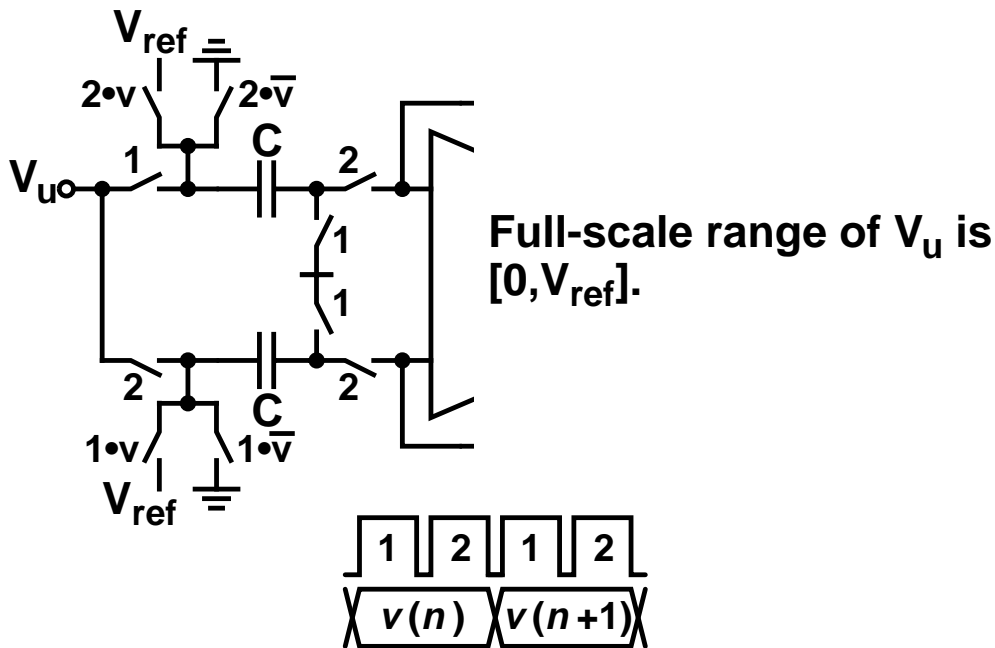
Yet another reason for using separate caps.

Unipolar Reference



- Be careful of the timing of v relative to the integration phase!

Single-Ended Input Shared Caps



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Homework #3 (Due 2015-02-02)

Construct a differential switched-capacitor implementation of MOD2 using ideal elements (switches, capacitors, amplifiers, comparator) and verify it.

Scale the circuit such that the full-scale differential input range is $[-1, +1]$ V and the op amp swing is $0.5 V_{p,diff}$ at -6 dBFS. You may assume that -0.5 -V and $+0.5$ -V references are available and that the input is available in differential form.

Choose capacitor values such that the SNR with a -6 dBFS input will be ~ 85 dB when $OSR = 128$. You may assume that the only source of noise is kT/C noise.

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Homework Deliverables

- 1 Schematic of MOD2 annotated with node voltages during reset (dc sim)
- 2 Open-loop impulse response plot (short transient sim)
- 3 Time-domain plots of input signal and integrator outputs for a -6 -dBFS input (transient sim)
- 4 Spectrum of output data for a -6 -dBFS input, with SNDR calculated
- 5 kT/C noise calculation (justify your choice of C)
- 6 Choose your own check and do it.

What You Learned Today And what the homework should solidify

- 1 MOD2 implementation
- 2 Switched-capacitor integrator
Switched-C summer & DAC too
- 3 Dynamic-range scaling
- 4 kT/C noise
- 5 Verification strategy