ECE1371 Advanced Analog Circuits
Lecture 8

COMPARATOR & FLASH ADC DESIGN

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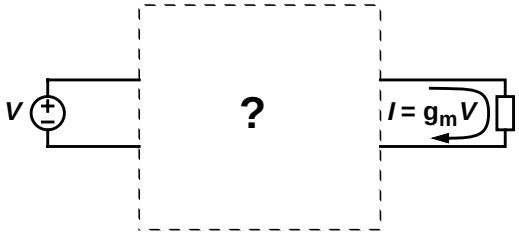
Course Goals

- **Deepen understanding of CMOS analog circuit design through a top-down study of a modern analog system— a delta-sigma ADC**
- **Develop circuit insight through brief peeks at some nifty little circuits**
  The circuit world is filled with many little gems that every competent designer ought to know.

Date	Lecture (M 13:00-15:00)			Ref	Homework
2015-01-05	RS	1	MOD1 & MOD2	ST 2, 3, A	1: Matlab MOD1&2
2015-01-12	RS	2	MOD*N* + ΔΣ Toolbox	ST 4, B	2: ΔΣ Toolbox
2015-01-19	RS	3	Example Design: Part 1	ST 9.1, CCJM 14	3: Sw.-level MOD2
2015-01-26	RS	4	Example Design: Part 2	CCJM 18	
2015-02-02	TC	5	SC Circuits	R 12, CCJM 14	4: SC circuit
2015-02-09	TC	6	Amplifier Design		
2015-02-16	Reading Week– No Lecture				
2015-02-23	TC	7	Amplifier Design		5: SC Int w/ Amp
2015-03-02	RS	8	Comparator & Flash ADC	CCJM 10	Project
2015-03-09	TC	9	Noise in SC Circuits	ST C	
2015-03-16	RS	10	Advanced ΔΣ	ST 6.6, 9.4	
2015-03-23	TC	11	Matching & MM-Shaping	ST 6.3-6.5, +	
2015-03-30	TC	12	Pipeline and SAR ADCs	CCJM 15, 17	
2015-04-06	Exam			Proj. Report Due Friday April 10	
2015-04-13	Project Presentation				

NLCOTD: Linear Transconductor

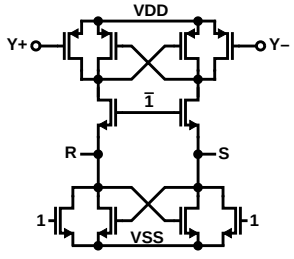


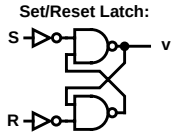
- **Useful in**
  1. **gm-C filter**
  2. **LNA**
  3. **mixer**
  4. **CT ΔΣ ADC**

Highlights
(i.e. What you will learn today)

1. **Operation of Example Comparator Circuit**
2. **Regeneration Time Constant τ**
3. **Metastability, Probability of Error**
4. **Offset, Dynamic Offset, Auto-zeroing**
5. **Flash ADC**
6. **A Bunch of Transconductor Circuits**

Review: Latched Comparator
From Lecture #4's 1-MHz MOD2

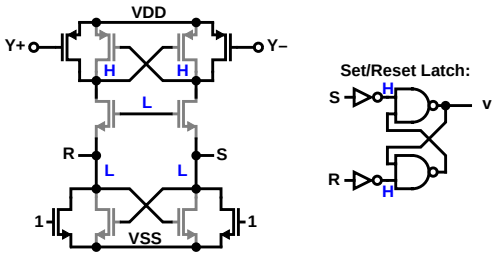




Inverter thresholds are chosen so that the inverters respond only after R/S have resolved.

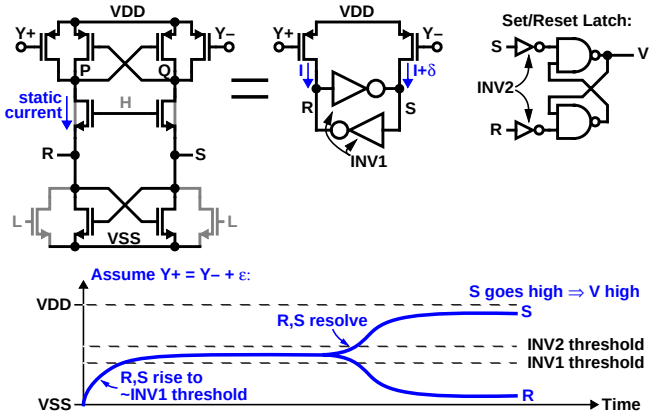
- **Falling phase 1 initiates regenerative action**
  S and R connected to a Set/Reset latch.

Phase 1 = High: “Reset” Mode



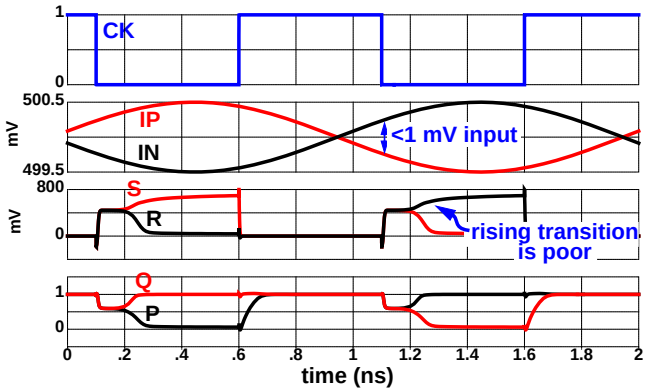
- Grayed-out devices are off
  ⇒ the active part of the comparator is reset
- R and S are low ⇒ the SR latch is in hold mode

Phase 1 Goes Low: “Latch” Mode

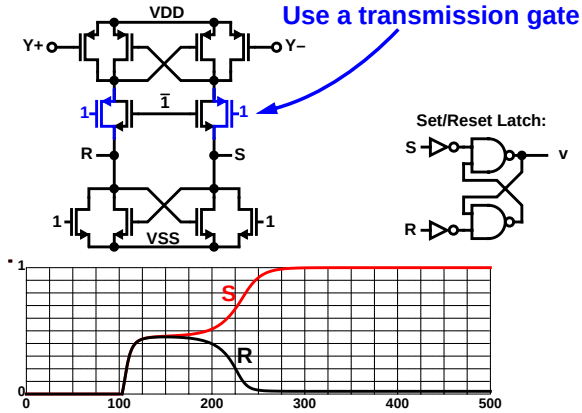


Example Waveforms

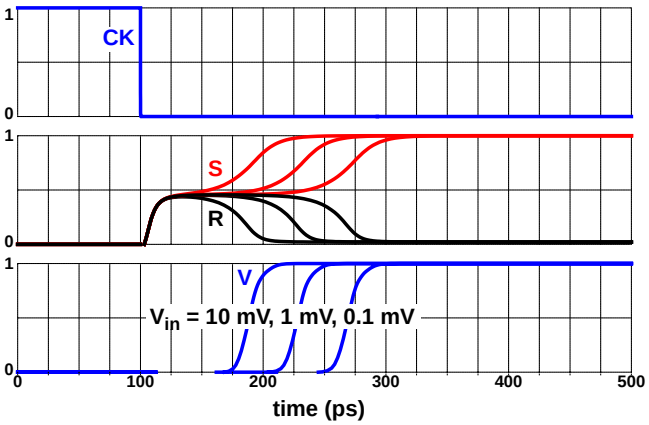
Quick Design in 65nm (VDD = 1V)



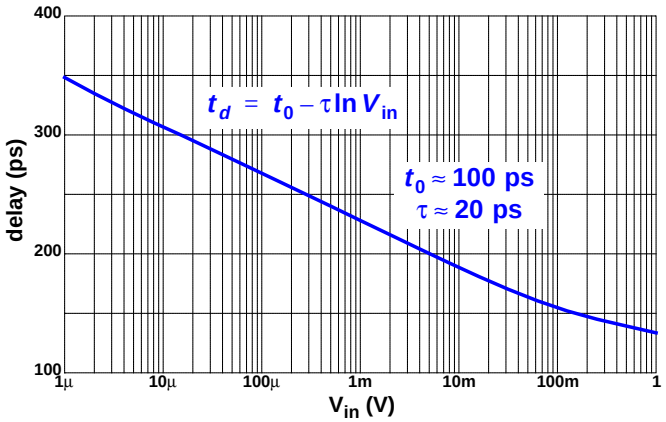
Better Design



Responses for Various V_{in}

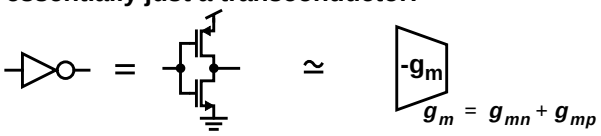


Delay vs. V_{in}

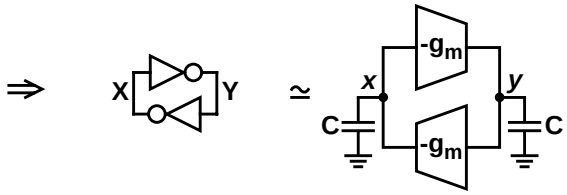


Latch Mode Dynamics

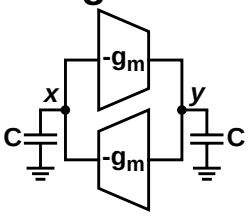
- For V_{in} near the trip point, an inverter is essentially just a transconductor:



- So near balance the comparator looks like this:



Small-Signal Analysis



$$C\dot{x} = -g_m y \qquad C\dot{y} = -g_m x$$

$$v_d = x - y \qquad v_{cm} = \frac{x+y}{2}$$

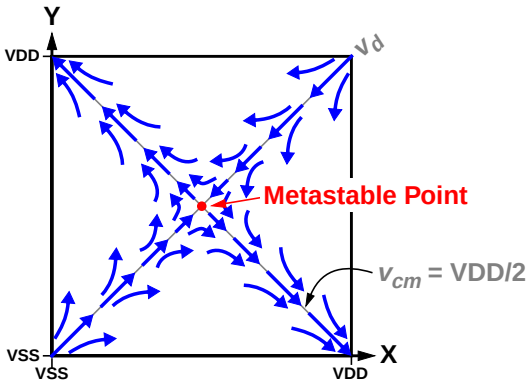
$$C\dot{v}_d = g_m v_d \qquad v_d(t) = v_{d0} e^{t/\tau}$$

$$C\dot{v}_{cm} = -g_m v_{cm} \qquad v_{cm}(t) = v_{cm0} e^{-t/\tau}$$

$$\tau = \frac{C}{g_m}$$

- Differential component grows exponentially
- CM component decays exponentially

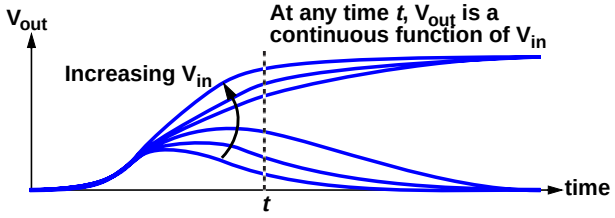
State-Space



- $v_{cm} \rightarrow$ VDD/2, $v_d \rightarrow \pm$VDD

Metastability

- Metastability is fundamentally unavoidable
- Assuming the universe is continuous and deterministic, a comparator can be unresolved for any length of time



Probability of Error, P_E

$$P_E = P\{\text{not resolved by time } t\}$$

$$= P\left\{V_{in} < \exp\left(-\left(\frac{t - t_0}{\tau}\right)\right)\right\}$$

- Take $t_0 = 100$ ps and $\tau = 20$ ps
- Then for $t = 500$ ps (1 GHz clock with a half-cycle between the comparator's clock and the clock of the subsequent latch),

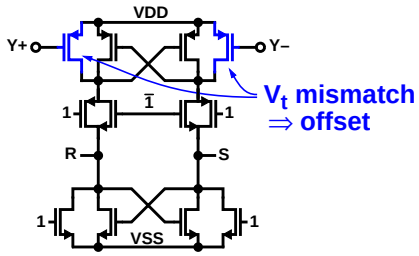
$$P_E = P\{|V_{in}| < 2 \text{ nV}\}$$

- Assuming V_{in} is uniformly distributed in [–0.5, +0.5] V, $P_E = 2 \times 10^{-9}$
  - Metastability occurs twice a second!

Metastability Summary

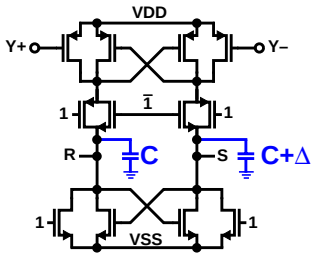
- Metastability is unavoidable
  - All you can do is make τ small and give enough time for regeneration to make P_E small.
- Supplementary Slides examine the effects of quantized charge and noise
  - Noise helps a comparator resolve when $V_{in} = 0$ but usually does not reduce P_E
- At best, metastability causes SNR degradation
  - At worst, it causes a system failure.

Offset



- Obvious sources of offset include mismatch in the input differential pair as well as mismatch in the regenerating devices

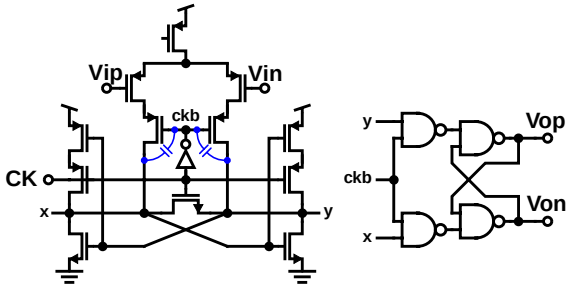
Dynamic Offset



S rises more slowly than R
⇒ offset

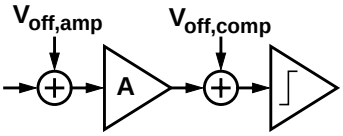
- Mismatched parasitic capacitance also causes offset
  - 20 mV/fF for this comparator!
- Bad design– Can fix this!

Improved Comparator
[S&T Fig. 9.36]



- Reset when CK = 1; regenerates when CK = 0
- x & y don't step if biased properly
  - Mismatch in overlap capacitance still a problem.

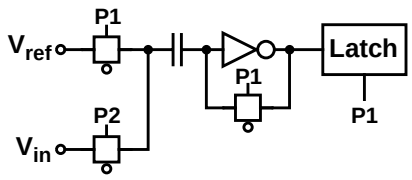
Reducing Offset with a Preamp



$$V_{off,tot} = V_{off,amp} + V_{off,comp}/A$$

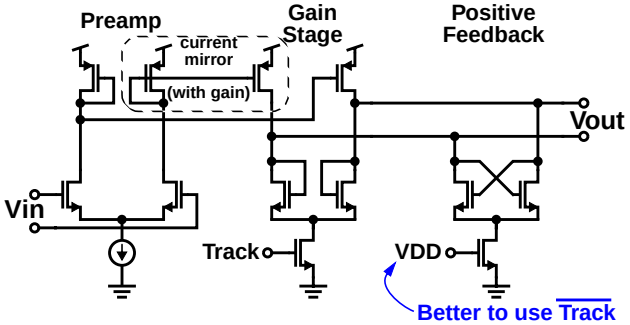
+ Comparator offset is reduced by preamp gain
  - Amplifier offset dominates.
+ Amplifier also isolates driving stage from "charge kickback"
– Amplifier bandwidth limits speed, especially recovery from overload

Auto-zeroed SC Comparator
[J&M Fig 13.17]



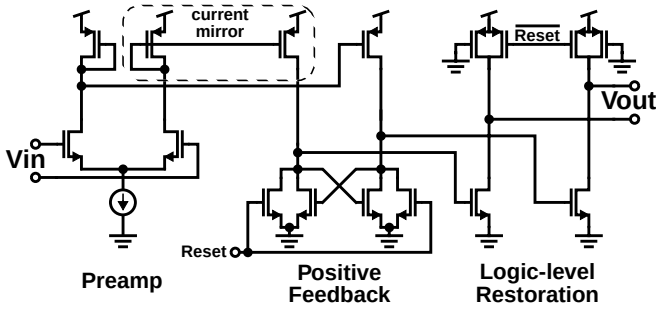
- During P1, the inverter/amplifier is biased at its threshold/offset voltage
- During P2, the difference between V_{in} and V_{ref} is amplified

Comparator with Preamp
[J&M Fig. 7.16]



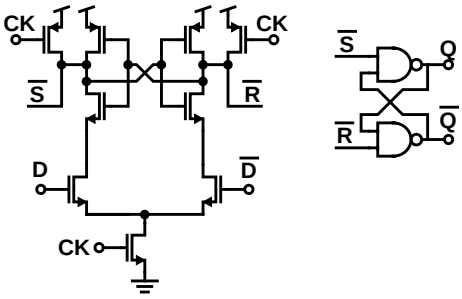
Two-Stage Comparator

[J&M Fig 7.17]



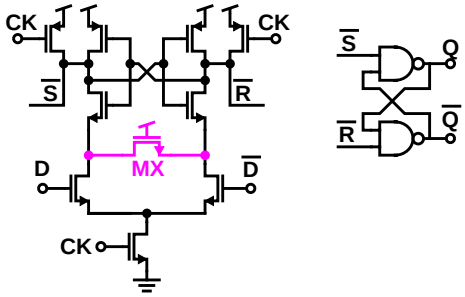
- **Precharges regeneration nodes low & digital output nodes high**

StrongArm Flip Flop



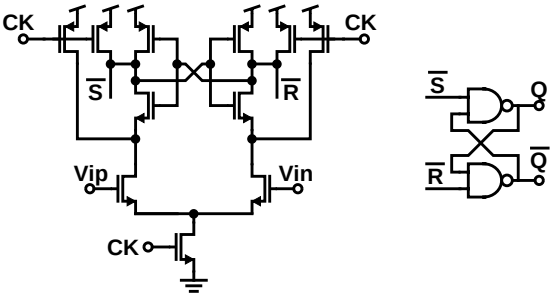
- **+ No static current**
- **+ Can be used as a comparator**
  - **Note that input CM voltage defines the bias point during regeneration.**

Improved StrongArm Design



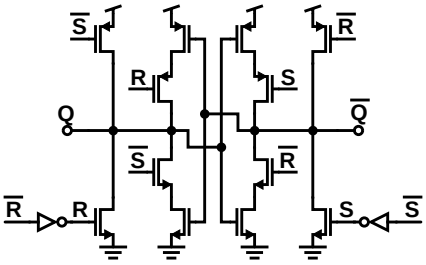
- **MX provides DC path to ground for leakage currents in case D changes after CK goes high**
  - **MX is needed to make latch static.**

Alternative Arrangement



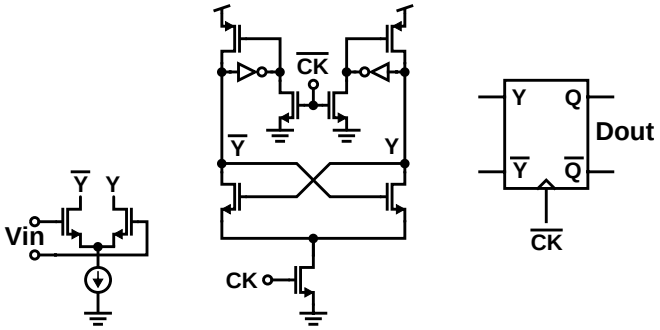
- **Well-defined initial state ⇒ less hysteresis**
  - **[Abidi 2014CICC] "Understanding the Regenerative Comparator Circuit"**

Symmetric Latch



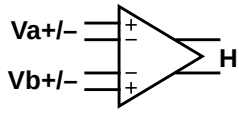
- **Faster than cross-coupled NAND gates**

Yang's High-Speed Comparator

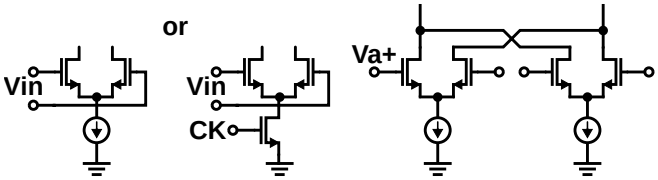


- **τ_{nom} = 6 ps (!) in 65nm CMOS**
  - **Used in a CTΔΣ ADC clocked at 4 GHz [Shibata2012].**

Dual-Difference Comparator

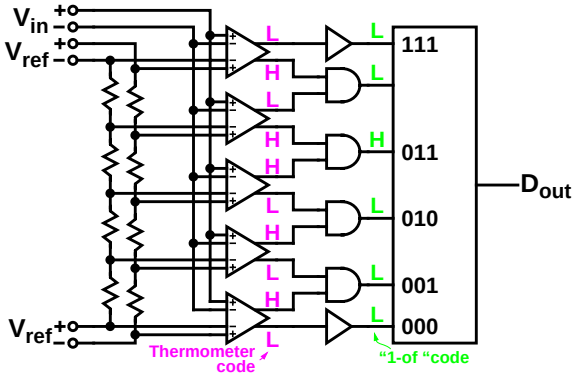


In any of our comparator circuits, replace: with:



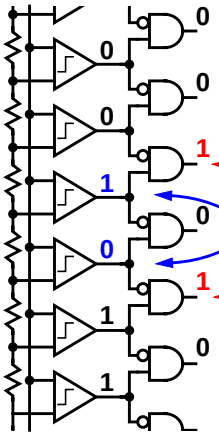
Q: Where should Va– go?

Flash ADC



Resistor String **Comparator Bank** **Decode Logic**

Flash Bubbles



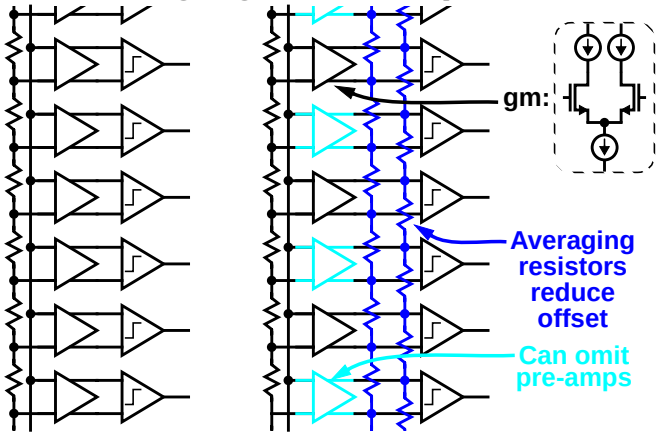
- Need to modify logic to handle bubbles gracefully unless bubbles guaranteed to not occur

Flash Bubble

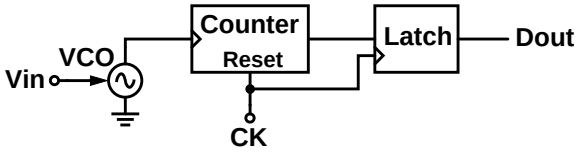
Code Violation

- Counting the number of 1s is the safest method
  - Use a "Wallace-Tree Adder"

Averaging and Interpolation

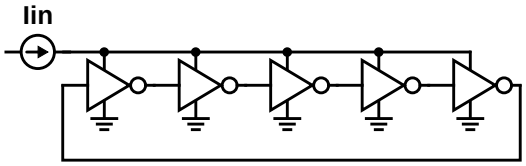


VCO as a Quantizer— Concept



+ Simple
+ Monotonic
– Not linear
– Ill-defined full-scale

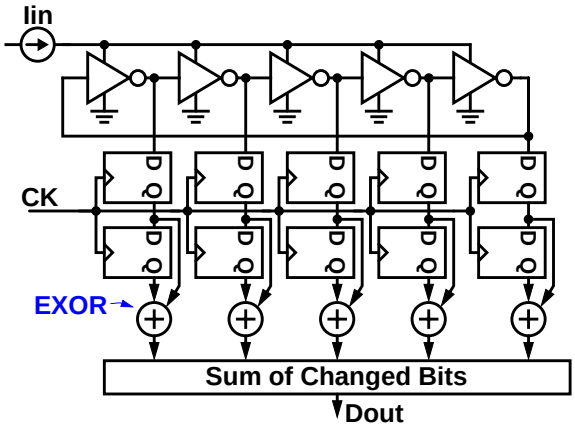
Current-Controlled Ring Oscillator (CCRO)



- Oscillation frequency is proportional to current

⇒ Can make a fairly linear quantizer

CCRO + Phase latch + EXOR = Q!

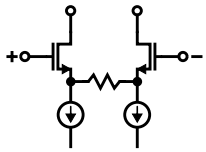


Improvements to CCRO Quantizer

- Put EXOR before 1st FF and remove 2nd FF
  - To eliminate unnecessary delay.
- Add inverters to increase resolution
  - Must keep f_{osc} constant to maintain full-scale.
- Use 2 rings in a pseudo-differential arrangement
  - To cancel even-order distortion and make mid-scale self-referenced.
- Use multiple rings with phase interpolation to increase resolution without hitting f_{osc} ceiling
- Driving the elements of the DACs with the EXOR outputs directly results in *mismatch-shaping*

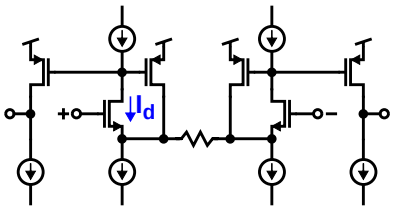
NLCOTD: Linear Transconductors

Degenerated Differential Pair



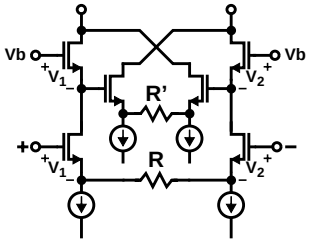
+ Simple!
– V_{gs} varies nonlinearly with $I_{out} \Rightarrow g_m$ is nonlinear

Force Constant V_{gs}



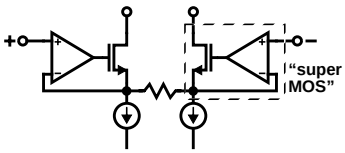
- I_d constant $\Rightarrow V_{gs}$ constant
– Linearity dependent on current-mirror linearity

Cascomp



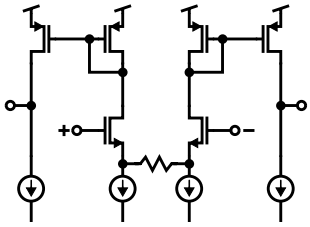
- V_{gs} of input devices replicated in cascodes and distortion-cancelling current injected into output
+ All NMOS $\Rightarrow$ fast
– Cancellation depends on matching
  - Should tie bulk to source?

Add Op Amps



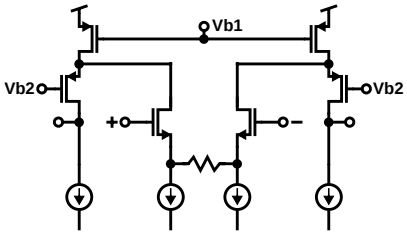
+ Linearity limited only by op amp gain and BW
+ High output resistance
– Output compliance depends on input swing

Mirror the Output Current



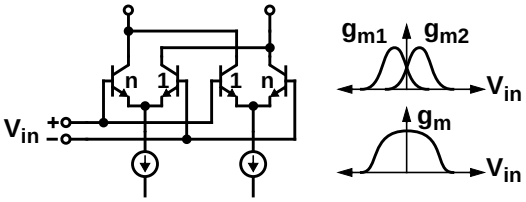
+ Output compliance is VDD – 2 V_{dsat}
– Top of differential pair at VDD – V_{gs}

Fold the Output Current



+ Increased headroom for differential pair
+ Increased output resistance

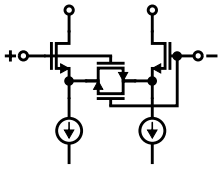
Multi-Tanh Doublet
[Gilbert JSSC Dec. 1998]



- With BJTs, ratioing the emitter areas creates a well-controlled offset
- With the right offset, the cubic term in the nonlinearity is zero!

$$n = 2 + \sqrt{3} = 3.73 \approx 15/4$$

MOS Quad



- Supposedly can get less distortion than a degenerated differential pair by fiddling with W/L

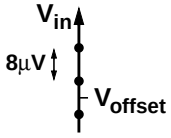
What You Learned Today

1 Operation of Example Comparator Circuit
2 Regeneration Time Constant τ
3 Metastability, Probability of Error
4 Offset, Dynamic Offset, Auto-zeroing
5 Flash ADC
6 A Bunch of Transconductor Circuits

Supplementary Slides
(Regarding Metastability)

Quantized Charge Helps?

- If C = 20 fF, then 1 electron yields 8 μV
- V_{in} = 2 nV and hence metastability impossible?



+ Unless V_{offset} is within 2 nV of one of the discrete V_{in} levels, metastability can't happen
– But if V_{offset} is within 2 nV of an allowed V_{in} level, metastability will be abnormally frequent
- Offset drift will tend to make metastability appear/disappear sporadically (?)

Noise Helps?

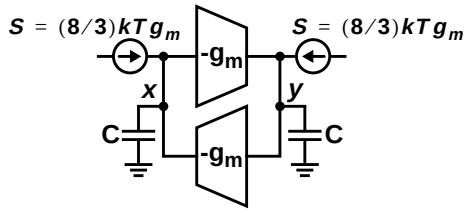
- kT/C = 500 μV, so it is impossible to guarantee that metastability will result even if V_{in} = 0

+ Noise does help a comparator resolve if it is metastable

– But for any given noise (random initial condition), there is always an input which results in metastability

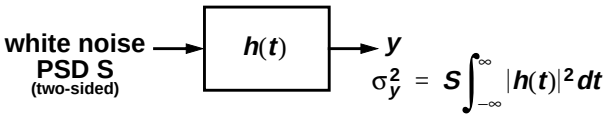
- Noise makes it hard to set initial conditions that will result in metastability, but does not reduce the probability of error

What About Noise During Regeneration?



- Noise from the g_ms prevents metastability?

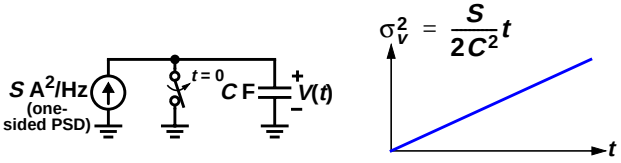
Math Break: Filtered White Noise



- The power of the output is the product of the PSD and the power gain of the filter
- Example: $h(t) = \begin{cases} 1 & 0 \le t \le T \\ 0 & \text{otherwise} \end{cases}$

$\Rightarrow \sigma_y^2 = ST$

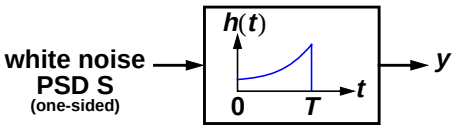
Circuits Application: Integrated White Noise



- Variance of V increases linearly with time
- "Random Walk" or "Brownian Motion"
  For any given increment of time Δt, the change in V is a random variable with constant variance

$\delta(t) \equiv V(t) - V(t-\Delta t) \Rightarrow \sigma_\delta^2 =$ constant

Today's Application



$$h(t) = \begin{cases} e^{t/\tau} & 0 \le t \le T \\ 0 & \text{otherwise} \end{cases}$$

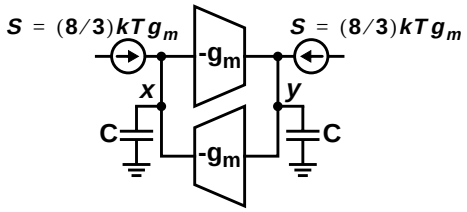
$$\sigma_y^2 = \frac{S\tau}{4}\left(e^{\frac{2T}{\tau}} - 1\right)$$

Another Math Fact: PDF of a Sum

- **Suppose *x* and *y* are two independent random variables with probability density functions (PDFs) $\rho_x(x)$ and $\rho_y(y)$**
- **Then the PDF of their sum is the convolution of the individual PDFs**

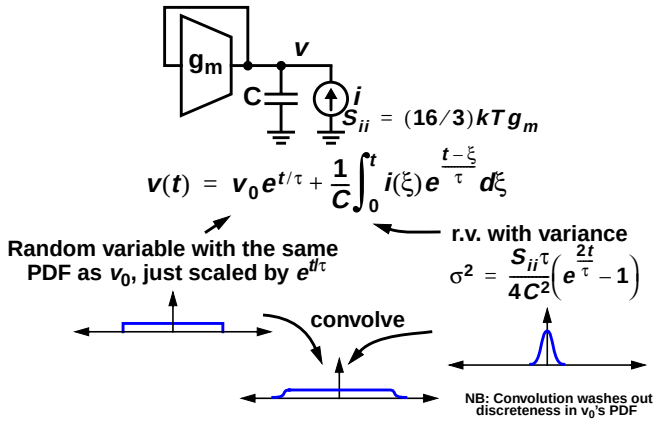
$$z = x + y \Rightarrow \rho_z(z) = \int_{-\infty}^{\infty} \rho_x(x)\rho_y(z-x)\,dx$$

Back to Circuits



- **Noise from the g_ms prevents metastability?**

Differential Circuit



Making Numbers…

- **Assume g_m = 1 mA/V, C = 20 fF, t = 400 ps**
  $\Rightarrow$ τ = 20 ps; 20τ to resolve
- **If v_0 uniformly distributed in [–2,+2] mV, then 1st term is uniformly distributed in [–1,+1] MV**
- **Standard deviation of 2nd term is 250 kV**
  Equivalent to a 0.5-mV initial condition
- **Noise during regeneration helps when the input is known to be small, but is usually negligible compared to the exponential growth of the initial conditions**