ECE1371 Advanced Analog Circuits
Lecture 3

EXAMPLE DESIGN– PART 2

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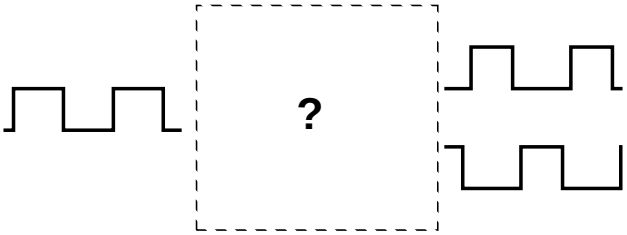
Course Goals

- **Deepen understanding of CMOS analog circuit design through a top-down study of a modern analog system**
  - **The lectures will focus on Delta-Sigma ADCs, but you may do your project on another analog system.**
- **Develop circuit insight through brief peeks at some nifty little circuits**
  - **The circuit world is filled with many little gems that every competent designer ought to know.**

Date	Lecture			Ref	Homework
2008-01-07	RS	1	Introduction: MOD1 & MOD2	S&T 2-3, A	Matlab MOD2
2008-01-14	RS	2	Example Design: Part 1	S&T 9.1, J&M 10	Switch-level sim
2008-01-21	RS	3	Example Design: Part 2	J&M 14	Q-level sim
2008-01-28	TC	4	Pipeline and SAR ADCs		Arch. Comp.
2008-02-04	ISSCC– No Lecture				
2008-02-11	RS	5	Advanced ΔΣ	S&T 4, 6.6, 9.4, B	ΔΣ Toolbox; Proj.
2008-02-18	Reading Week– No Lecture				
2008-02-25	RS	6	Comparator & Flash ADC	J&M 7	
2008-03-03	TC	7	SC Circuits	J&M 10	
2008-03-10	TC	8	Amplifier Design		
2008-03-17	TC	9	Amplifier Design		
2008-03-24	TC	10	Noise in SC Circuits	S&T C	
2008-03-31	Project Presentation				
2008-04-07	TC	11	Matching & MM-Shaping		Project Report
2008-04-14	RS	12	Switching Regulator		Q-level sim

NLCOTD: Non-Overlapping Clock Generator

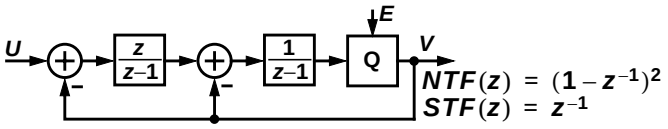
- **Our SC circuits require two non-overlapping clocks. How do we generate them?**



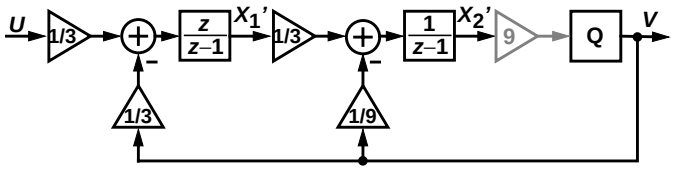
Highlights
(i.e. What you will learn today)

1. **Transistor-level implementation of MOD2**
   - **op-amp, SC CMFB, comparator, clock generator**
2. **MOD2 variants**
3. **Variable quantizer gain**

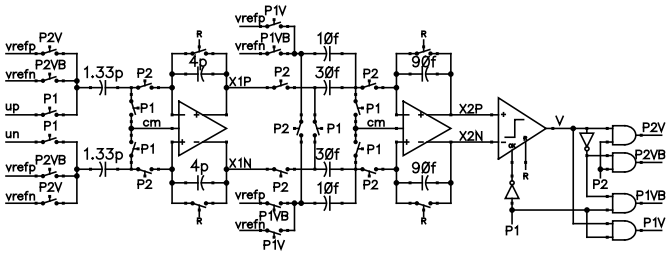
Review: MOD2
Standard Block Diagram



Scaled Block Diagram

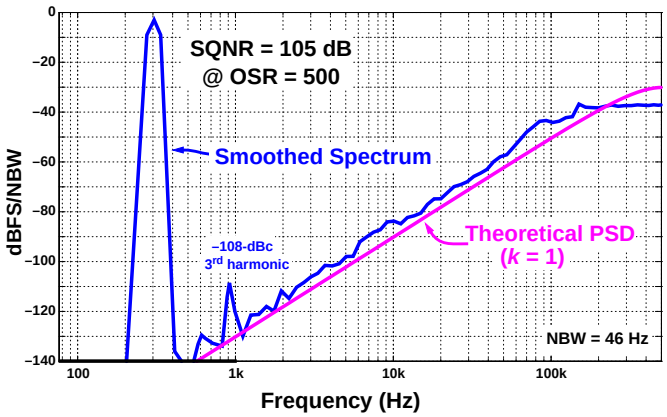


Review: Schematic



- 1st-stage capacitor sizes set for SNR = 100 dB @ OSR = 500 and –3-dBFS input
  - V_{ref} = 1V and the full-scale input range is ±1 V.
- 2nd-stage capacitor sizes set by minimum allowable capacitance

Review: Simulated Spectrum



Review: Implementation Summary

✓ 1 Choose a viable SC topology and manually verify timing

✓ 2 Do dynamic-range scaling

You now have a set of capacitor ratios.

Verify operation.

✓ 3 Determine absolute capacitor sizes

Verify noise.

⋙ 4 Determine op-amp specs and construct a transistor-level schematic

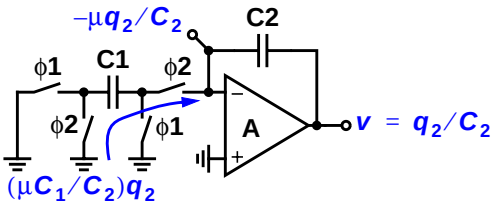
Verify.

5 Layout, fab, debug, document, get customers, sell by the millions, go public, …

Effect of Finite Op Amp Gain

Linear Theory

- Suppose that the amplifier has finite DC gain A. Define $\mu = 1/A$.
- To determine the effect on the integrator pole, let's look at our SC integrator with zero input:



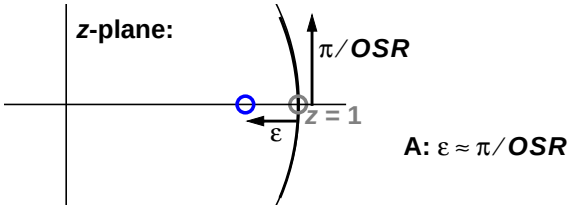
- A fraction of q_2 leaks away each clock cycle:

$$q_2(n+1) = (1-\varepsilon)q_2(n),$$

where $\varepsilon = \mu C_1/C_2$

- Thus, the integrator is lossy, with a pole at $z = 1-\varepsilon$

Q: How big can ε get before the effect becomes significant?



A: $\varepsilon \approx \pi/OSR$

Op Amp Gain Requirement

Linear Theory

- According to the linear theory, finite op amp gain should not degrade the noise significantly as long as

$$A > (C_1/C_2)(OSR/\pi)$$

- For our implementation of MOD2, in which $C_1/C_2 = 1/4$ and $OSR = 500$, this leads to

$$A > 40 = 32 \text{ dB},$$

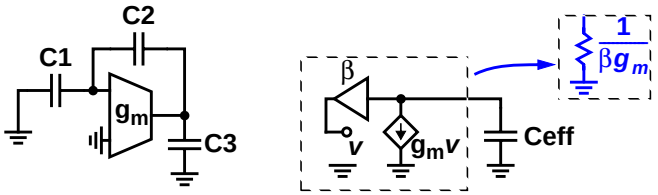
which is quite a lax requirement!

- As OSR is decreased, the gain requirement goes down

Op Amp Transconductance

Settling time

- Model the op amp as a simple g_m:



$$\beta = C_2/(C_1 + C_2)$$

$$C_{eff} = C_3 + C_1C_2/(C_1 + C_2)$$

- This is a single-time-constant-circuit with $\tau = C_{eff}/(\beta g_m)$

Settling Requirements

- If g_m is linear, incomplete settling has the same effect as a coefficient error and thus g_m can be very low
- In practice, the g_m is not linear and we need to ensure nearly complete settling
- As a worst case scenario, let's require transients to settle to 1 part in 10^5
  - This should be more than enough for –100 dBc distortion.

Settling Requirements (cont'd)

- If linear settling is allocated 1/4 of a clock period, we want $\exp\left(-\frac{T/4}{\tau}\right) = 10^{-5}$, or $\tau = \frac{T}{4\ln 10^5} = 20$ ns

  and thus $g_m = \frac{C_{eff}}{\beta\tau} = \frac{C_{eff}}{\beta} 4f_s \ln 10^5$

- For INT1 of our MOD2:

$$C_{eff} = 0.5\left(\frac{4p \cdot 1.33p}{4p + 1.33p} + 30f\right) = 0.5 \text{ pF}^*$$

$$\beta = 3/4$$

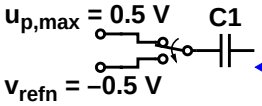
$$f_s = 1 \text{ MHz}$$

$$\Rightarrow \quad g_m = 30\ \mu\text{A/V}$$

*. 0.5 comes from the single-ended to differential translation.

Slewing

- The maximum charge transferred through C1 is

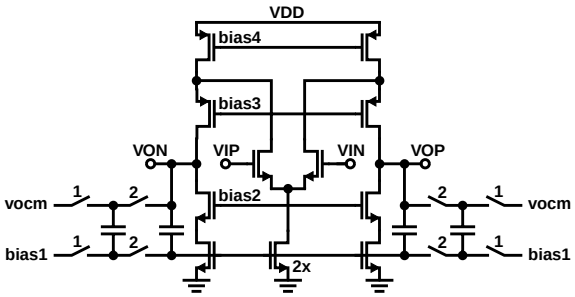


$q_{max} = C_1 \cdot 1\text{V} = 1.33$ pC

- If we require the slew current to be enough to transfer q_{max} in 1/4 of a clock period, then

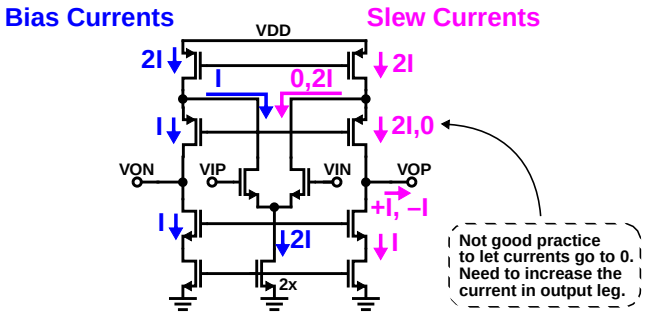
$$I_{slew} = \frac{q_{max}}{T/4} \approx 5\ \mu\text{A}$$

Building Block– Op Amp



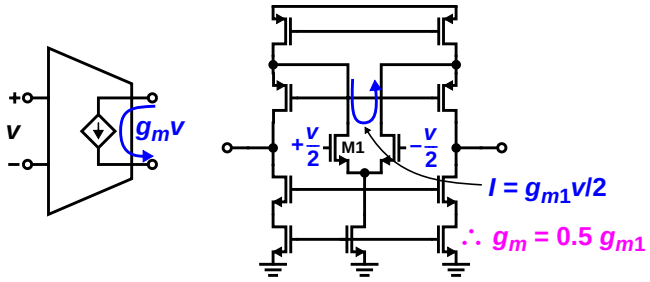
- Folded-cascode op-amp with switched-capacitor common-mode feedback

Op-Amp Design— Bias Current



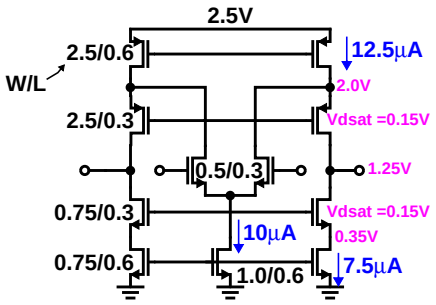
- Slew constraint dictates I >5 μA

Op-Amp Design— gm



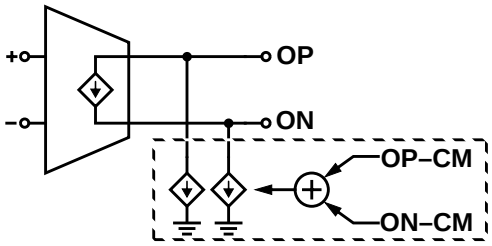
- Square-law MOSFET model: $g_{m1} = (2I_D)/(\Delta V)$
- $I_D = 5\ \mu A$, $g_m \geq 30\ \mu A/V \Rightarrow \Delta V \leq 0.33\ V$
  Usually $\Delta V \approx 200$ mV, so we should be able to get high enough g_m.

Transistor Sizes & Bias Point



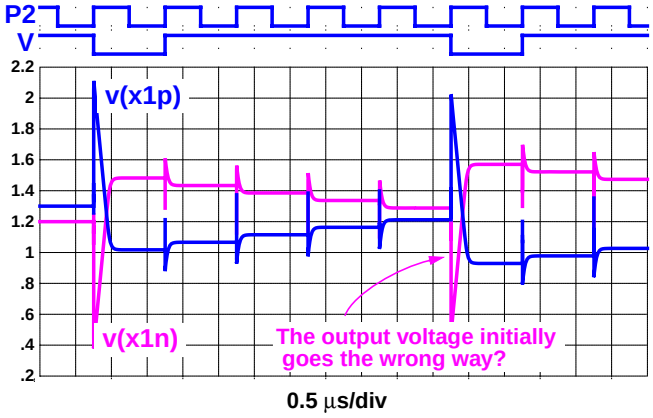
- Allowable swing is +0.6 V, –0.75 V
- Simulated g_m = 36 µA/V, A = 48 dB
  g_m is high enough and the gain is 6× required.

Ideal Common-Mode Feedback

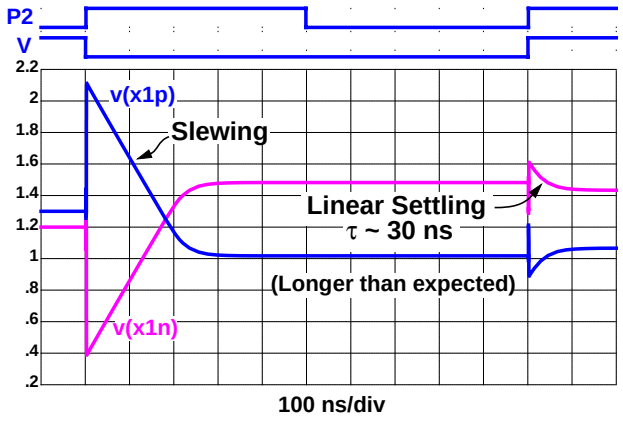


- Can use this circuit to speed up the simulation

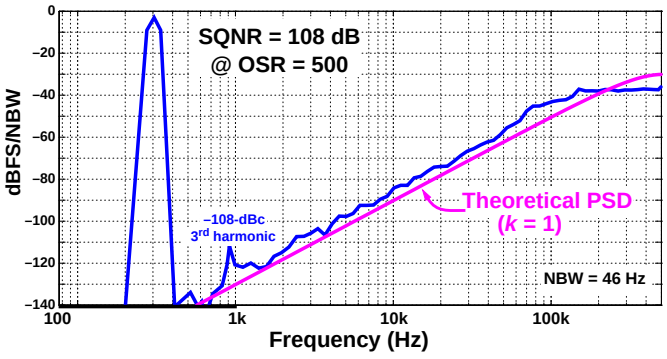
Simulated Waveforms



Expanded Waveforms



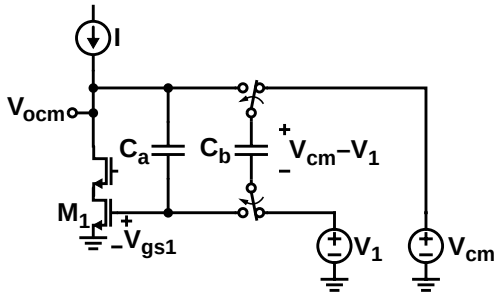
Simulated Spectrum



- This was too easy!
  Although this one simulation *did* take an hour.

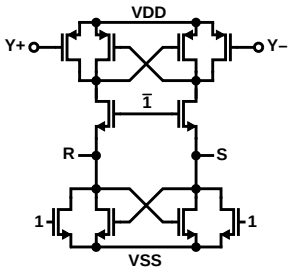
SC Common-Mode Feedback

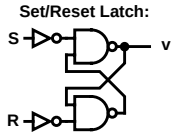
Common-Mode 1/2-Circuit



- $V_{ocm} = V_{cm} + V_{gs1} - V_1$
  If $V_1 = V_{gs1}$, then $V_{ocm} = V_{cm}$.

Latched Comparator



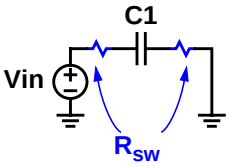


Inverter thresholds are chosen so that the inverters respond only after R/S have resolved.

- Falling phase 1 initiates regenerative action
  S and R connected to a Set/Reset latch.

Switch Resistance

Sampling Phase



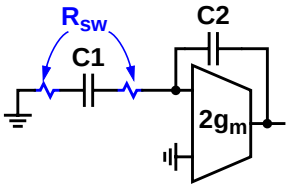
- If R_{sw} is constant, its has only a filtering (linear) effect, which is benign
- Unfortunately, the on-resistance of MOS switches varies with V_{gs} (and hence V_{in})

⇒ Must make MOS switches large enough

Switch Resistance

Integration Phase

Differential Half-Circuit:

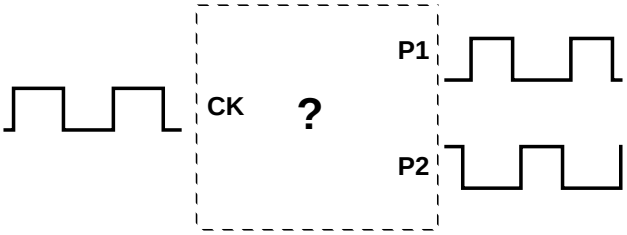


- R_{sw} increases the settling time by a factor of $1 + 4g_mR_{sw}$

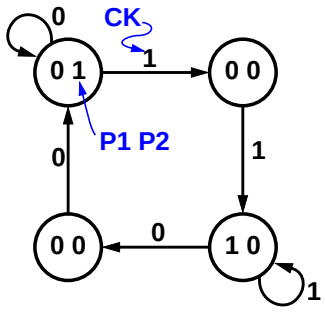
⇒ Set $R_{sw} \le \frac{1}{40g_m}$ to make the increase in τ small

- So in our MOD2, we want $R_{sw} \le 0.75\ k\Omega$.
  BTW, my simulation used $R_{sw} = 1\ k\Omega$ and was OK.

NLCOTD: Non-Overlapping Clock Generator



State Diagram



Truth Table

CK	P1	P2	P1'	P2'
0	0	1	0	1
1	0	1	0	0
1	0	0	1	0
1	1	0	1	0
0	1	0	0	0
0	0	0	0	1

Karnaugh Maps

P1':

CK \ P1P2	00	01	11	10
0	0	0	X	0
1	1	0	X	1

$P1' = CK \cdot \overline{P2}$

$= \overline{\overline{CK} + P2}$

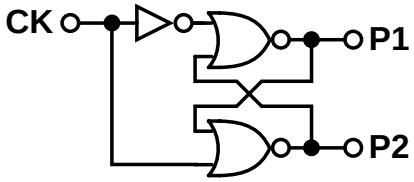
P2':

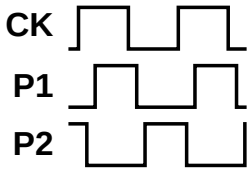
CK \ P1P2	00	01	11	10
0	1	1	X	0
1	0	0	X	0

$P2' = \overline{CK} \cdot \overline{P1}$

$= \overline{CK + P1}$

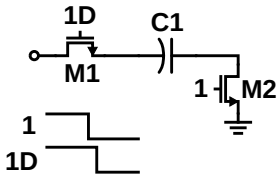
Non-Overlapping Clock Generator





- Non-overlap time set by NOR's t_{PLH}

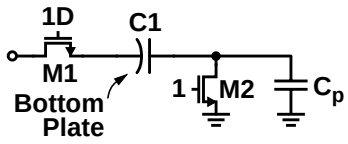
Clocking Details— Early/Late Phases

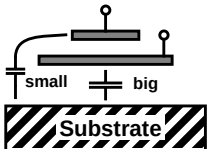


- Charge injected via M1 is (non-linearly) signal-dependent, whereas charge injection from M2 is signal-independent

⇒ Open M2 (early) then open M1 (late) so that charge injected from C_{gs1} cannot enter C1

Clocking Details— Bottom-plate sampling





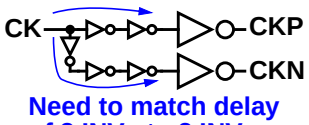
- Parasitic capacitance on the right terminal of C1 degrades the effectiveness of early/late clocking
- C_p for the top plate is smaller, so use the top plate for the right terminal and the bottom plate for the left

Complementary Clock Alignment

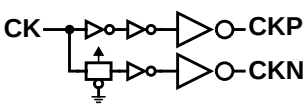
- We need complementary clocks if transmission gates are used for the switches

Q: How do we align them?

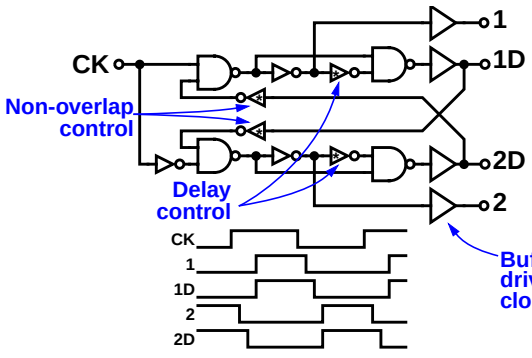
A: Carefully size the inverters relative to their capacitive loads, or use a transmission gate to mimic an inverter delay:



Need to match delay of 3 INVs to 2 INVs



Professional Clock Generator

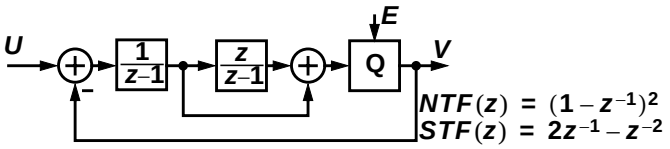


- To maximize the time available for settling, make the early and late phases start at the same time

Review: Implementation Summary

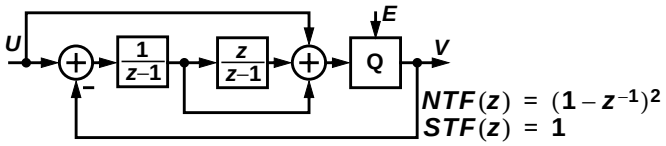
- ✓ 1 Choose a viable SC topology and manually verify timing
- ✓ 2 Do dynamic-range scaling
- ✓ 3 Determine absolute capacitor sizes
- ✓ 4 Determine op-amp specs and construct a transistor-level schematic
  - Verify. Verify. Verify.
- 5 Layout, fab, debug, document, get customers, sell by the millions, go public, …
  - This last step is an "exercise for the reader."

Topological Variant– Feed-Forward



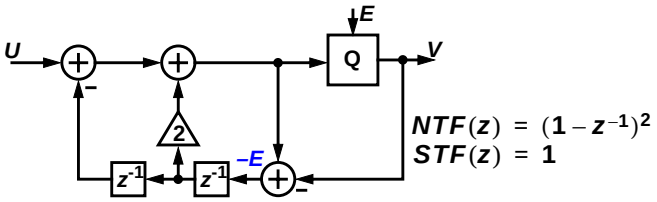
- \+ Output of first integrator has no DC component
  - Dynamic range requirements of this integrator are relaxed.
- – Although $|STF| \approx 1$ near $\omega = 0$, $|STF| = 3$ for $\omega = \pi$
  - Instability is more likely.

Topological Variant– Feed-Forward with Extra Feed-In



- \+ No DC component in either integrator's output
  - Reduced dynamic range requirements in both integrators, esp. for multi-bit modulators.
- \+ Perfectly flat STF
  - No increased risk of instability.
- – Timing is tricky

Topological Variant– Error Feedback



- \+ Simple
- – Very sensitive to gain errors
  - Only suitable for digital implementations.

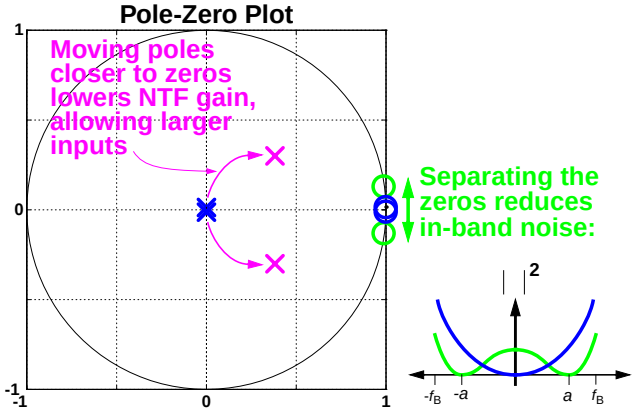
Is MOD2 The Only 2nd-Order Modulator?

- Except for the filtering provided by the STF, any modulator with the same NTF as MOD2 has the same input-output behavior as MOD2
  - SQNR curve is the same.
  - Tonality of the quantization noise is unchanged.
- Internal states, sensitivity, thermal noise etc. can differ from realization to realization

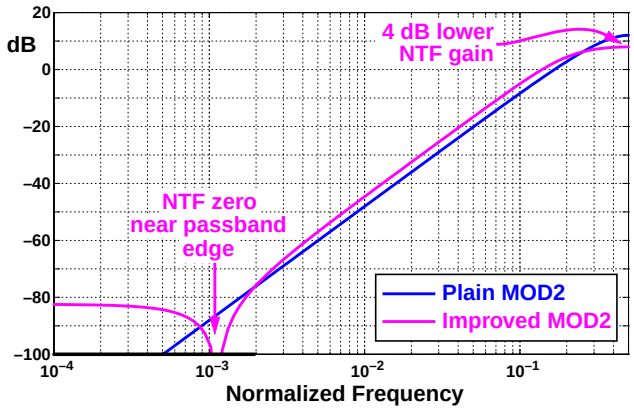
BUT, in terms of input-output behavior,

- A 2nd-order modulator is truly different only if it possesses a truly different (2nd-order) NTF

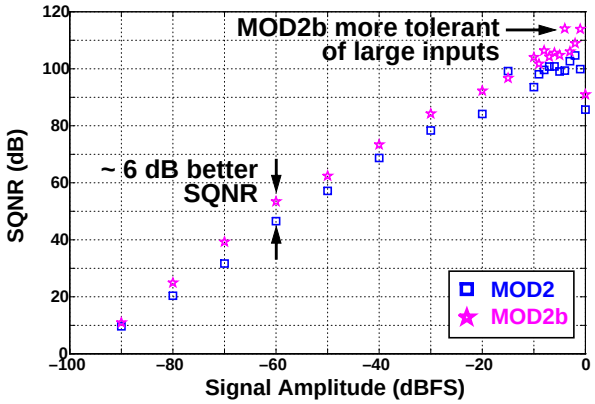
A Better 2nd-Order NTF



NTF Comparison

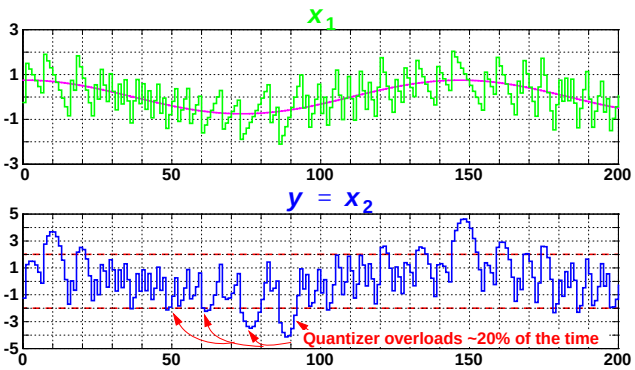


SNR vs. Amp Comparison



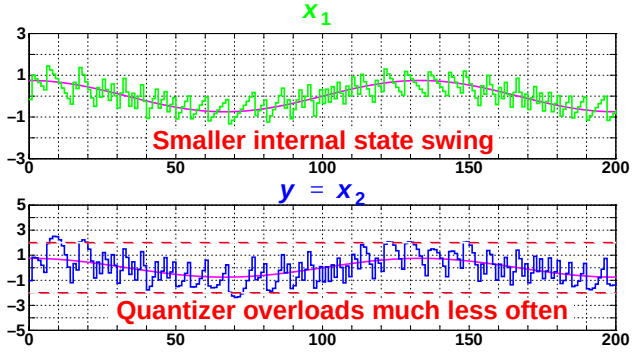
MOD2 Internal Waveforms

Input @ 75% of FS

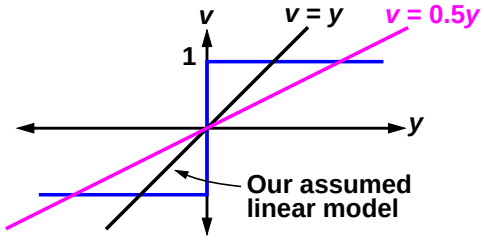


MOD2b Internal Waveforms

Input @ 75% of FS



Gain of a Binary Quantizer



- The effective gain of a binary quantizer is not known a priori
- The gain (k) depends on the statistics of the quantizer's input
  - Halving the signal doubles the gain.

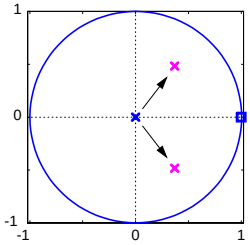
Gain of the Quantizer in MOD2

- The effective gain of a binary quantizer can be computed from the simulation data using

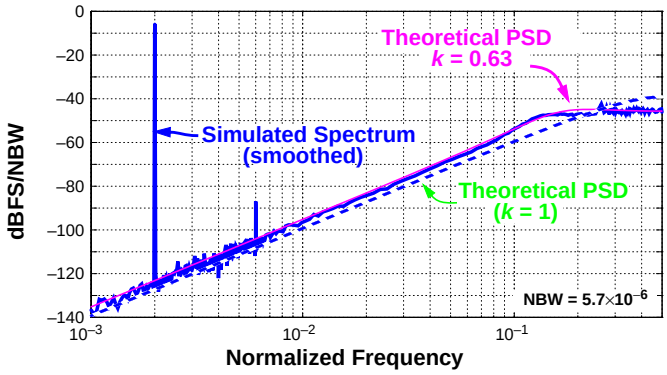
$$k = \frac{E[|y|]}{E[y^2]}$$ [S&T Eq. 2.5]

- For the simulation of 1-35, $k = 0.63$
- $k \neq 1$ alters the NTF:

$$NTF_k(z) = \frac{NTF_1(z)}{k + (1-k)NTF_1(z)}$$



Revised PSD Prediction



- Agreement is now excellent

Variable Quantizer Gain

- When the input is small (below –12 dBFS), the effective gain of MOD2's quantizer is $k = 0.75$
- MOD2's "small-signal NTF" is thus

$$NTF(z) = \frac{(z-1)^2}{z^2 - 0.5z + 0.25}$$

- This NTF has 2.5 dB less quantization noise suppression than the $(1-z^{-1})^2$ NTF derived from the assumption that $k = 1$
  - Thus the SQNR should be about 2.5 dB lower than ✳.
- As the input signal increases, k decreases and the suppression of quantization noise degrades
  - SQNR increases less quickly than the signal power. Eventually the SQNR saturates and then decreases as the signal power reaches full-scale.

Homework #3

1. Design amplifiers for your MOD2 of Homework #2 and verify your ADC. Use f_s = 10 MHz.
   - You may assume ideal comparator, switches, biasing and common-mode feedback.
2. Using your MOD2 model from Homework #1, compute and plot the effective gain of the quantizer as a function of the DC input.
   - Also compare the simulated spectrum for MOD2 with the "predicted" spectrum for a –3-dBFS sine-wave.
3. Bonus: Create a circuit which generates 3 non-overlapping phases of width ~T given a clock of period T. See if you can do the same for a clock of period 2T.
   - Demonstrate that your circuit works in simulation.

What You Learned Today

And what the homework should solidify

1. Transistor-level implementation of MOD2
   - op-amp, SC CMFB, comparator, clock generator
2. MOD2 variants
3. Variable quantizer gain

Op Amp Gain Requirement

Nonlinear Theory 1

- MOD2 has a "deadband" around $u = 0$ whose width is approximately

$$\frac{0.5(a_1c_1)+a_2}{A^2} = \frac{0.5((1/3)\cdot(1/3))+(1/9)}{A^2} = \frac{1}{6A^2}$$

- To make the deadband less than 1 "LSB" wide,

$$\frac{1}{6A^2} < \text{undbv}(-100) = 10^{-5},$$

$$\text{or } A > 400 = 52 \text{ dB}$$

- Since we didn't need so much gain to get excellent AC performance, this calculation looks like it is conservative

Op Amp Gain Requirements

Nonlinear Theory 2

- Finite DC gain ⇒ incomplete charge transfer
- The gain is a nonlinear function, so the residual charge is nonlinearly related to the output voltage of the amplifier
  - The residual charge is akin to noise.
- However, if the amplifier output contains signal components, then nonlinear gain can result in harmonic distortion
  - The feedforward topology is known to yield low distortion even when the amplifier gain is low.
- The effects are difficult to quantify analytically, and so we typically rely on simulations