ECE1371 Advanced Analog Circuits
Lecture 4

PIPELINE AND SAR ADCS

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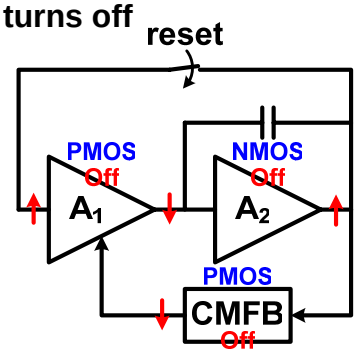
Course Goals

- **Deepen Understanding of CMOS analog circuit design through a top-down study of a modern analog system**
  - **The lectures will focus on Delta-Sigma ADCs, but you may do your project on another analog system.**
- **Develop circuit insight through brief peeks at some nifty little circuits**
  - **The circuit world is filled with many little gems that every competent designer ought to recognize.**

Date	Lecture			Ref	Homework
2008-01-07	RS	1	Introduction: MOD1 & MOD2	S&T 2-3, A	Matlab MOD2
2008-01-14	RS	2	Example Design: Part 1	S&T 9.1, J&M 10	Switch-level sim
2008-01-21	RS	3	Example Design: Part 2	J&M 14, S&T B	Q-level sim
2008-01-28	TC	4	Pipeline and SAR ADCs	J&M 11,13	Pipeline DNL
2008-02-04	ISSCC – No Lecture				
2008-02-11	RS	5	Advanced ΔΣ	S&T 4, 6.6, 9.4, B	ΔΣ Toolbox; Proj
2008-02-18	Reading Week – No Lecture				
2008-02-25	RS	6	Comparator and Flash ADC	J&M 7	
2008-03-03	TC	7	SC Circuits	J&M 10	
2008-03-10	TC	8	Amplifier Design		
2008-03-17	TC	9	Amplifier Design		
2008-03-24	TC	10	Noise in SC Circuits	S&T C	
2008-03-31	Project Presentations				
2008-04-07	TC	11	Matching & MM-Shaping		Project Report
2008-04-14	RS	12	Switching Regulator		Q-level sim

NLCOTD: Startup Circuit

- **Example: Integrator in reset mode**
  - **Output tied to input, 2-stage OpAmp**
  - **If output CM of A_1 is low, output CM of A_2 is high, everything turns off**



How do we keep this from turning off during reset?

Highlights
(i.e. What you will learn today)

1. **Review of ADC performance limitations**

2. **Basic operation of Pipeline ADCs**

3. **Basic operation of Successive Approximation ADCs**

4. **Fundamental trade-offs in ADCs**
   - **Bandwidth, Resolution and Power**
   - **Figures of Merit**

Review

- **Performance Limitations in ADCs**
  - **Offset Error**
  - **Gain Error**
  - **Integral Nonlinearity (INL) Error**
  - **Differential Nonlinearity (DNL) Error**
  - **Sampling Time Uncertainty**
  - **Missing Codes**
  - **Conversion Time and Sampling Rate**

Offset and Gain Errors

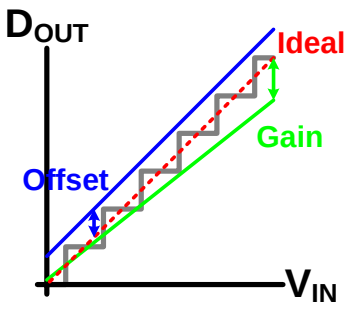
- Look at transition points of input analog voltage
  - $V_{0...01}$ is transition from 0 to 1 in output code

- Offset Error

$$E_{off} = \frac{V_{0...01}}{V_{LSB}} - \frac{1}{2}LSB$$

- Gain Error

$$E_{gain} = \left(\frac{V_{1...1}}{V_{LSB}} - \frac{V_{0...01}}{V_{LSB}} \right) - \left(2^N - 2\right)$$

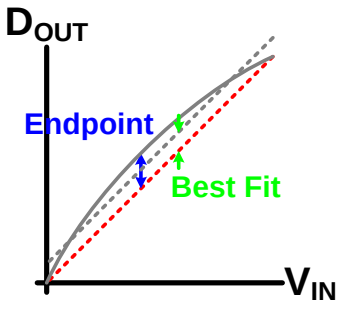


INL and DNL Errors

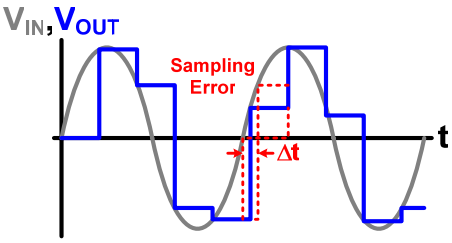
- Remove Offset and Gain errors before finding INL and DNL error

- INL Error
  - Deviation from straight line

- DNL Error
  - Transition values should be 1 LSB apart
  - Error is deviation from 1 LSB
  - Differentiate INL Error



Sampling Time Uncertainty



$$V_{IN} = \frac{1}{2}\sin(2\pi f_{IN} t)$$

- **Error occurs with uncertainty in sampling time**
  - **Worst case at maximum slope of input signal**

$$\left.\frac{\Delta V}{\Delta t}\right|_{max} = \pi f_{IN}$$

  - **For error less than 1 LSB**

$$\Delta t < \frac{1}{2^N \pi f_{IN}}$$

Other Limitations

- **Missing Codes**
  - **Digital output code never occurs**
  - **Guaranteed not to happen if max(DNL) < 1 LSB or max(INL) < 0.5LSB**
- **Conversion Time and Sampling Rate**
  - **Conversion Time: time for a single measurement, includes latency of converter**
  - **Sampling Rate: maximum rate where samples can be continuously converted; not always the inverse of conversion time**

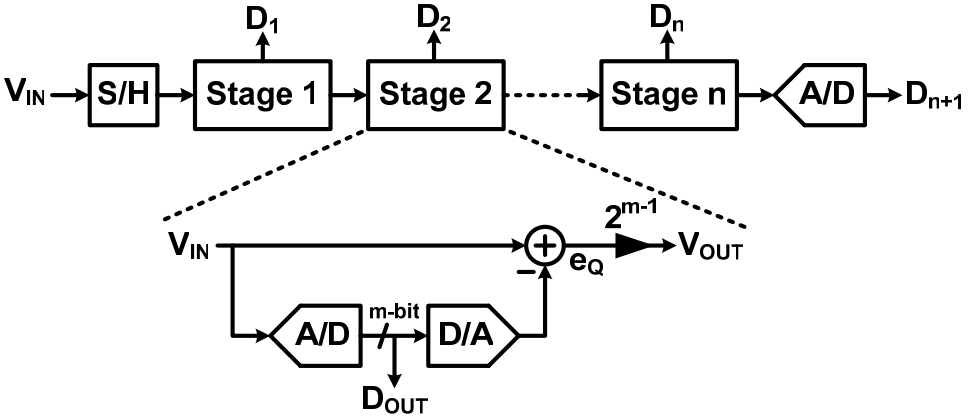
Comparison: Nyquist vs ΔΣ ADCs

- **Larger bandwidth in Nyquist rate ADCs**
  - **Oversampling costs bandwidth, increases accuracy**
- **Nyquist ADC uses entire output spectrum**

- **Noise in ΔΣ primarily important in signal band**
  - **Larger out-of-band shaped noise gets filtered**
- **Nyquist ADC digital output has one-to-one correspondence with a single input value**
  - **ΔΣ ADCs have memory, and the output is not simply a function of a single input**

Pipeline ADC

- **Each stage quantizes the amplified quantization error signal from the previous stage**
- **Higher throughput, lower complexity**



Digital Outputs

- **Binary weight and add digital outputs of each stage**

- **Example: 10-bit ADC**

  8 stages with 1.5-bit per stage, 2-bit final stage

  $D_{1...8}=\{-1,0,1\}$, $D_9=\{-1.5,-0.5,0.5,1.5\}$

  $D_{OUT}=D_1 2^8+D_2 2^7+D_3 2^6+D_4 2^5+D_5 2^4+D_6 2^3+D_7 2^2+D_8 2^1+D_9 2^0$

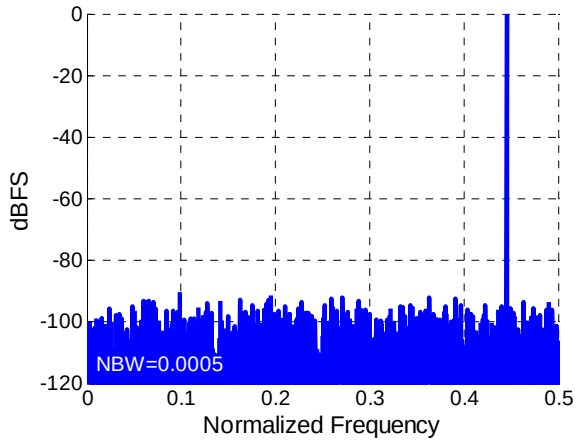
  1024 output levels: 10-bit converter

  1-bit per stage x 8 stages + 2-bit final stage = 10 bits

Sample Output Spectrum

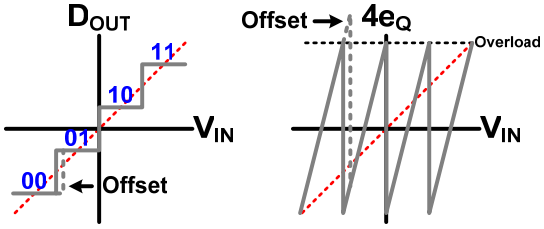
- **What is the SQNR?**

  Rectangular Window, N=2048=2^{11}

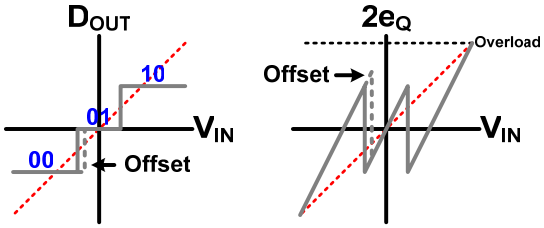


Gain and Quantization

- **Using full range sensitive to offsets in A/D**
  - **Offset saturates input to subsequent stage**



- **Less sensitive to offsets**
  - **Fewer bits/stage, smaller gain to next stage**



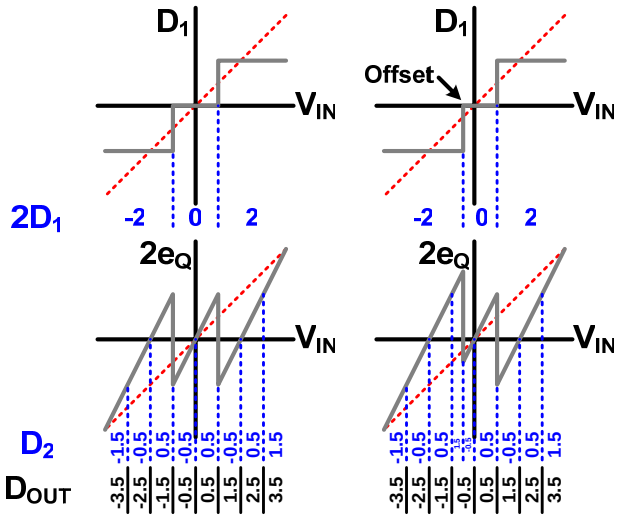
Offset Errors

- **Example: 3-bit ADC**
  1.5-bit stage followed by 2-bit final stage
  - $D_1=\{-1,0,1\}$
  - $D_2=\{-1.5,-0.5,0.5,1.5\}$
  - $D_{OUT}=D_1 2^1+D_2 2^0$

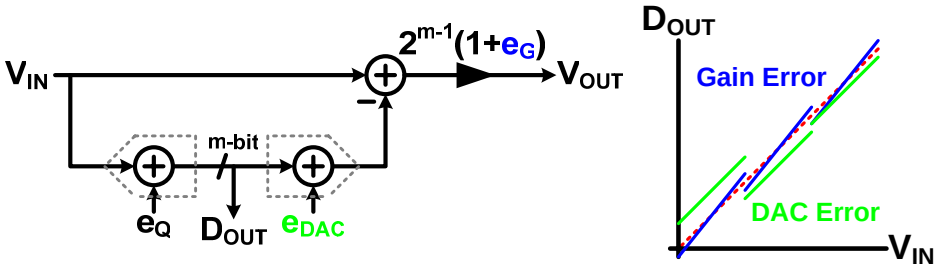
- **With an offset error, the outputs are the same**
  - **Quantization error does not saturate the input to the subsequent stage**

Offset Errors

- Two Cases: No Offset; Offset present



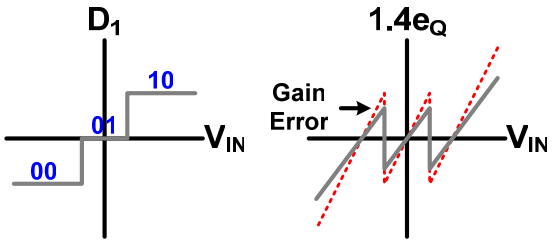
Error Sources



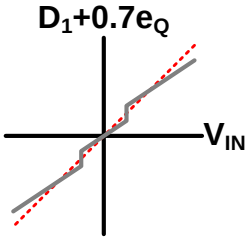
- Sub-ADC error doesn't matter
- DAC error and gain error cause discontinuity in transfer function
  - Signal dependent tones
- In a MASH, they increase noise

Gain Error

- **Example: Assume a gain error of 30%**

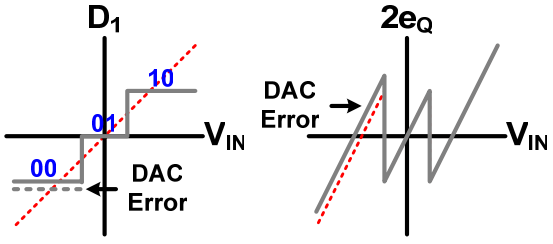


Sum the 2 curves assuming the residue $1.4e_Q$ is quantized perfectly by the later stages

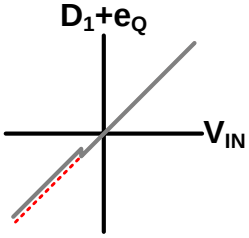


DAC Error

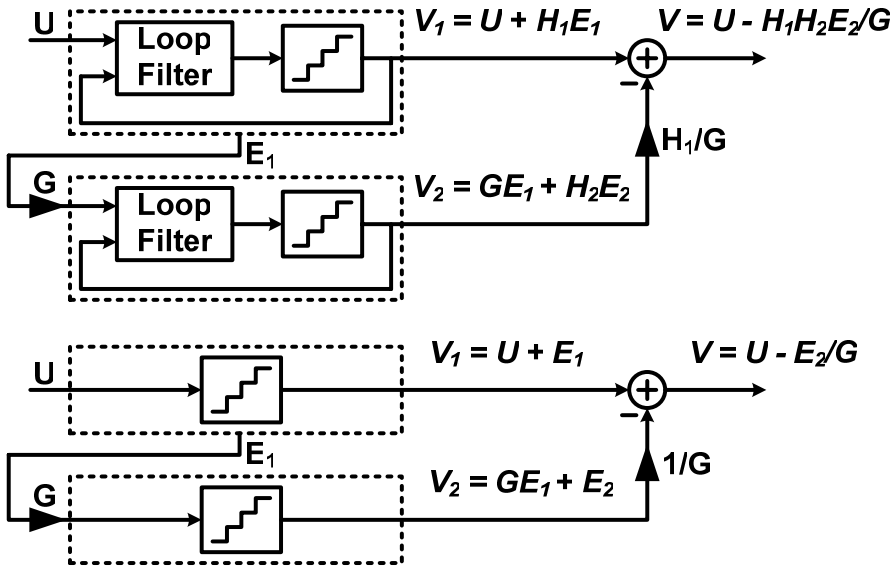
- **Example: Assume a DAC error of ~20%**



Sum the 2 curves assuming the residue is quantized perfectly by the later stages



Pipeline and MASH ΔΣ ADC



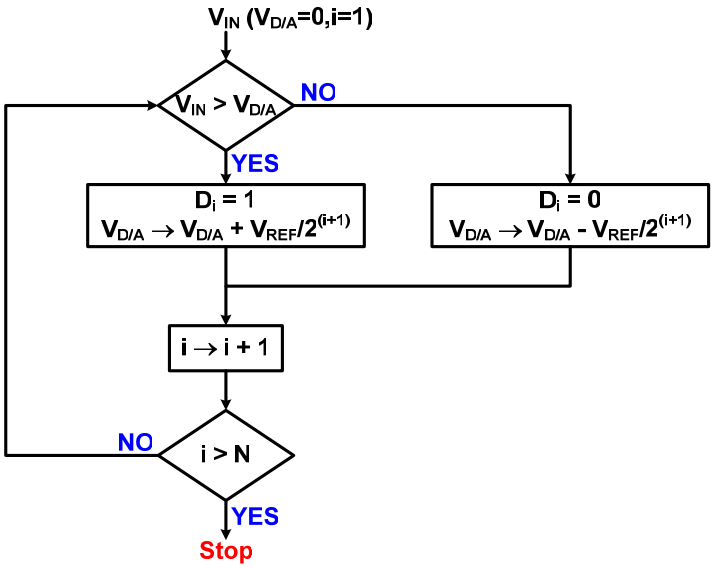
Motivation for SAR ADCs

- Many ADCs sample much faster (>1 MSPS) than needed for many applications
  - Industrial sensors
  - Power line measurements
  - Audio
  - Medical imaging
- Accuracy and power are the next priorities

- SAR ADCs are low power, and like any Nyquist rate ADCs, can be oversampled for improved accuracy

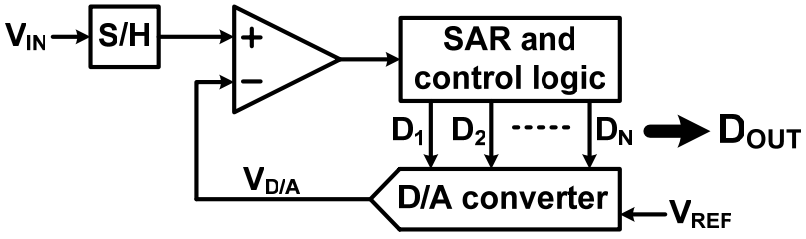
Successive Approximation ADC

- ADC based on binary search algorithm



DAC-based SAR ADC

- How do we implement this algorithm?
  - D_1=1, $D_{2...n}$=0, check $V_{D/A}$ against V_{IN}
  - If $V_{IN} > V_{D/A}$, D_1=1
  - If $V_{IN} < V_{D/A}$, D_1=0
  - Now try D_2=1, carry on…



SAR Advantages

- **Useful for signals from 1 Hz to 1 MHz**
  - **Internal clock must be faster than signal depending on the resolution**
- **Very accurate and power efficient**
  - **Less power with same resolution and bandwidth than other converters (see ISSCC)**
- **Does not need internal OpAmps**
  - **Only uses a single comparator**
- **Lower kT/C noise**
  - **No input referred noise from other stages**

SAR Algorithm

- **Algorithm finds largest DAC value less than V_{IN}**
- **Every single bit acquired must be accurate to the resolution of the system**
  - **DAC linearity**
  - **Comparator Offset**
  - **S/H offset and linearity**
- **Comparator must respond to large changes**
  - **Large overdrive to 0.5 LSB in a single bit cycle period**

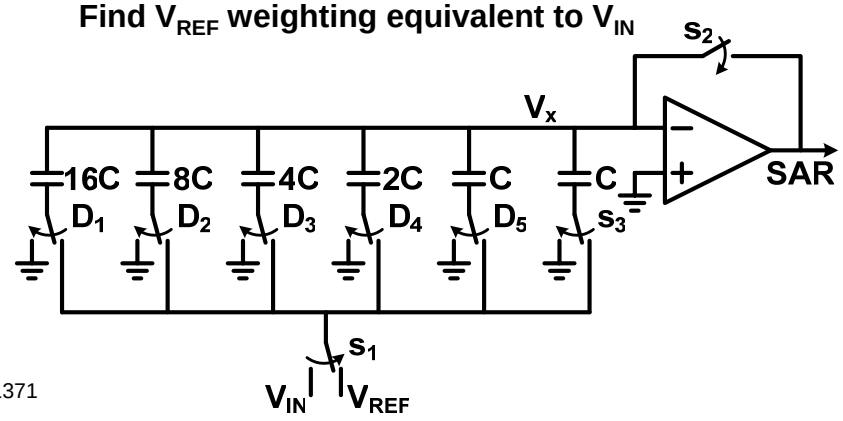
SAR Algorithm

- **Bandwidth limitation**
  For N-bit resolution, N bit cycles are required, reducing the effective sampling frequency by N

- **Comparison nodes must be quiet before comparator triggers**

Unipolar Charge-Redistribution SAR

1. **Charge all caps to V_{IN} (s_2 on; s_1,s_3 off)**
2. **Switch caps to ground, V_x=-V_{IN} (s_3 on; s_1,s_2 off)**
3. **Switch s_1 to V_{REF}, start bit cycling**
   Switch D_1 to V_{REF}, if V_x negative then keep D_1 at V_{REF}
   Find V_{REF} weighting equivalent to V_{IN}

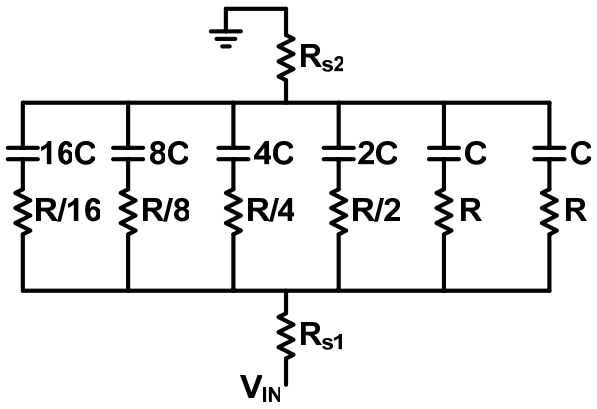


Unipolar Charge-Redistribution SAR

- Extra capacitor C required for exact divide by 2
- DAC capacitor array serves as Sample-and-Hold
- Switching sequence is parasitic insensitive
  - Parasitic capacitors attenuate the signal on V_x
  - Better to keep capacitor bottom plates on the V_{REF} side (not the comparator side)
- Signed conversion with added $-V_{REF}$ input
  - If $V_x < 0$ on step 2, proceed with V_{REF}
  - If $V_x > 0$ on step 2, use $-V_{REF}$, opposite comparison

Speed Estimate of SAR

- Model RC network when V_{IN} is charged
  - Replace switches with R's
  - Assume switches are sized proportional to capacitors



Speed Estimate of SAR

- **Speed limited by RC time constant of capacitor array and switches**

$$\tau_{eq} = (R_{s1} + R_{s2} + R/2^N)2^N C$$

For better than 0.5 LSB accuracy

$$e^{-T/\tau_{eq}} < \frac{1}{2^{N+1}}$$

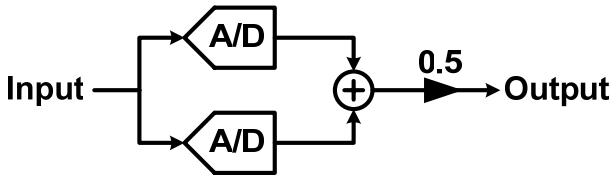
Sets minimum value for the charging time T

$$T > 0.69(N+1)(R_{s1} + R_{s2} + R/2^N)2^N C$$

What are the Fundamental Trade-offs among BW, DR and P?

DR-P Trade-Off: Part 1

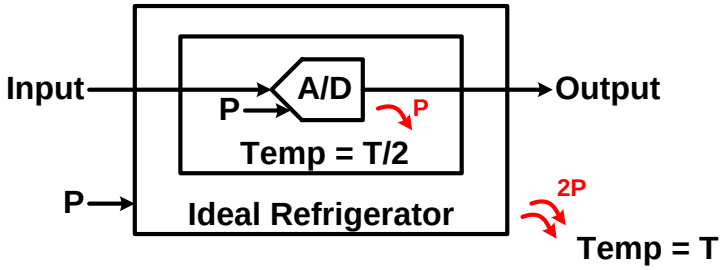
- To increase DR at the expense of P, parallel two ADCs and average:



- Reduces noise by a factor of √2 : DR ↑ 3 dB, but uses twice the power: P ↑ 3 dB
  - Assumes arithmetic requires no power, noise sources are uncorrelated and the source can drive two ADCs.

DR-P Trade-Off: Part 1b

- Can increase DR by 3 dB by reducing T by a factor of 2:



- But this also costs twice the power (based on thermodynamics)

DR-P Trade-Off: Part 2

- **To reduce P at the expense of DR, "cut the ADC in half"**
  - **May not be practical if the ADC is already small, but if it can be done, P ↓ 3 dB & DR ↓ 3 dB**
- **∴ For an ADC of some BW**

X dB in DR costs X dB in P,

or

DR (in dB) – 10log10(P) is a constant

Q: Is This Trade-Off Optimal?

- **A: Yes, because it is bi-directional**
  - **The fact that you can (in principal) go both ways for any ADC means that no other trade-off can exist for ADCs that are optimal.**
- **Consider a (supposedly) optimal ADC that can get more than 3 dB increase in DR for a doubling of P**
  - **Double P, then cut that ADC in half.**
  - **The resulting ADC has the same P as the original, but more DR.**

What About BW?

- **Reducing BW by a factor of 2 increases DR by 3 dB but leaves P alone**
  - **Assuming the noise is white (distortion is not dominant) and that digital filtering takes no power.**
- **Time-interleaving two ADCs doubles BW and doubles P, but leaves DR unchanged**
  - **Assumes that interleaving is perfect (can be calibrated with no extra power).**
  - **I/Q processing also doubles BW & P @ same DR.**
- **In these examples,**

  DR (in dB) + 10log10(BW/P) is a constant

Resulting FOM

$$FOM = (DR)_{dB} + 10\log_{10}\frac{BW}{P}$$

- **For a given FOM, factors of 2 in BW or P are equivalent to a 3 dB change in DR**

- **Should really include T, but since T is usually assumed to be 300K, omit it**
  - **Steyaert et al.** $FOM = \frac{4kT \cdot DR \cdot 2BW}{P}$

Oversampled vs. Nyquist Rate

- For switched-capacitor design, assume power is dominated by kT/C noise
- Assume power is dominated by 1st stage
  - In $\Delta\Sigma$ ADCs, this is usually more accurate
  - In Pipeline ADCs, more noise is from the later stages
- Which is more power efficient?
  - For the same resolution and speed, oversampled operates N times faster, capacitor is N times smaller
  - $\therefore$ Power is the same
  - It is the 'little things' (biasing, clocks, stage sizing, OpAmp gain, architecture) that make a big difference

Common FOM

$$FOM = \frac{P}{2BW \cdot 2^{ENOB}}$$

- Units of Joules per Conversion Step
  - P in J/s, BW in 1/s, 2^{ENOB} in conversion steps
- Fundamentally incorrect:
  1 extra bit costs 2x P, instead of 4x P
  - 1 extra bit means noise is reduced by 6dB, which requires 4 parallel ADCs, not 2
- Favours lower resolution ADCs

Common FOM

- **Example: OTA dominated by thermal noise**

  SNR = Signal Power / Noise Power

  Reduce noise power by 6 dB to get 1 more bit

  Noise Power proportional to 1/C

  To reduce noise power by 6 dB, or 4x, we need to increase C by 4

  Keep V_{EFF} and BW (g_m/C) constant

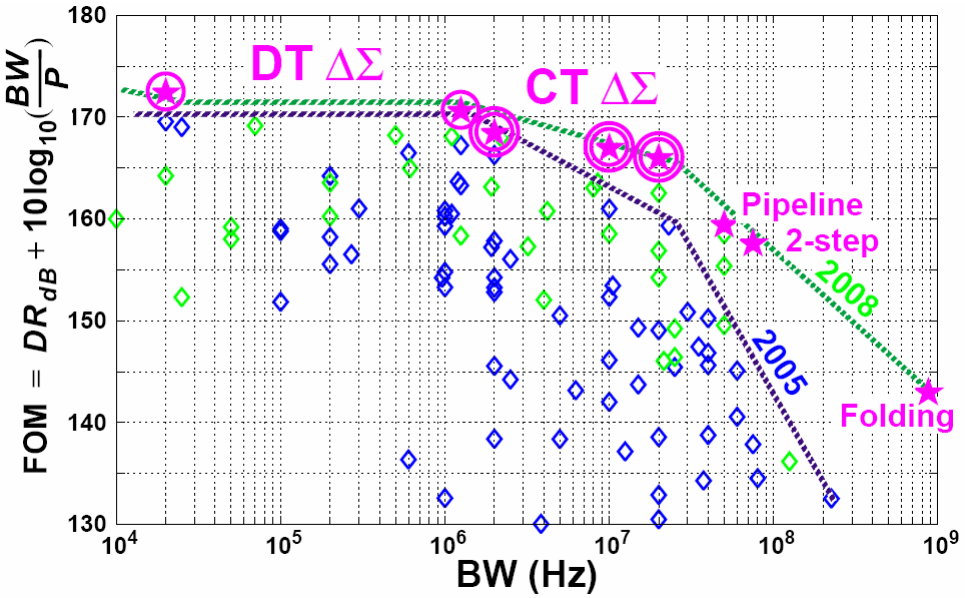
  Increase I_D and W by 4 (like 4 OTAs in parallel)

  OTA power increased by 4

  $\therefore$ 4x power required for 1 extra bit

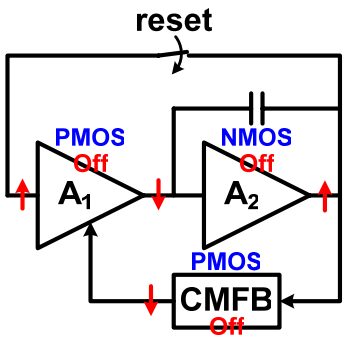
  Inconsistent with 'Common FOM'

FOM vs. BW



NLCOTD: Startup Circuit

How do we keep this from turning off during reset?



Homework

1. **Determine analytically the allowable gain error for the 1st-stage of a 1.5 bit/stage 10-bit pipeline ADC so that the DNL error is less than**
   - **a) 2 LSB**
   - **b) 0.5 LSB**

Now simulate the pipeline in MATLAB to do the following:

2. **Plot the DNL error for both cases.**
3. **Plot the output spectrum for both cases with a full-scale sine wave input.**
4. **What is the SNDR and what did you expect it to be for both cases?**

What You Learned Today

1. **ADC performance limitations**

2. **Basic operation of Pipeline and Successive Approximation ADCs**

3. **Gain Errors in Pipeline ADCs (Homework)**

4. **Fundamental trade-offs between BW, DR and P and ADC FOMs**

Projects (1)

List of ΔΣ projects…

(Choose OSR, order, cascaded/single-loop)

- **40MS/s 12-bit ΔΣ Modulator**
- **2.2MS/s 14-bit ΔΣ Modulator**
- **24kS/s 18-bit ΔΣ Modulator**

List of Pipeline projects…

- **50MS/s 14-b Pipeline ADC**
- **200MS/s 10-b Pipeline ADC**

Projects (2)

More interesting projects…

- **25MS/s, 5th-order, 14-b ΔΣ Modulator**

  Balmelli, JSSC Dec. 2004 (OSR=8,f_S=200MHz)

- **22-bit incremental (resetting ΔΣ) ADC**

  Quiquempoix, JSSC July. 2006 ('OSR'=2048, 15 S/s)

- **13-b Audio ΔΣ using Switched-RC integrators**

  Ahn, JSSC Dec. 2005 (OSR=64,f_S=3.1MHz, 0.6V supply)

- **10-b 200MS/s Pipeline ADC with amplifier sharing**

  Kurose, JSSC July. 2006 (two channels, I & Q)

Projects (3)

High-Speed Continuous-Time ΔΣ projects…

- **640MHz, 12-bit, continuous-time ΔΣ**

  Mitteregger, JSSC Dec. 2005 (OSR=16, 3rd-order)

- **300MHz, 11-bit, continuous-time ΔΣ**

  Paton, JSSC July 2004 (OSR=10, 4th-order)

Other projects…

Feel free to propose projects for approval.