ECE1371 Advanced Analog Circuits
Lecture 7

SWITCHED CAPACITOR CIRCUITS

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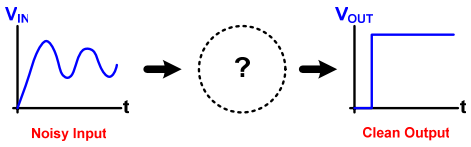
Course Goals

- Deepen Understanding of CMOS analog circuit design through a top-down study of a modern analog system
  - The lectures will focus on Delta-Sigma ADCs, but you may do your project on another analog system.
- Develop circuit insight through brief peeks at some nifty little circuits
  - The circuit world is filled with many little gems that every competent designer ought to recognize.

Date	Lecture			Ref	Homework
2008-01-07	RS	1	Introduction: MOD1 & MOD2	S&T 2-3, A	Matlab MOD2
2008-01-14	RS	2	Example Design: Part 1	S&T 9.1, J&M 10	Switch-level sim
2008-01-21	RS	3	Example Design: Part 2	J&M 14, S&T B	Q-level sim
2008-01-28	TC	4	Pipeline and SAR ADCs	J&M 11,13	Pipeline DNL
2008-02-04	ISSCC – No Lecture				
2008-02-11	RS	5	Advanced ΔΣ	S&T 4, 6.6, 9.4, B	CTMOD2; Proj.
2008-02-18	Reading Week – No Lecture				
2008-02-25	RS	6	Comparator and Flash ADC	J&M 7	
2008-03-03	TC	7	SC Circuits	Raz 12, J&M 10	
2008-03-10	TC	8	Amplifier Design		
2008-03-17	TC	9	Amplifier Design		
2008-03-24	TC	10	Noise in SC Circuits	S&T C	
2008-03-31	Project Presentations				
2008-04-07	TC	11	Matching & MM-Shaping		
2008-04-14	RS	12	Switching Regulator		Project Report

NLCOTD: Schmitt Trigger

Problem: Input is noisy or slowly varying



How do we turn this into a clean digital output?

Highlights
(i.e. What you will learn today)

1. Motivation for SC Circuits
2. Basic sampling switch and charge injection errors
3. Fundamental SC Circuits
   - Sample & Hold, Gain and Integrator
4. Other Circuits
   - Bootstrapping, SC CMFB

Why Switched Capacitor?

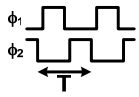
- Used in discrete-time or sampled-data circuits
  - Alternative to continuous-time circuits
- Capacitors instead of resistors
  - Capacitors won't reduce the gain of high output impedance OTAs
  - No need for low output impedance buffer to drive resistors
- Accurate frequency response
  - Filter coefficients determined by capacitor ratios (rather than RC time constants) and clock frequencies
  - Capacitor matching on the order of 0.1% - when the transfer characteristics are a function of only a capacitor ratio, it can be very accurate
  - RC time constants vary by up to 20%

Basic Building Blocks

- **Opamps**
  - Ideal usually assumed
  - Some important non-idealities to consider include:
    1. DC Gain: sets the accuracy of the charge transfer, how 'grounded' the virtual ground is
    2. Unity-gain freq, Phase Margin & Slew Rate: determines maximum clock frequency
    3. DC Offsets: circuit techniques to combat this and 1/f noise – Correlated Double Sampling, Chopping
- **Capacitors**
  - Large absolute variation, good matching
  - Large bottom plate capacitor adds parasitic cap

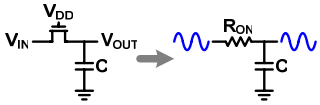
Basic Building Blocks

- **Switches**
  - MOSFET switches are good – large off resistance (GΩ), small on resistance (100Ω - 5kΩ, depending on transistor sizing)
  - MOSFET switches have non-linear parasitic capacitors
- **Non-Overlapping Clocks**
  - Clocks are never on at the same time
  - Required so that charge is never lost/shared
  - Clock Generator previously discussed

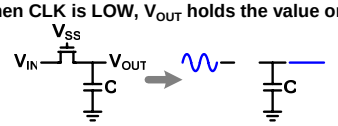


Basic Sampling Switch

- **MOSFET used as sample-and-hold**
  - When CLK is HIGH, V_{OUT} follows V_{IN} through the low-pass filter created by R_{ON} and C
  - R_{ON} varies depending on V_{IN}, V_{OUT}, and V_{DD}



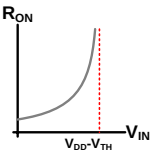
  - When CLK is LOW, V_{OUT} holds the value on C



On-Resistance Variation

- **With an NMOS sampling switch, as V_{IN} approaches V_{DD}-V_{TH}, R_{ON} increases dramatically**
  - In smaller technologies, as V_{DD} decreases the swing on V_{IN} is severely limited

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{IN} - V_{TH})}$$

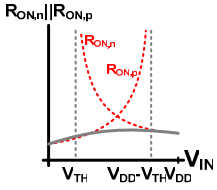


  - Sampling switch must be sized for worst case R_{ON} so that the bandwidth is still sufficient

On-Resistance Variation

- **PMOS switches suffer from the same problem as V_{IN} approaches V_T**
- **Complementary switch can allow rail-to-rail input swings**
  - Ignoring variation of V_{TH} with V_{IN}, $R_{ON,eq}$ is constant with V_{IN} if

$$\mu_n C_{ox} \frac{W}{L} = \mu_p C_{ox} \frac{W}{L}$$



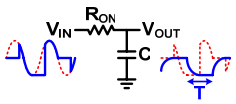
Settling Accuracy

- **Two situations to consider**
  - 1) Discrete-time signal
    - When analyzing a signal within the switched-capacitor circuit (for example, at the output of the first OTA)
  - 2) Continuous-time signal
    - When analyzing a signal that is sampled at the input

Settling Accuracy – DT

- **Discrete-Time Signal**
  - Settling Error = $e^{-T/4RC}$
  - For N-bit accuracy in T/4 seconds

$$R_{ON}C < \frac{T}{4N\ln 2}$$



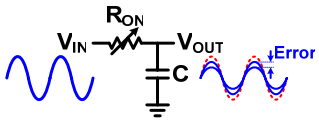
  - This is the maximum R_{ON} (for a given C)
- **Example:**
  - Assume 1 GHz to 4 GHz variation of $\frac{1}{2\pi R_{ON}C}$
  - Input sinusoidal signal at 50 MHz
  - For f_S=100MHz, N=22 bits with discrete-time signal (typically you are limited by the OTA)

Settling Accuracy – CT

- **Continuous-Time Signal**
  - $R_{ON}C$ acts as a low-pass filter and introduces amplitude and phase change
  - Variations in the input signal size cause variations in R_{ON}, causing distortion in the sampled signal
  - Both the amplitude and phase vary – which one causes distortion?

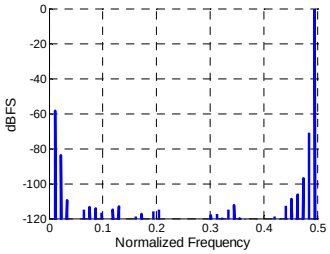
Amplitude Error

- **Less significant error**
  - Due to variation in magnitude of low-pass filter
  - At 50 MHz (with same $R_{ON}C$ variation as DT case), maximum possible error is 0.1%



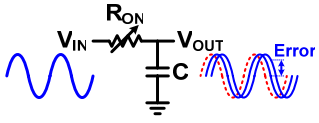
Distortion in sampled CT input

- **Input ~50 MHz, sampled at 100MHz**
  - Distortion at 57dB, or ~9 bits
  - This is larger than the maximum possible error due to amplitude variation



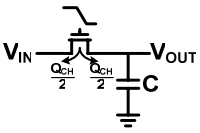
Phase Error

- **More significant error**
  - Due to variation in phase of low-pass filter
  - At 50 MHz (with same $R_{ON}C$ variation as DT case), maximum possible error is a few percent - error is less than that



Charge Injection

- **When a transistor turns off, the channel charge Q_{CH} goes into the circuit**
  - Doesn't exactly divide in half - depends on impedance seen at each terminal and the clock transition time
  - $Q_{CH} = WLC_{ox}(V_{DD} - V_{IN} - V_{TH})$
- **Charge into V_{IN} has no impact on output node**
  - Doesn't create error in the circuit
- **Charge into C causes error ΔV in V_{OUT}**



$$\Delta V = \frac{Q_{CH}}{2C} = \frac{WLC_{ox}(V_{DD} - V_{IN} - V_{TH})}{2C}$$

Charge Injection

- **In previous analysis, charge injection introduces a gain and offset error**
  - **This is still linear and could be tolerated or corrected**

$$V_{OUT} = V_{IN} - \Delta V = V_{IN}\left(1 + \frac{WLC_{ox}}{2C}\right) - \frac{WLC_{ox}(V_{DD} - V_{TH})}{2C}$$

- **But…**

  V_{TH} is actually a function of ~ $\sqrt{V_{IN}}$
  - **Introduces non-linear term that cannot be corrected in the circuit**

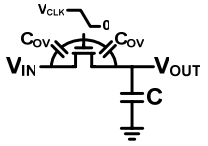
Charge Injection vs. Speed

- **Charge injection**
  - **Proportional to transistor size (WL)**
- **Speed**
  - **R_{ON} inversely proportional to aspect ratio (W/L)**
- **Figure of Merit**
  - **Product of speed (1/τ) and charge injection (1/ΔV)**

$$(\tau\Delta V)^{-1} = \left(\frac{C}{\mu_n C_{ox}(W/L)(V_{DD} - V_{IN} - V_{TH})}\right)^{-1}\left(\frac{WLC_{ox}}{C}(V_{DD} - V_{IN} - V_{TH})\right)^{-1} = \frac{\mu_n}{L^2}$$

Clock Feedthrough

- **Overlap capacitance allows clock to couple from the gate to drain/source terminals**
  - **Change in voltage ΔV independent of the input signal**
  - **Error is an offset voltage which is cancelled with differential operation**



$$\Delta V = \frac{C_{ov}}{C + C_{ov}} V_{CLK}$$

Charge Error Cancellation

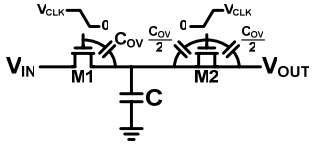
- **Differential operation**
  - **Cancels offset errors, depending on the matching between differential circuits**
  - **Applies to signal dependent portion of charge injection error, and clock feedthrough error**
- **Complementary Switches**
  - **Error cancelled for 1 input level**

$$W_n L_n C_{ox}(V_{CLK} - V_{IN} - V_{THN}) = W_p L_p C_{ox}(V_{IN} - |V_{THP}|)$$

  - **Clock feedthrough cancelled depending on similarity of overlap capacitance for PMOS and NMOS switches**

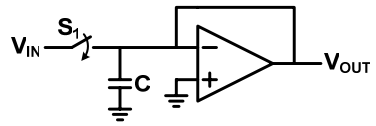
Charge Error Cancellation

- **Dummy Switch**
  - **Use second transistor to remove charge injection by main transistor**
  - **Inverted clock operates on dummy switch**
  - **Charge from M1: $q_{M1} = W_1 L_1 C_{ox}(V_{CK} - V_{IN} - V_{TH1})/2$**
  - **Charge from M2: $q_{M2} = W_2 L_2 C_{ox}(V_{CK} - V_{IN} - V_{TH2})$**
  - **If charge splits equally in M1 (not quite true), then with M2 half the size of M1, $q_{M1} = q_{M2}$**



Sample and Hold Amplifier

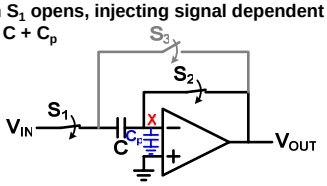
- **Input dependent charge from S_1 onto C**
  - **When S1 turns off, charge q adds to C**
  - **V_{OUT} is then equal to V_{IN}+q/C where q has a non-linear dependence on V_{IN}**



We can improve on this by making V_{OUT} independent of sampling switch charge…

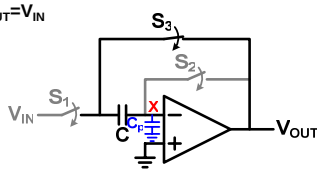
S/H Amplifier

- **Two phases**
  - Phase 1: S_1 and S_2 closed, V_{IN} sampled on C
  - Phase 2: S_3 closed, C is tied to V_{OUT}
- **Phase 1**
  - Charge on C is CV_{IN}
  - S_2 opens, injecting signal indep. charge at node X
  - Then S_1 opens, injecting signal dependent charge q onto C + C_p



S/H Amplifier

- **Phase 2**
  - Node X is a virtual ground and charge on C_p is zero
  - Charge on C is still CV_{IN}
  - S_3 injects charge on X that must be discharged due to virtual ground node – it does not disturb charge on C
  - $\therefore V_{OUT}=V_{IN}$

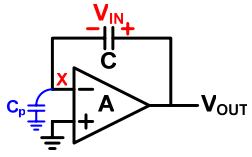


S_1 / S_3 are non-overlapping, S_2 slightly ahead of S_1

Gain of the S/H

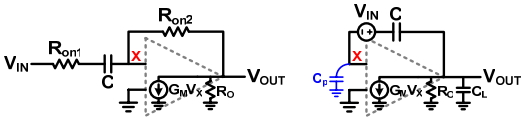
- **Finite OTA gain reduces gain of sampler**
  - On Phase 1, C charges to V_{IN}
  - On Phase 2, node X goes from 0 to $V_X = -V_{OUT}/A$
  - Charge comes from C, changing q_C to $CV_{IN} + C_pV_X$
  - $V_{OUT} - (CV_{IN} + C_pV_X)/C = V_X$

$$V_{OUT} = \frac{V_{IN}}{1+\frac{1}{A}\left(\frac{C_p}{C}+1\right)} \approx V_{IN}\left[1-\frac{1}{A}\left(\frac{C_p}{C}+1\right)\right]$$



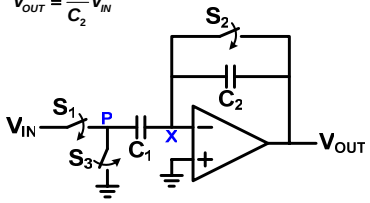
Speed of the S/H

- **In sampling mode (Phase 1)**
  - At node X, $R_X \sim 1/G_m$, $\tau_1 \sim (R_{on1}+1/G_m)C$
- **In amplification mode (Phase 2)**
  - Replace charge on C by voltage source V_{IN} (like switching in voltage source at start of Phase 2)
  - After analysis, $\tau_2 = (C_LC_p+C_pC+CC_L)/G_MC$
  - Reduces to $\tau_2 \sim C_L/G_M$ if C_p is small



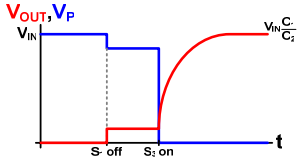
Basic Amplifier

- **Sampling phase when S_1 and S_2 closed**
  - Input signal sampled onto C_1
- **Amplifying phase when S_3 closed**
  - Charge on C_1 transferred to C_2 so that the final output is $V_{OUT} = \frac{C_1}{C_2}V_{IN}$



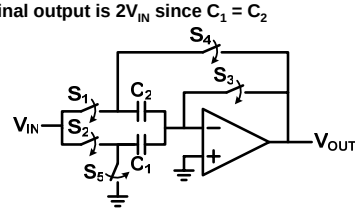
Basic Amplifier

- **S_2 must open before S_1 for the charge injection to be signal independent**
  - Charge from S_2 opening is deposited on C_1, but is not signal dependent
  - Charge from S_1 opening causes glitch in V_{OUT}
  - When S_3 closes, V_{OUT} goes to final value, regardless of what happened between S_2 opening and S_3 closing



Precision Gain-2

- Sampling phase when S_1, S_2, S_3 closed
  - Input signal sampled onto C_1 and C_2
- Amplifying phase when S_4, S_5 closed
  - Charge on C_1 is transferred to C_2 , doubling the charge on C_2
  - Final output is $2V_{IN}$ since $C_1 = C_2$



Precision Gain-2

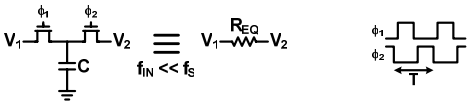
- How is it more precise?
  - The feedback factor in both gain circuits is

$$\frac{C_2}{C_2 + C_1 + C_p}$$

  - In the precision Gain-2 circuit, $C_1 = C_2$, while the basic amplifier has $C_1 = 2C_2$, resulting in a smaller feedback factor and a slower circuit
  - The gain error is inversely proportional to the feedback factor, so the precision circuit is more accurate for a given amplifier gain A

$$\frac{V_{OUT}}{V_{IN}} \approx 2\left(1 - \frac{C_2 + C_1 + C_p}{AC_2}\right)$$

Resistor Equivalence of SC



- Average current through switched-capacitor

$$\phi_1 : Q_1 = CV_1 \quad \phi_2 : Q_2 = CV_2$$

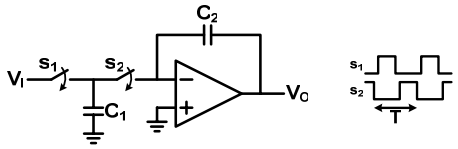
$$I_{AVG} = \frac{Q_1 - Q_2}{T} = \frac{C(V_1 - V_2)}{T}$$

- Equivalent current through a resistor ($f_{IN} << f_S$)

$$I_{EQ} = \frac{V_1 - V_2}{R_{EQ}}$$

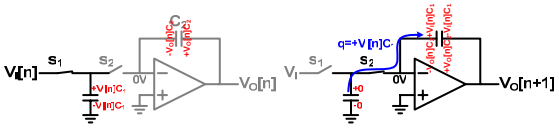
$$R_{EQ} = \frac{T}{C} = \frac{1}{Cf_S}$$

Switched-Capacitor Integrator



- Two non-overlapping clock phases control s_1,s_2
  - Phase 1: Sampling phase – input is sampled onto capacitor C_1
  - Phase 2: Integrating phase – additional charge is added to previous charge on C_2

Switched-Capacitor Integrator



Phase 1: s_1 on, s_2 off Phase 2: s_1 off, s_2 on

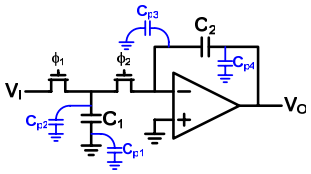
- Final charge on L.S. of C2 is $+V_O[n+1]C_2$

$$+V_O[n+1]C_2 = +V_O[n]C_2 - V_I[n]C_1$$

$$zV_O(z)C_2 = V_O(z)C_2 - V_I(z)C_1$$

$$\frac{V_O}{V_I}(z) = -\frac{C_1}{C_2}\frac{1}{z-1}$$

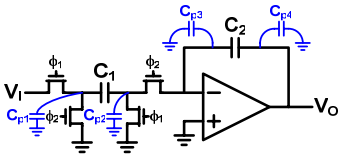
Parasitic Sensitive



- Parasitic capacitances C_{p1}, C_{p3} and C_{p4} have no impact on transfer function
- C_{p2} in parallel with C_1, changes transfer function

$$\frac{V_O}{V_I}(z) = -\frac{(C_1 + C_{p2})}{C_2}\frac{1}{z-1}$$

Parasitic Insensitive



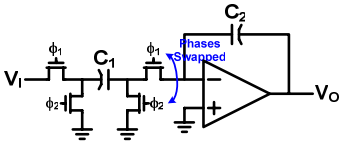
- Transfer function is non-inverting, delaying

$$\frac{V_O}{V_I}(z) = \frac{C_1}{C_2}\frac{1}{z-1}$$

Parasitic Insensitive

- Parasitics have no impact on transfer function
  - Better linearity since non-linear capacitors are unimportant
- Top plate on virtual ground node
  - Minimizes parasitics, improves amplifier speed and resolution, reduces noise coupled to node
- Two extra switches needed
  - More power to drive the switches for the same on-resistance

Delay-Free Integrator



- Same structure, still parasitic insensitive
- Transfer function is inverting, delay-free

$$\frac{V_O}{V_I}(z) = -\frac{C_1}{C_2}\frac{z}{z-1}$$

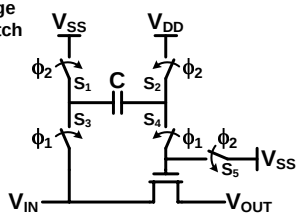
Bootstrapping

- At low supply voltages, signal swing is limited
  - Maximum distortion determines the tolerable variation in R_{ON}, and this limits the signal swing
- Want to increase V_{GS} on the sampling switch
  - Can do this by increasing the supply voltage for the sampling switch, but this requires slower thick oxide devices
  - Alternatively, add a constant voltage to the input signal and use that as the gate voltage – keep V_{GS} constant, reducing the variation in R_{ON}

Bootstrapped Circuit

- Basic operation
  - ϕ_2: C is charged to V_{DD} and gate of sampling switch is discharged to V_{SS} (turned off)
  - ϕ_1: V_{IN} is added to voltage across C, sampling switch turns on, gate voltage of the sampling switch is $V_{IN} + V_{DD}$

Ideally, there is always $V_{GS} = V_{DD}$ for the sampling switch



Bootstrapped Circuit

- C must be sized so that charge sharing between gate capacitance of switch is not significant

$$V_G = V_{IN} + \frac{C}{C + C_G}V_{DD}$$

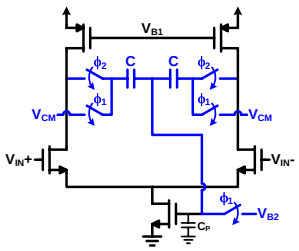
- Rise time controlled by size of S_4, fall time controlled by size of S_5
- Extra transistors required to limit gate-source voltages to V_{DD} and prevent overstress
  - See Dessouky, JSSC Mar.2001

Switched-Capacitor CMFB

- Two parts to the circuit
  - First, sense the common mode of the output
  - Second, compare the common mode to the expected common mode, and adjust the bias accordingly
- Sensing
  - Could use 2 resistors – they are either too small and reduce the gain, or they can get prohibitively large
  - Could use 2 capacitors – they don't reduce the gain, but the voltage across them is undefined
  - The voltage across them can be refreshed every clock cycle

Switched-Capacitor CMFB

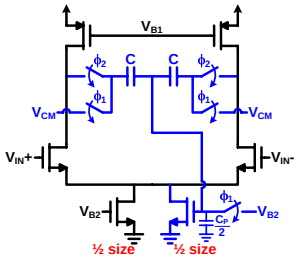
- One alternative…
  - Phase 1: precharge capacitors to ideal value
  - Phase 2: sense the difference and adjust the bias accordingly



But… there may be large changes in the tail current bias

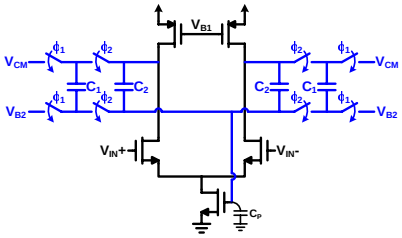
Switched-Capacitor CMFB

- Solution: Part of the tail current source can be controlled by a constant bias voltage
  - Will this work?



Switched-Capacitor CMFB

- Alternatively, use 2 capacitors so that only a fraction of the charge is shared to adjust the bias voltage
  - Typically, C_2 is 4-10 times C_1



NLCOTD: Schmitt Trigger

What You Learned Today

1. Errors introduced with simple sampling switch
   - RON variation, charge injection
2. Main SC Circuits – S/H, Gain and Integrators
   - Parasitic Insensitive
   - Signal-independent charge injection
3. Bootstrapped Circuit
4. Switched Capacitor CMFB