ECE1371 Advanced Analog Circuits Lecture 8

AMPLIFIER DESIGN

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Course Goals

- Deepen Understanding of CMOS analog circuit design through a top-down study of a modern analog system
 - The lectures will focus on Delta-Sigma ADCs, but you may do your project on another analog system.
- Develop circuit insight through brief peeks at some nifty little circuits The circuit world is filled with many little gems that every competent designer ought to recognize.

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Date	Lecture			Ref	Homework		
2008-01-07	RS	1	Introduction: MOD1 & MOD2	S&T 2-3, A	Matlab MOD2		
2008-01-14	RS	2	Example Design: Part 1	S&T 9.1, J&M 10	Switch-level sim		
2008-01-21	RS	3	Example Design: Part 2	J&M 14, S&T B	Q-level sim		
2008-01-28	тс	4	Pipeline and SAR ADCs	J&M 11,13	Pipeline DNL		
2008-02-04	ISSCC – No Lecture						
2008-02-11	RS	5	Advanced ΔΣ	S&T 4, 6.6, 9.4, B	CTMOD2; Proj.		
2008-02-18	Reading Week – No Lecture						
2008-02-25	RS	6	Comparator and Flash ADC	J&M 7			
2008-03-03	тс	7	SC Circuits	Raz 12, J&M 10			
2008-03-10	тс	8	Amplifier Design				
2008-03-17	тс	9	Amplifier Design				
2008-03-24	тс	10	Noise in SC Circuits	S&T C			
2008-03-31	RS	11	Switching Regulator				
2008-04-07		Project Presentations					
2008-04-14	тс	12	Matching & MM-Shaping		Project Report		
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Highlights

(i.e. What you will learn today)

- 1. Choice of V_{EFF}
- Several trade-offs with Noise, Bandwidth, Power,... 2. Amplifier Topology
- 3. Amplifier Settling
- Dominant Pole, Zero and Non-Dominant Pole 4. Gain-Boosting
- Stability, Pole-Zero Doublet
- 5. Delaying vs. Non-Delaying stages

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NLCOTD: Wide-Swing Cascode Current Mirror

- How do we bias cascode transistors to optimize signal swing?
- Standard cascode current mirror wastes too much swing $V_x = V_{EFF} + V_T$ $V_Y = 2V_{EFF} + 2V_T$ Minimum V_z is $2V_{EFF} + V_T$, which is V_T larger than necessary



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Choice of Effective Voltage

• Effective Voltage V_{EFF} = V_{GS} - V_T

$$V_{\text{EFF}} = \frac{2I_{\text{D}}}{g_{\text{m}}} = \sqrt{\frac{2I_{\text{D}}}{\mu_{\text{n}}C_{\text{ox}}}W_{\text{L}}}$$

- Assumes square-law model In weak-inversion, this relationship will not hold
- What are the trade-offs when choosing an appropriate effective voltage?
 Noise Power
 Bandwidth Swing
 Matching

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Thermal Noise and V_{EFF}

Noise Current and Noise Voltage

 $\overline{I_n^2}$

$$= 4 \, k T \gamma g_m \qquad \overline{V_n^2} = \frac{4 \, k T \gamma}{g_m}$$

 Ex. Common Source with transistor load CS transistor has input referred noise voltage proportional to V_{EFF}

$$\overline{V_n^2} = V_{\rm EFF,1} \frac{4kT\gamma}{2I_D}$$

Current source has input referred noise voltage inversely proportional to V_{EFF}

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$$\overline{V_n^2} = \frac{4kT\gamma}{2I_D} \frac{V_{EFF,1}^2}{V_{EFF,2}}$$

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Thermal Noise and V_{EFF}



Bandwidth and V_{EFF}

- Bandwidth dependent on transistor unity gain frequency f_{τ}

$$f_{T} = \frac{g_{m}}{2\pi(C_{GS} + C_{GD})}$$
 If C_{GS} dominates capacitance
1.5 μ

$$f_T \approx \frac{1.5\mu_n}{2\pi L^2} V_{EFF}$$

 $\label{eq:small_l} \begin{array}{l} Small L, large \; \mu \; maximizes \; f_{_T} \\ For \; a \; given \; current, \; decreasing \; V_{_{EFF}} \; increases \; W, \\ increases \; C_{_{GS}} \; and \; slows \; down \; the \; transistor \end{array}$

• f_T increases with V_{EFF}

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Power and V_{EFF}

- Efficiency of a transistor is g_m/l_D Transconductance for a given current – high efficiency results in lower power Bipolar devices have $g_m = l_C/V_t$, while (square-law) MOS devices have $g_m = 2l_D/V_{EFF}$; V_{EFF} larger than V_t
- V_{EFF} is inversely proportional to g_m/I_D Increasing V_{EFF} reduces efficiency of the transistor Biasing in weak inversion increases efficiency



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Matching and V_{EFF}

- With low V_{EFF} transistor is in weak inversion What happens with mismatch in $V_t?$
- Use a current-mirror as an example with mismatched threshold voltages



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Matching and V_{EFF}

- In strong inversion with $V_{\rm t}$ mismatch there is a quadratic relationship

$$\frac{I_{OUT}}{I_{IN}} = \frac{(V_{GS} - V_{t,2})^2}{(V_{GS} - V_{t,1})^2}$$

- 1mV error in V_t is ~1% error in I_{OUT} (for V_{EFF}~200mV)
- In weak inversion with $V_{\rm t}$ mismatch there is an exponential relationship

$$\frac{I_{OUT}}{I_{IN}} = \frac{\frac{V_{GS} - V_{t,1}}{nV_{T}}}{\frac{V_{GS} - V_{t,2}}{nV_{T}}} = e^{\frac{V_{t,2} - V_{t,1}}{nV_{T}}}$$

1mV error in V_t is ~4% error in I_{OUT}

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Swing and V_{EFF}

- Minimum V_{DS} of a transistor to keep it in saturation is V_{EFF}

Usually V_{DS} is V_{EFF} + 50mV or more to keep r_o high (keep the transistor in the saturation region) With limited supply voltages, the larger the V_{EFF}, the larger the V_{DS} across the transistor, less room for signal swing

Consequences

Can't cascode – reduced OTA gain Stage gain is smaller – input referred noise is larger (effectively the SNR at the stage output is less)

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Speed-Efficiency Product

• What is the optimal V_{EFF} using a figure of merit defined as the product of f_T and g_m/I_D Optimal point at V_{EFF} = 130mV in 0.18µm



Summary of Trade-Offs

- Benefits of larger V_{EFF}
 Larger bandwidth
 Better device matching
 Lower input-referred noise for current-source
 transistors
- Benefits of smaller V_{EFF}
 Better efficiency lower power
 Larger signal swings
 Better noise performance for input transistors

Good starting point: V_{EFF} ~ V_{DD}/10

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Device Parameter Summary

Device Parameter	Circuit Implications			
	Current Efficiency, g _m /I _D (matching) Power Dissipation			
V _{EFF}	Speed Cutoff Frequency, f _T (phase margin) Noise			
L	Headroom Cutoff Frequency, f _T			
w	Obtain from L, I _D Self Loading (C _{GS} , C _{GD})			

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Common Source Design

 Simple Design Example Specs: C_L = 5pF, f_u = 100MHz, Gain = 40

V_{EFF}: Assume we size it slightly higher than optimal f_T*g_m/I_D V_{EFF} = 180mV

Bandwidth: $\omega_U = g_m/C_L = 2\pi 10^8$ $g_m = 3.14mS$



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Common Source Design

How do we find L for the desired gain? Find current densities (V_{EFF} =180mV) for various L's Find the corresponding $g_m r_o$ of these transistors





Common Source Design



Common Source Design

W:

We have L and I_D 85uA for 4u/0.35u, we need 376uA W = 376uA/85uA*4um = 4.4 x 4u/0.35u

2nd Pole:

C_{GS} ~ 9fF*4.4 = 40fF (1+A)C_{GD} ~ 1.5fF*4.4*46 = 304fF With 50 source resistance, ω_{p2} ~ 9 GHz

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Amplifier Topology

• Briefly... (covered in Analog I, from Razavi Ch.9)

Topology	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded- Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain- Boosted	High	Medium	Medium	High	Medium

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Amplifier Errors

• Two errors: Dynamic and Static

 Static Errors Limit the final settling accuracy of the amplifier Capacitor Mismatch (C₁/C₂ error) Finite OTA gain $C_2 A$ $\frac{V_{o}}{V_{i}}(z) = \frac{C_{i}}{C_{2}} \left(\frac{\frac{C_{2} - C_{i}}{C_{2}(1+A) + C_{i}}}{z - \frac{C_{2}(1+A)}{C_{2}(1+A) + C_{i}}} \right)$

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Amplifier Errors



Dynamic Errors: Occurs in the integration phase • when a 'step' is applied to the OTA Slewing Finite bandwidth Feedforward path Non-dominant poles

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Amplifier Errors

· First look at frequency independent response Static error term 1/Aß

$$\frac{V_o}{V_i} = -\frac{C_1}{C_2} \frac{1}{1+1/A\beta} \approx -\frac{C_1}{C_2} \left(1 - \frac{1}{A\beta}\right)$$
$$\beta = \frac{C_2}{C_1 + C_2 + C_{iN}}$$

• Example: 0.1% error at output C₁ 1pF

= 4pF, C₂ = 1pF, C_{IN} = 1
$$\frac{V_o}{V_i} \approx -4\left(1 - \frac{6}{A}\right)$$

> 6000 for 0.1% error

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• What is the transfer function of this circuit? By inspection... Gain is $-C_1/C_2$ Zero when $V_XSC_2 = V_XG_m$ Pole at $\beta G_m/C_{L,eff}$ where $C_{L,eff} = C_2(1-\beta) + C_L$ $\frac{V_o}{V_i} = -\frac{C_i}{C_2} \frac{1 - \frac{SC_2}{G_m}}{1 + \frac{SC_{L,eff}}{RC_2}}$

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Single-Pole Settling Error

 Single-pole settling (ignore zero) Step response of 1st-order (unity-gain) system

Unit step $\frac{1}{s}$ through system $\frac{1}{1+s/\beta\omega_{unity}}$

Inverse Laplace transform of $\frac{1}{s(1+s/\beta\omega_{unity})}$

Step response is $1 - e^{-\beta \omega_{unity} t}$

Error is $e^{-\beta \omega_{unity}t}$

Settles to N-bit accuracy in $t > \frac{N \ln 2}{\beta \omega_{unity}}$

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Pole and Zero Settling Error

Single-pole settling with feedforward zero
 Step response, 1st-order system with feedforward zero



Effect of Zero on Settling

- Zero slows down settling time Additional settling term $-\frac{\beta \omega_{unity}}{\omega_z} e^{-\beta \omega_{unity}t}$ Coefficient a function of feedback factor β $-\frac{\beta \omega_{unity}}{\omega_z} = \frac{\beta G_m / C_{L,eff}}{G_m / C_2} = \frac{\beta C_2}{(1-\beta)C_2 + C_L}$
- To reduce impact of feedforward zero... Smaller β (one of the few advantages of reducing β) Larger C_L

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Effect of Zero on Settling

 Example of settling behaviour ^β = 1/2, C_L = C₂/2





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Two-Pole Settling Error

 Dominant and non-dominant pole settling Step response, 2nd-order system

Unit step
$$\frac{1}{s}$$
 through system $\frac{1}{\omega_{s^2} \cdot \beta \omega_{unity}} + \frac{s}{\beta \omega_{unity}} + \frac{1}{s}$

Step response is dependent on relative values of $\beta \omega_{unity}$ and ω_{p2}

3 Cases:

Overdamped, $\omega_{p2} > 4\beta\omega_{unity}$ Critically damped, $\omega_{p2} = 4\beta\omega_{unity}$ Underdamped, $\omega_{p2} < 4\beta\omega_{unity}$

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Two-Pole Settling Error

• Overdamped, $\omega_{p2} > 4\beta\omega_{unity}$ 2^{nd} pole much larger than unity-gain frequency Similar to 1st-order settling as 2nd pole approaches infinity Step response is $1 - \frac{B}{2}e^{-At} - \frac{A}{2}e^{-Bt}$

$$B-A \qquad A-B$$
$$A,B=\frac{\omega_{p2}}{2}\pm\frac{\sqrt{\omega_{p2}^{2}-4\omega_{p2}\beta\omega_{unity}}}{2}$$

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• Critically damped, $\omega_{p2} = 4\beta\omega_{unity}$ No overshoot Step response is $1 - e^{-2\beta \omega_{unity}t} - 2\beta\omega_{unity} te^{-2\beta \omega_{unity}t}$

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Two-Pole Settling Error

 Underdamped, ω_{p2} < 4βω_{unity} Minimum settling time depending on desired SNR Increasing overshoot as ω_{p2} decreases Step response is



Two-Pole Settling



Two-Pole Settling

Critically damped system settles faster than single-pole system



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Two-Pole Settling

 Underdamped system gives slightly better settling time depending on the desired SNR





Two-Pole Settling

• For a two-pole system, phase margin can be used equivalently

$$PM = 90 - \frac{180}{\pi} \tan^{-1} \left(\frac{\omega_{\rho 2}}{\omega_{unity}} \right)$$

Critically damped: PM = 76 degrees Underdamped: PM < 76 degrees (45 degrees if $\omega_{p2} = \beta \omega_{unity}$) Overdamped: PM = 76 to 90 degrees

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Gain-Boosting

- · Increase output impedance of cascoded transistor
 - Impedance boosted by gain of amplifier A $V_{OUT}/V_{IN} = -g_m R_{OUT}$ $R_{OUT} \sim Ag_m r_o^2$
- · Doesn't cost voltage headroom Amplifier requires some power, but does not have to be very fast

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Gain-Boosting

Need to analyze gain-boosting loop to ensure ٠ that it is stable Cascade of amplifier A and source follower from node Y to node X · What is the load capacitance at node Y? C_{GS}? ~0.1C_{GS}? Node Y might be dominated by parasitic capacitances with large variations - use C_c for a predictable response ECE1371 8-38

Gain-Boosting

 Stability of gain-boosted amplifier For 1st-order roll-off, the unity-gain frequency of the additional amplifier must be greater than the 3dB frequency of the original stage

 $\omega_{3dB} < \omega_{UG,A}$

• 2nd pole of feedback loop is equivalent to 2nd pole of main amplifier Set unity-gain frequency of additional amplifier lower

than 2nd pole of main amplifier (or set it to $\omega_{UG,A}$ ~ $\omega_{2nd}/3$ for a phase margin of ~71 degrees)

 $\omega_{\text{UG,A}} < \omega_{\text{2nd}}$

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Gain-Boosting

A_{ORIG}: Original amplifier response without gain-boosting A_{ADD}: Frequency response of feedback amplifier A A_{TOT}: Gain-boosted amplifier frequency response



Gain-Boosting

- Pole-zero doublet occurs at ω_{UG,A} Must ensure that this time constant does not dominate the settling behaviour
- Set βω₅ (3dB frequency of closed loop amplifier response) below $\omega_{UG,A}$ Ensures that time constant is dominated by 3dB frequency and not the pole-zero doublet $\beta \omega_5 < \omega_{UG,A}$

Final Constraint: $\beta \omega_5 < \omega_{UG,A} < \omega_{2nd}$

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Pole-Zero Doublet

Z_{CL}: Load Capacitance Z_{OUT}: gain-boosted output impedance ~ (1+A)g_mr_o² Z_{ORIG}: cascoded output impedance ~ g_mr_o² Z_{TOT}: Total Output Impedance



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Pole-Zero Doublet

• Why is this a problem?

1

Doublet introduces a slower settling component in the step response Step response (where ω_z and ω_p are the doublet pole and zero locations):

$$-e^{-\beta\omega_{unity}t}+\frac{\omega_z-\omega_p}{\beta\omega_{unity}}e^{-\omega_z t}$$

A higher-frequency doublet will always have an impact but will die away quickly A lower-frequency doublet will not have as large an impact, but it will persist much longer

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Delaying vs. Non-Delaying Stage

- Depending on the architecture and stage sizing, this can be a large power penalty
 - Large \mathbf{C}_{L} greatly reduces the power efficiency of an amplifier

Amplifier must be larger, resulting in a smaller feedback factor and reduced bandwidth



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Delaying Stage

• Delaying

Subsequent stage does not load the output Very little C_L on output of the amplifier

· Example:

1st stage 4x larger than 2nd stage ($C_3 = 0$ for delaying, $C_3 = C_1/4$ for non-delaying) Each stage has gain of 2 ($C_1/C_2 = 2$, $C_3/C_4 = 2$)

$$C_{L,eff} = \frac{C_2(C_1 + C_{IN})}{C_1 + C_2 + C_{IN}} + C_3 = \beta(C_1 + C_{IN}) + C_3$$
$$P_{delay} \propto \beta \omega_{anity} = \frac{\beta g_m}{C_{L,eff}} = \frac{g_m}{C_1 + C_{IN}}$$

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Non-Delaying Stage

Non-Delaying

Subsequent stage loads the output Applicable in pipeline ADCs, sometimes $\Delta\Sigma$ (usually subsequent stages much smaller, depending on OSR) Opamp is wasted during the non-amplifying stage (could power it down to save power)

• Example (continued):

$$\beta \omega_{unity} = \frac{p \cdot g_m}{C_{L_{eff}}} = \frac{g_m}{1.75C_i + 1.5C_{iN}}$$

Increase g_m by 1.75 => C_{IN} increases by 1.75

(approximately the same bandwidth with 1.75x power) $P_{non-delay} \propto 1.75 \beta \omega_{unity} = \frac{1.75 g_m}{1.75 C_i + 2.6 C_{iN}}$

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Amplifier Stability

- Both phases are important
 Different loading on sampling and amplification phase
- Feedback factor is larger in sampling phase than amplification phase Amplifier could potentially go unstable if it was originally sized for optimal phase margin in the amplification mode
- Non-Delaying stages are more susceptible to instability in sampling phase since a much smaller load capacitance is present

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Amplifier Stability

• Example: $C_1 = 2pF, C_2 = 1pF, C_{IN} = 1pF$ $C_L = 0.5pF \text{ (load of subsequent stage)}$ Delaying Stage Amplification: $\beta \omega_{unity} = g_m/3pF$ Sampling: $\beta = 1/2, C_{L,eff} = 1pF, \beta \omega_{unity} = g_m/2pF$ Phase Margin: 73 -> 65 Non-Delaying Stage Amplification: $\beta = 1/4, C_{L,eff} = 1.25pF, \beta \omega_{unity} = g_m/5pF$ Sampling: $\beta = 1/2, C_{L,eff} = 0.5pF, \beta \omega_{unity} = g_m/1pF$ Phase Margin: 73 -> 33

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NLCOTD: Wide-Swing Cascode Current Mirror

What You Learned Today

- 1. Choice of V_{EFF} Trade-offs with various paramters
- 2. Amplifier Topology
- 3. Amplifier Step Response
- 4. Gain-Boosting
- 5. Choice of Delaying/Non-Delaying Stages

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