ECE1371 Advanced Analog Circuits
Lecture 9

AMPLIFIER DESIGN

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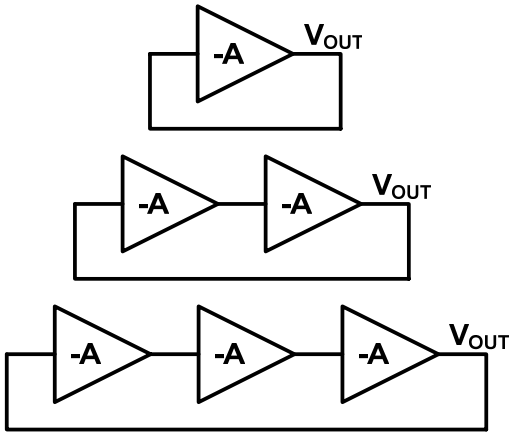
Course Goals

- **Deepen Understanding of CMOS analog circuit design through a top-down study of a modern analog system**
  - **The lectures will focus on Delta-Sigma ADCs, but you may do your project on another analog system.**
- **Develop circuit insight through brief peeks at some nifty little circuits**
  - **The circuit world is filled with many little gems that every competent designer ought to recognize.**

Date	Lecture			Ref	Homework
2008-01-07	RS	1	Introduction: MOD1 & MOD2	S&T 2-3, A	Matlab MOD2
2008-01-14	RS	2	Example Design: Part 1	S&T 9.1, J&M 10	Switch-level sim
2008-01-21	RS	3	Example Design: Part 2	J&M 14, S&T B	Q-level sim
2008-01-28	TC	4	Pipeline and SAR ADCs	J&M 11,13	Pipeline DNL
2008-02-04	ISSCC – No Lecture				
2008-02-11	RS	5	Advanced $\Delta\Sigma$	S&T 4, 6.6, 9.4, B	CTMOD2; Proj.
2008-02-18	Reading Week – No Lecture				
2008-02-25	RS	6	Comparator and Flash ADC	J&M 7	
2008-03-03	TC	7	SC Circuits	Raz 12, J&M 10	
2008-03-10	TC	8	Amplifier Design		
2008-03-17	TC	9	Amplifier Design		
2008-03-24	TC	10	Noise in SC Circuits	S&T C	
2008-03-31	RS	11	Switching Regulator		
2008-04-07	Project Presentations				
2008-04-14	TC	12	Matching & MM-Shaping		Project Report

NLCOTD: Ring Oscillators

- **Which of these circuits will oscillate?**



Highlights
(i.e. What you will learn today)

1. **How to design a folded-cascode OTA**

2. **Learn important trade-offs for OTA design**
   Including simulated examples

3. **Gain-boosting design example for OTA**

Design Specifications

- **Amplifier for 12-bit, 100MHz Pipeline ADC**
  1.5bit/stage => Closed-loop gain of 2

- **Target Bandwidth: 100MHz**
  T=10ns
  Assume ~1.5ns rise/fall/non-overlap time
  Try to settle within < 3.5ns
  Settling Error < -80dB
  If it is a critically damped system where $\omega_{p2} = 4\beta\omega_{unity}$
  $\beta\omega_{unity}$ **= 500MHz to settle in 2ns**
  If it is single-pole settling
  $\beta\omega_{unity}$ **= 500MHz to settle in 3ns**

Design Specifications

- **Target Gain Aβ: 75 dB**
  - **Input-referred error must be better than 12-bit**
  - **With all the other sources of error, put it at 13-bit (kT/C noise is ~12.3-bit)**
- **Swing: +/- 800mV differential**
  - **Assume noise has been calculated based on this swing requirement**
    - **Input signal +/- 800mV differential**
    - **Output signal will also be +/- 800mV differential**
  - **Each side of the OTA should swing from CM +/- 400mV (output CM will be around 900mV)**

Design Specifications

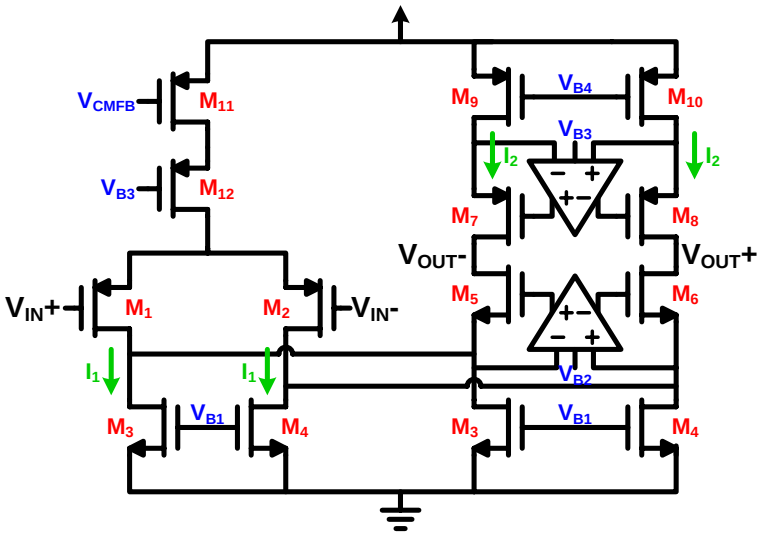
- **Capacitor Sizing**
  - **Based on noise requirements**
  - **C_1 = 2pF**
  - **C_2 = 1pF**
  - **C_L = 1pF**
  - **(assume 2nd stage is half the size of 1st stage – this means that input referred noise contribution is 3dB below the 1st stage)**
- **Power**
  - **Pipeline Target FOM: 160dB**
  - **74dB + 10log10(100MHz/P) = 160dB**
  - **P = 250mW**

Amplifier Topology

- **From Lecture 8…**

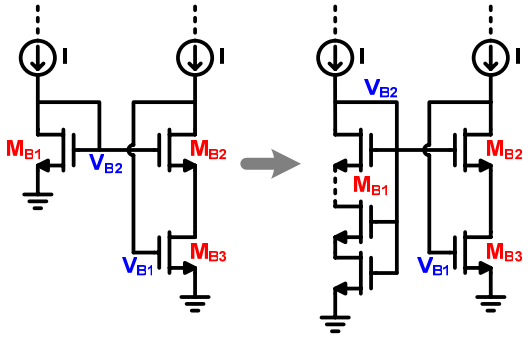
Topology	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

Folded-Cascode OTA



Biasing

- Use two wide-swing cascode current mirrors for V_{B3}, V_{B4} and V_{B1}, V_{B2}
  - M_{B1} is n times smaller so that V_{EFF} is $\sqrt{n}$ times bigger
- What if M_{B2} and M_{B3} are only a single finger?
  - M_{B1} cannot be 5-6 times smaller



Amplifier Topology

- Why Folded-Cascode instead of Telescopic?

✓ Better swing – with Telescopic, it is difficult to get the desired swing (assuming V_{EFF}~200mV + margins, and only 1.8V supply)

✓ Low (or high) Input CM (saves power since switches are smaller)

✗ Slower (lower non-dominant pole) and less power efficient

Amplifier Topology

- **Why PMOS input pair? (we will see more of this)**

  ✓ **Input CM: with PMOS input pair, input CM is lower, NMOS switches are used to pass the signal**

  ✓ **Non-dominant pole: larger since folding node uses NMOS devices which have smaller capacitance for a given V_{EFF}**

  ✓ **Flicker noise: smaller in PMOS devices (not too important in high-speed design)**

  ✗ **Larger β in NMOS: For the same transconductance, the input capacitance from NMOS input devices will be smaller**

Amplifier Topology

- **How should currents I_1 and I_2 be ratioed?**

  Amplifier transconductance g_m is determined by the transconductance of M_1 and M_2 => high current I_1

  Output impedance r_{OUT} is determined by the output impedance of M_3-M_{10} => low current I_2

  I_1 should not be too much larger than I_2 due to amplifier slewing (more on this…)

Amplifier Topology

- How should currents I_1 and I_2 be ratioed?

  But… increased transconductance increases C_{IN} and decreases β

  Recall (assuming no load capacitance C_L):

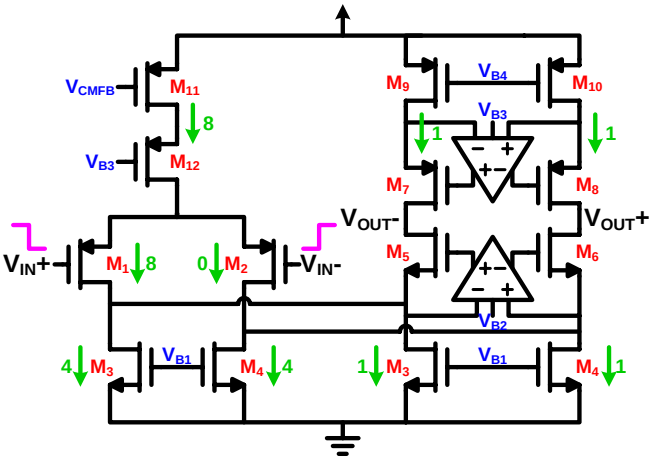
$$\beta\omega_{unity} = \frac{\beta g_m}{C_{L,eff}} = \frac{g_m}{C_1 + C_{IN}}$$

  So… once C_{IN} approaches C_1, $\beta\omega_{unity}$ does not increase linearly with g_m

Slewing

- Extra care must be taken if OTA slews

  Example: $I_1=4I_2$, Where does the excess current go?

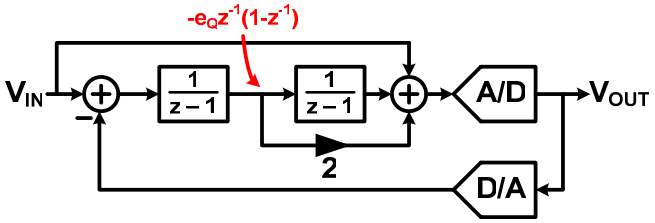


Slewing

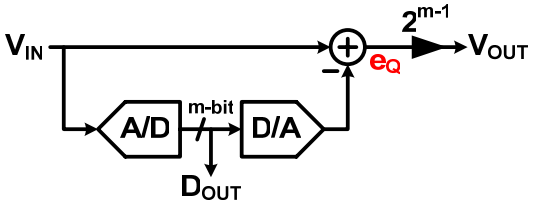
- M_4 absorbs current from capacitance at V_{OUT}+, M_1, M_{11}, M_{12} go into triode until the current is equal to $I_{D,M3}$
  - Capacitance at V_{OUT}- draws current from M_9
- Therefore, size the currents I_1 and I_2 the same
  - $M_{1,2}$ can still be sized to increase transconductance
  - Slewing is no longer a major problem (can be more power efficient)
- More likely to happen when output changes are large (e.g. no signal, just noise in the output)

Aside: OTA Output Signal

- Input Feed-forward $\Delta\Sigma$



- Pipeline ADC Stage



Current Source

- **Why Cascode instead of Large L?**

  Both can give a high output impedance…

  ✓ **Smaller capacitance to ground – increased impedance at high frequency, maintaining a higher CMRR (which is proportional to the tail current source impedance)**

  ✗ **Larger voltage across transistors (doesn't matter in this case since there is lots of room for the input CM)**

  ✗ **More complicated biasing (doesn't matter in this case since V_{B3} is already generated)**

Transistor Lengths

- **Generally minimum channel length is not used**
  - **Use ~1.5x minimum L for analog design**
  - **Moderately improves output impedance without sacrificing too much speed**
  - **Better matching between transistors**
  - **Reduce impact of short channel effects (threshold variation, mobility degradation, velocity saturation, DIBL, hot carrier effects)**

- **If bandwidth is imperative, use minimum L**

Choosing V_{EFF}

- **Input Pair (M_1,M_2)**
  - **Larger V_{EFF} means faster transistors, smaller transistors (increasing β)**
  - **Smaller V_{EFF} causes more slewing since it can easily be switched with large transients, but has lower noise and larger g_m**
- **Current Source Transistors (M_3,M_4)**
  - **Responsible for non-dominant pole**
  - **Larger V_{EFF} reduces noise and parasitic capacitances, improves non-dominant pole**

Power

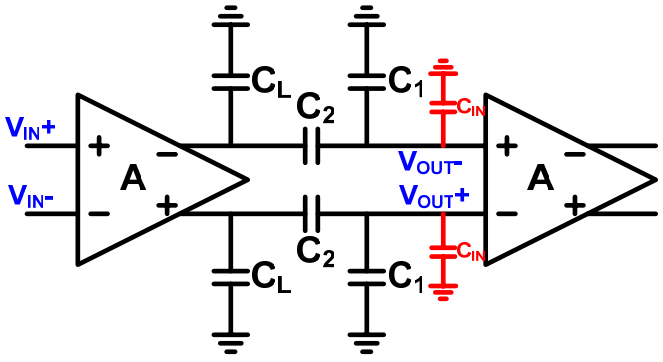
- **The power consumed by the 1st-stage OTA will be a significant fraction of the total power**
  - **It will be a good indication of the FOM you'll be targeting for your design**
- **Pipeline ADC**
  - **With S/H, other stages, and other overhead (clocks, buffers, biasing, comparators, etc.) first stage will probably consume 25-30% of the total power**
- **$\Delta\Sigma$ ADC**
  - **Since other stages are smaller, but other overhead still exists (possibly a higher resolution quantizer), first stage will probably consume 40-60% of the total power**

Quick Design / 1st Iteration

- 1:1 ratio between 1st and 2nd current branch
- Input transistor size: 9u/0.18um fingers
- Size every other transistor with a V_{EFF} ~ 180mV
  - PMOS: 55uA for 9um/0.24um fingers
  - NMOS: 55uA for 2um/0.24um fingers
- Use 140 fingers (more on this…)

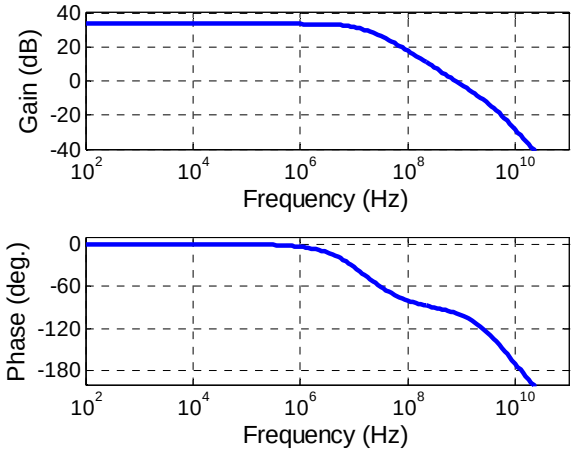
AC Testbench

- V_{OUT}/V_{IN} gives loop gain Aβ
  - C_1, C_2 and input capacitance of 2nd OTA gives proper feedback network



AC Simulation

$\beta\omega_{unity}$: 561 MHz, PM: 84.9 deg., DC Gain: 31.4 dB



AC Simulation

- **Observations…**

  Gain is low

  This can be corrected when gain-boosting is added, which should give about 40dB or more using folded-cascode gain-boosters

  Phase Margin is high

  This can be traded with bandwidth – the unity gain is not as high as it could be (β could be increased)

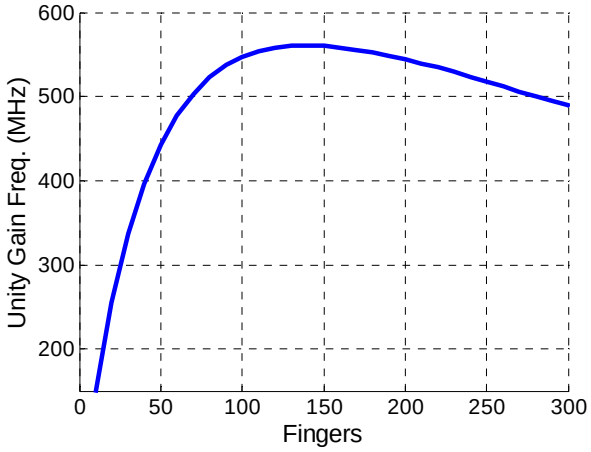
  The 2nd pole will reduce somewhat when gain-boosting is added (increased capacitance on the critical node), so it is worth having extra PM at this stage of the design

Optimizing Bandwidth

- **Why choose 140 fingers?**
  - **Once the V_{EFF}'s have been determined, there is nothing else to design except the size of the amplifier**
- **Increasing the number of fingers reduces β**
  - **An optimal point is eventually reached beyond which no further bandwidth improvements are achieved**
- **A parametric sweep can be performed to find this optimal point**
  - **Keep in mind: more fingers = more power**

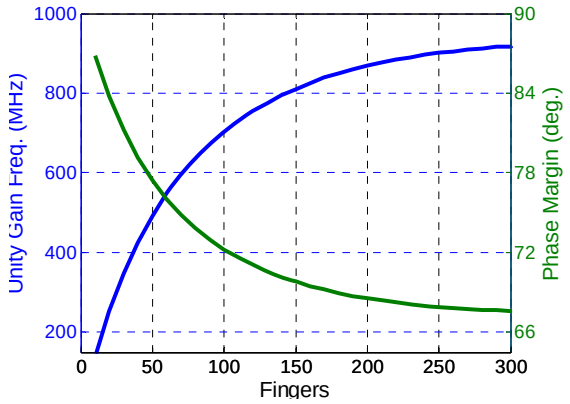
Optimizing Bandwidth

- **Optimal point ~ 140 fingers**
  - **4 branches x 140 fingers x 55uA = 30.8mA**



What about NMOS input?

- **We can try the same simulations with an NMOS input – what should happen?**
  - **Larger bandwidth ($\beta\omega_{unity}$ larger), less phase margin ($\beta\omega_{unity}$ larger, ω_{p2} smaller)**

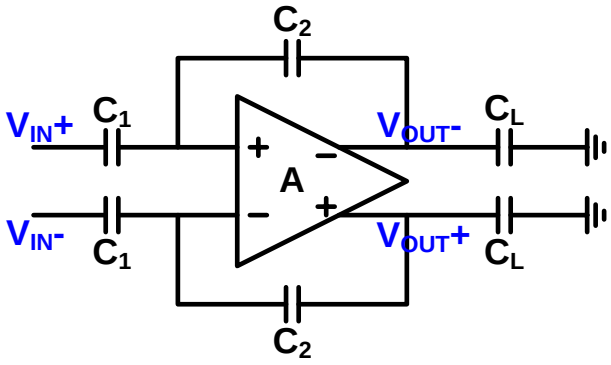


What about NMOS input?

- **Unity-gain is only 400MHz with an 80 degree PM**
  - **Although it is 70% less power!**
- **Make it more stable with larger PMOS V_{EFF}**
  - **Change PMOS fingers to 2um/0.24um**
  - **PMOS V_{EFF} becomes ~300mV**
- **Result**
  - **50 fingers, UG = 551MHz, PM = 79.8, DC Gain = 34.9dB**
  - **Swing reduced by 120mV, SNR reduced by 1.5dB, Capacitor (and amplifier) increased by ~35%**
  - **Still about 50% less than the original power**

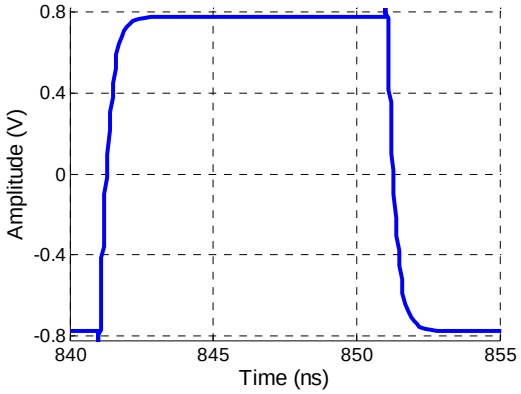
Transient Testbench

- **Make sure settling behaviour is as expected**
  - **Configured in amplification phase**
  - **Use differential step at input for full-scale output**



Transient Testbench

- **Settles to within 0.01% of final value in 2.1ns**
  - **Similar to predicted settling of 2-pole system**
  - **Zero adds some time (measured as ~0.05ns)**



Gain-Boosting

- **Need to increase the DC gain without losing too much bandwidth or stability**
  - **Gain-Boosting theoretically decouples improved gain from frequency response**
- **Single-Ended or Differential**
  - **Single-ended has lower-frequency mirror pole, slows down gain-booster (more difficult to optimize pole-zero doublet)**
  - **Differential gain-boosting does not increase common-mode gain of overall amplifier significantly**
  - **Differential requires CMFB**

Gain-Booster Design

- **Type of Amplifier**
  - **Input CM is very close to rail (either VDD or VSS)**
  - **Output CM is approximately mid-rail**
  - **Want ~40dB gain with moderate to high speed (single-stage with cascoding)**

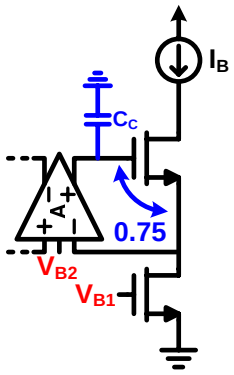
  => Choose differential Folded-Cascode (Telescopic cannot handle the input/output CM, single-ended not fast enough)
    - **PMOS input for NMOS (V_{B2}) biases**
    - **NMOS input for PMOS (V_{B3}) biases**

Gain-Booster Design

- **Gain**
  - Need another 43-44dB for the 75dB total
- **Frequency response**
  - $\beta\omega_{unity}$ ~ 560MHz, ω_{p2} ~ 4GHz
  - Gain-booster unity-gain should be ~ 1GHz
- **V_{EFF}**
  - Can use higher V_{EFF}'s since swing is not as important
- **Input Pair**
  - Size of PMOS input pair in the V_{B2} gain-booster impacts the non-dominant pole and should be kept small

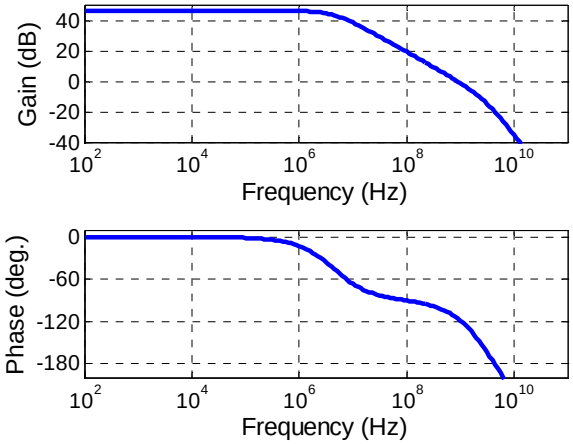
Gain-Boosted Loop

- **Source Follower introduces a gain of ~ 0.75 (assuming deep N-well is not used – body effect is present)**
  - This reduces the bandwidth by the same amount
  - Gain-Boosted amplifier A needs a unity-gain frequency of approximately 1.33 GHz
- **Also, add a compensation capacitor of ~100fF so that parasitics do not dominate the capacitance at that node**



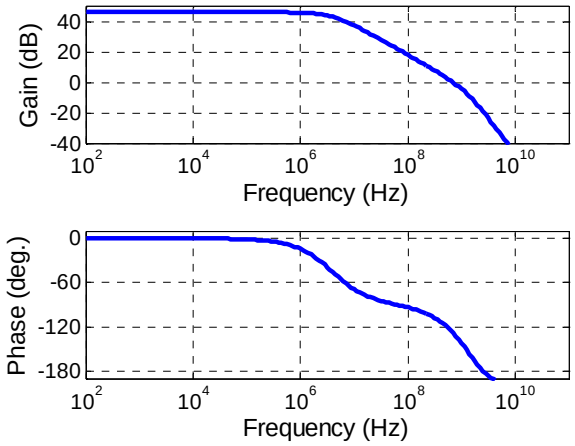
V_{B2} Gain-Booster AC Simulation

ω_{unity}: 901 MHz, PM: 64.2 deg., DC Gain: 46.8 dB



V_{B3} Gain-Booster AC Simulation

ω_{unity}: 703 MHz, PM: 55.7 deg., DC Gain: 46.4 dB



Size of Gain-Boosters

- V_{B2} gain booster is similar to main amplifier
  - Size of amplifier is 6
  - Compensation capacitor is 100fF
  - 4 branches x 6 fingers x 55uA = 1.32mA
- V_{B3} gain booster has NMOS inputs
  - Size of amplifier is 20
  - Compensation capacitor is 200fF
  - 4 branches x 20 fingers x 55uA = 4.4mA
  - Much larger since load capacitance on PMOS transistors is ~4x larger

Pole-Zero Doublet

- Recall settling behaviour

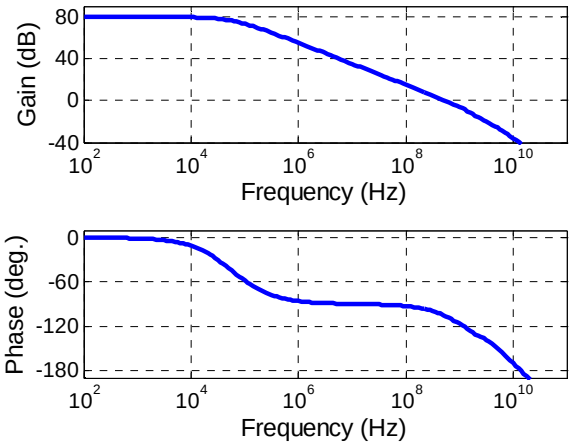
$$1 - e^{-\beta\omega_{unity}t} + \frac{\omega_z - \omega_p}{\beta\omega_{unity}} e^{-\omega_z t}$$

- Advantage of PMOS main amplifier
  - Distance between $\beta\omega_{unity}$ and ω_{p2} is larger
  - More room to have $\beta\omega_{unity} < \omega_{u,GB} < \omega_{p2}$
  - The farther $\omega_{u,GB}$ is from $\beta\omega_{unity}$, the closer together the pole and zero are in the doublet
  - => Smaller impact of pole-zero doublet

Main Amplifier with Gain-Booster

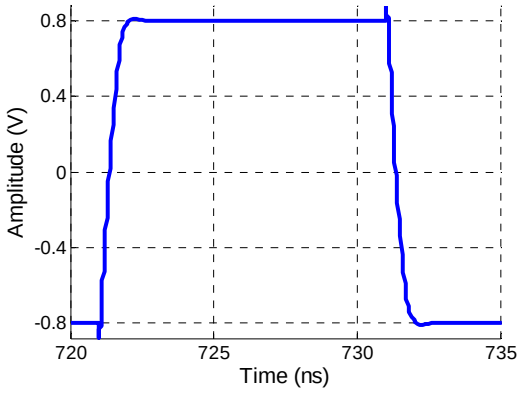
$\beta\omega_{unity}$: 545 MHz, PM: 74.1 deg., DC Gain: 79.5 dB

Where is the pole-zero doublet?



Transient Response

- **Settles to within 0.01% of final value in 2.54ns**
  - **Very small 8mV overshoot (0.5%)**
  - **About 25% slower with gain-booster**

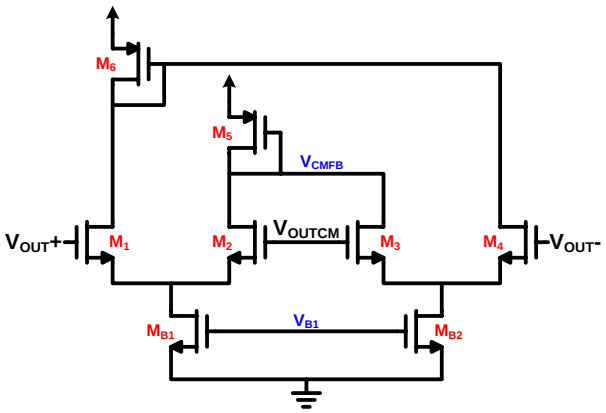


CMFB Loop Stability

- Two different CMFB loops to look at
  - Continuous-time CMFB for gain-boosters
  - Discrete-time CMFB for main amplifier
- Analyze loop gain through CMFB network
  - Break the loop somewhere (tail current)
  - Load the amplifier as it was when the loop was broken
  - Analyze the gain from the tail current to the tail current control voltage
  - Make sure all voltages are at their correct DC values

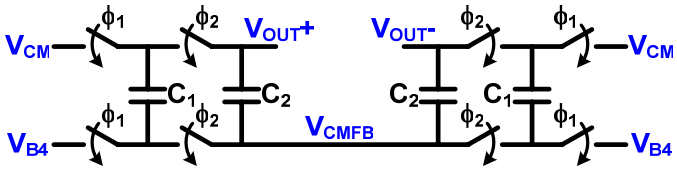
CMFB in Gain-Boosters

- Continuous-time CMFB should be sufficient
  - Swing is not as important since voltages should not change very much



CMFB in Main Amplifier

- As presented in SC lecture
  - Allows larger swing than continuous-time CMFB
  - Large capacitors overload the output more than is necessary, while small capacitors cause CM offset voltages from charge injection
  - Typically use minimum size switches/transmission gates depending on the voltage level passed



Summary of Results

- Full-scale (+/- 800mV differentially) settling time
  - DC Gain: 79dB
  - Phase Margin: 74 deg.
  - 0.01% (80dB): 2.54ns with 0.5% overshoot
- Power
  - (30.8mA + 1.3mA + 4.4mA) x 1.8V = 66mW
  - ~25% of total power => total power ~ 250mW
- Common Modes
  - Design based on using 400mV input CM and 900mV output CM
  - 400mV should allow all switches to be relatively small (except the ones attached to the output)

NLCOTD: Ring Oscillators

What You Learned Today

1. **Design of a folded-cascode OTA**
2. **Important trade-offs in OTA design**
3. **Gain-boosting design example for OTA**