High Speed Metamaterial-Inspired Negative Group Delay Circuits in CMOS for Delay Equalization

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***Abstract*—Two metamaterial-inspired CMOS integrated circuits for millimetre-wave frequencies of operation are investigated that utilize lumped element components and tuneable varactors in an LC ladder configuration for negative group delay (NGD) values. Measurement and simulation results of a passive, fixed transmission line (TL) structure are presented along with an equivalent circuit model. Realized NGD values are observed from 20 to 24 GHz with a minimum value of -84 ps. By the addition of an accumulation-mode varactor the proposed circuit can be made tuneable; measured NGD values from 13.3 to 26.2 GHz are observed. These high speed circuits may be useful to minimize group delay (GD) variations generated by active and passive devices and thus can act as delay equalizers when placed in cascade. Concepts are illustrated by reducing GD in lowpass (LP), highpass (HP) and bandpass (BP) filters. The proposed circuits can be useful to reduce unwanted dispersion effects in silicon-based devices and systems and high speed interconnects at millimetre-wave frequencies.**

I. Introduction

In high speed telecommunications, unwanted dispersion effects are problematic and can degrade overall system performance. Linear phase or flat group delay (GD) values are necessary to avoid distortion of high frequency signals. In the electrical domain, or more specifically in microelectronic circuit systems, equalizers can be used to compensate and minimize GDs introduced by transistor latency, transmission line (TL) interconnects, and circuit elements such as amplifiers, filters and oscillators [1]-[3].

Traditional equalization techniques using phase compensation have shown much promise [4] in reducing delay. But achieving negative GD values using low order designs may be difficult and thus the potential range of equalization can be limited. More recently printed, delay compensation circuits using metamaterial-based TL structures have been proposed [5], [6]. These design exhibit abnormal group velocities and negative group delays (NGDs) and thus offer new methods for GD equalization below 5 GHz [7], [8], [9]. Unfortunately, such passive metamaterial TL structures are generally limited by high insertion loss values, and in practice, amplifiers can be used to mitigate such losses [8], [10]-[12].

By the application of such metamaterial TL design concepts, two CMOS integrated circuits are presented in this work for millimetre-wave frequencies of operation. Other metamaterial-based TL structures have been implemented in CMOS [13], [14] but to the authors' knowledge the proposed circuits are the first to offer NGD values in a standard CMOS technology. As shown in Fig. 1, passive metal-insulator-metal (MIM) capacitors and spiral inductors are placed in a TL configuration defining a single unit cell. By series loading of an RLC resonator, NGD values can be observed from 20 to 24 GHz. The proposed 0.18μm CMOS circuit can be made tuneable by inclusion of an active accumulation-mode NMOS varactor (within the RLC resonator) and measured NGD values are observed from 13.3 to 26.2 GHz. Losses can be reduced by the addition of a pre-amplifier and additional GD control may also be possible by further element tuning using active devices in the shunt or series branches of the compact CMOS circuit.

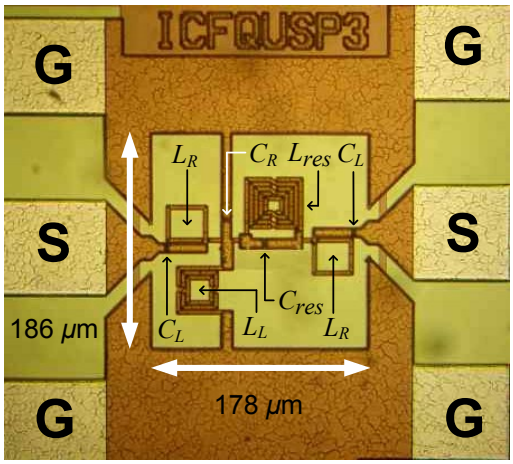

Fig. 1. Passive fully integrated CMOS MMIC offering NGD from 20 to 24 GHz. Square and symmetrical inductors and MIM capacitors define the CMOS structure (total size: 186 μm x 178 μm, excluding pads).

When placed in cascade with TL interconnects and common active or passive devices, the proposed CMOS circuits may be used as delay equalizers to minimize GD as illustrated in Fig. 2. For example, gain peaking in amplifiers or high Q filters may increase unwanted GD variations and thus the

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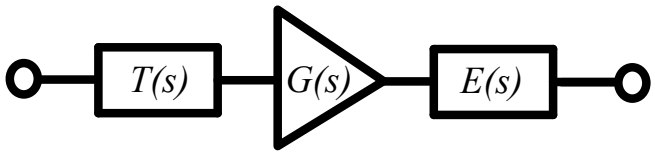

Fig. 2. Illustration of a cascade connection of a generic circuit device (examples include oscillators, filters and amplifiers), TL interconnect or high speed system, $T(s)$, and the proposed equalizer, $E(s)$, to minimize GD. In addition, a pre-amplifier, $G(s)$, can be used to reduce insertion losses.

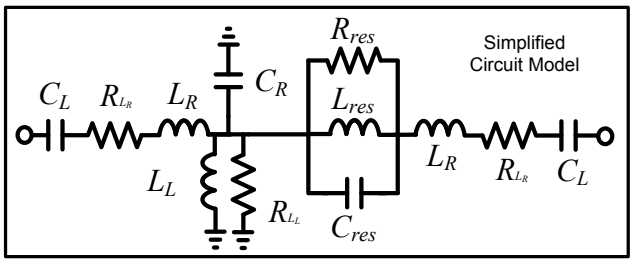

Fig. 3. An equivalent circuit model for the proposed CMOS TL structure.

proposed NGD circuits may mitigate such effects. In addition, the presented CMOS circuits could also be placed at the termination of a network offering a low cost solution for GD reduction and correction in constructed high speed circuit systems. This equalization technique is investigated in a circuit example by reducing GDs of ideal lowpass (LP), highpass (HP) and bandpass (BP) filters [4] using an equivalent circuit model developed for the passive NGD circuit (Fig. 3). When GD is of concern the presented high speed CMOS circuits may offer some advantages over common allpass filters, delay equalization and phase compensation techniques [4] in terms of compactness, tunability and ease of design for silicon-based devices and high speed systems.

II. Negative Group Delay TL Structures

Metamaterial TL structures [5], [6] offering NGDs [7] have been theoretically analyzed in the literature. Their dispersion properties can be described by regions of phase compensation, defined by right- and left-handed TL components within a unit cell; L_R C_R, L_L and C_L. Essentially, by the addition of a parallel RLC resonator (L_{res}, C_{res} and R_{res} embedded in series within each unit cell) NGD values can be observed near the resonant frequency of the RLC, $f_{res} = 1/2\pi\sqrt{C_{res}L_{res}}$, but at the cost of high insertion losses due to absorption of the resonator [7], [8]. In addition, high Q values $\left(Q = R_{res}/\sqrt{L_{res}/C_{res}}\right)$ can be observed near f_{res} [15]. Multiple unit cells can be placed in cascade for increased NGD values producing a region of anomalous dispersion [7].

In the time domain such circuits cause the output peak of a wave packet or signal, to precede the input. This interesting phenomenon can be described by casual pulse reshaping in which the TL structure generates a copy of the incident signal from initial transients [5].

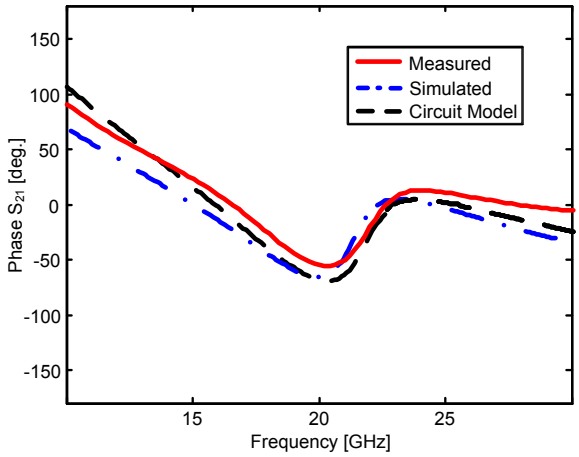

Fig. 4. Insertion phase for the passive NGD circuit. Positive phase slope values of 21.4°/GHz are observed from 21.0 - 23.5 GHz.

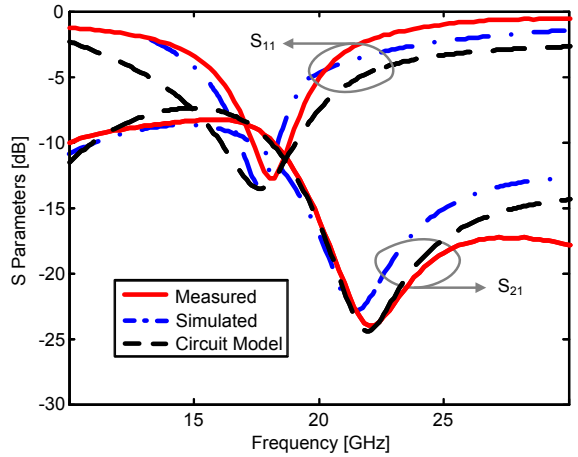

Fig. 5. Measured and simulated return and insertion losses for the passive NGD circuit. Results are also compared to the circuit model of Fig. 3.

III. CMOS Design, Implementation & Applications

The passive CMOS structures were fabricated in a low cost 0.18μm thick metal 6 CMOS process as shown in Fig. 1. Spiral inductors (L_R, L_L and L_{res}) and metal-insulator-metal (MIM) capacitors (C_R, C_L and C_{res}) define the completely lumped circuit elements. The compact TL structure was contained within a large ground plane, allowing for simple integration with other high speed CMOS circuits.

An equivalent circuit model of the unit cell (Fig. 3) was developed using a commercial circuit simulator (Agilent ADS) and modeled values were verified using Π/T extraction techniques. Results were compared with measurements and full-wave simulations as shown in Figs. 4-6. A good agreement is achieved. Lumped element component values and equivalent circuit details are described in Table I. Positive phase slope values can be realized from 21.0 - 23.5 GHz (near the resonant frequency of the RLC, $f_{res} = 21.7$ GHz), and as expected, high insertion loss values ($|S_{21}| \leq -15$ dB) are observed from 20-25 GHz .

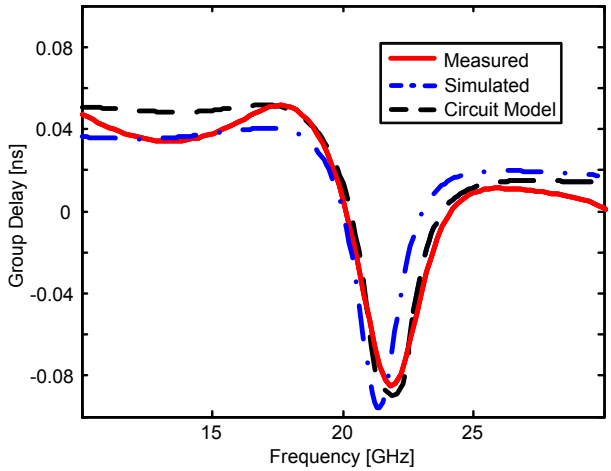

Fig. 6. Group delay for the passive CMOS structure. Negative values are observed with the measurements [simulations] <circuit model> from 20 to 24 GHz with a minimum value of -84 [-89] <-84> ps. Group delay variations of less than 135 ps are observed from 10 to 30 GHz.

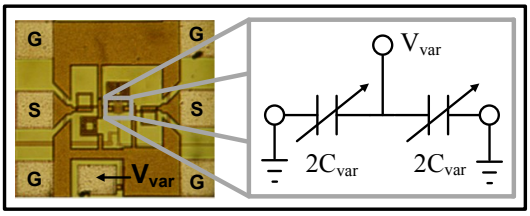

Fig. 7. Active GD control by varying V_{var} and replacing C_{res} with two voltage controlled AMOS varactors, C_{var}, in the parallel RLC resonator.

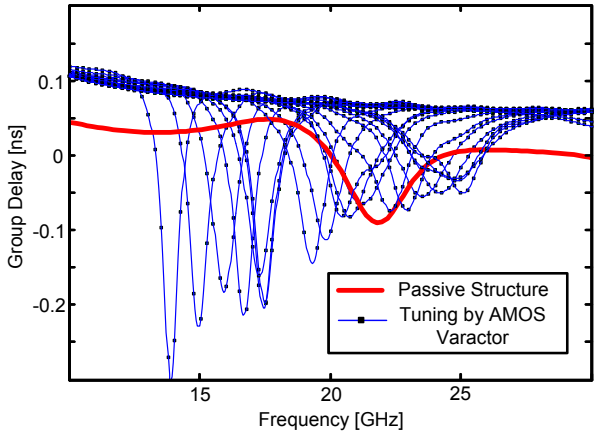

Fig. 8. Measurements of the passive CMOS structure (solid red line in Fig. 6) and active NGD tuning by replacing C_{res} with an AMOS varactor as shown in Fig. 7. By variation of the varactor control voltage, V_{var}, NGD values can be observed from 13.3 to 26.2 GHz ($\Delta V_{var} \in [-2.0, +2.2]$ V).

A. RLC Resonator Design for Negative Group Delay

It should be noted that the RLC resonator was implemented without the addition of a parallel resistor, R_{res}, reducing the required components of the NGD device. In fact, the low series losses of the spiral inductor were increased (as required for NGDs) by $Q^2 + 1$ when placed in parallel with the MIM capacitor [15]. Thus the simple parallel connection of a MIM capacitor and spiral inductor (with low loss, 3.25 Ω) can realize the required RLC resonator.

B. Active Tuning of the Negative Group Delay CMOS Circuit

By replacing the C_{res} MIM capacitor with voltage controlled varactors as shown in Fig. 7 the resonant frequency of the RLC can be tuned and thus NGD values can be varied from 13.3 to 26.2 GHz as shown in Fig. 8. A singly tuned accumulation-mode N-MOS varactor (256 fingers for each $2C_{var}$, nominal value of approximately 0.5 pF for zero bias) was utilized in the CMOS circuit. It is interesting to note that the active varactor elements introduced a positive delay (variation $\leq +65$ ps) lowering the overall NGD when compared to the passive CMOS device. Additional varactors can be used in the TL sections and thus increased NGD tuning is possible. Such millimeter-wave active CMOS designs may be useful as tunable equalizers in high speed circuit systems when high GD variations are of concern.

C. Application to Delay Equalization

The proposed NGD CMOS circuits can also be placed in cascade with interconnects and common active and passive devices, and thus may be used as delay equalizers [4] to minimize GD variations in high speed circuit systems. Ideal LP, HP and BP filters [4] were designed in ADS and results were compared with and without the additional equalization circuit (in cascade) for GD reduction. Results and details of the investigated filters are shown in Figs. 9 and Table II. As expected the NGD circuit reduced GD variations for all three designs by more than 61.3 %.

In addition, the LP Chebyshev filter response with and without delay equalization is shown in Figs. 9 (b) and (c). Reasonable insertion loss values are observed (with a maximum of 7.9 dB for the cascade configuration, while 15 dB for the passive NGD circuit) along with reduced group delay

TABLE I
PASSIVE CMOS COMPONENTS AND EQUIVALENT CIRCUIT DETAILS

Value	Design Notes	Circuit Detail
	CMOS Lumped Element	Footprint [μm]
C_{res}	MIM Capacitor	8 x 12
L_{res}	Symmetrical Inductor	47 x 50
C_R	MIM Capacitor	8 x 12
C_L	MIM Capacitor	8 x 35
L_R	Spiral Inductor	34 x 35
L_L	Symmetrical Inductor	37 x 40
	Equivalent Circuit Model Values	Modeled Losses
C_{res}	0.2075 pF	– – – – – – –
L_{res}	0.2592 nH	R_{res} = 382 Ω
C_R	0.6672 pF	– – – – – – –
C_L	0.8128 pF	– – – – – – –
L_R	0.0902 nH	R_{L_L} = 33.5 Ω
L_L	0.1187 nH	R_{L_R} = 4.8 Ω

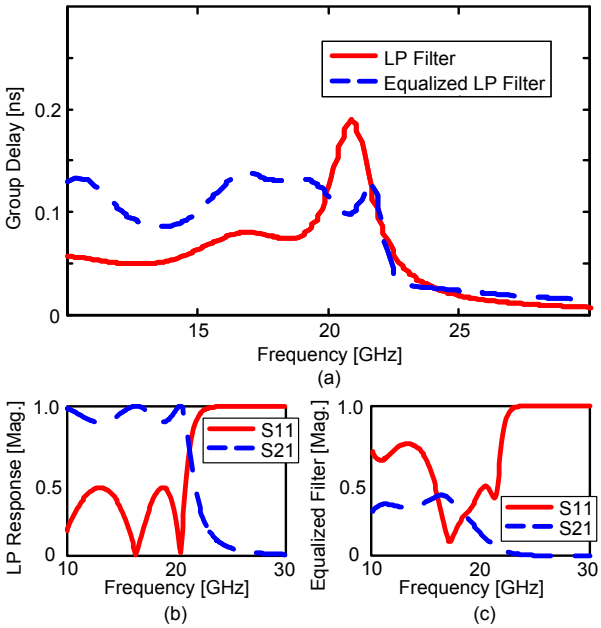

Fig. 9. Low pass Chebyshev filter results with and without the cascaded NGD circuit for delay equalization. (a): group delay variations of 123 and 183 ps are observed from 10 to 30 GHz, respectfully, (b): magnitude of the filter response with no equalization and (c) filter response with equalization.

variations (60 ps from 10-30 GHz) suggesting a reasonable, equalized design. For the investigated HP [BP] filter with and without the cascaded NGD circuit, GD variations of 106 and 173 ps [279 and 394 ps] are observed from 10 to 30 GHz.

IV. Conclusion

Completely integrated metamaterial-inspired NGD CMOS circuits are presented for delay equalization. Measurement and simulation results are presented along with an equivalent circuit model. Negative GD values are observed from 20 to 24 GHz, and by the addition of AMOS varactors, the device can be made tuneable. For practical implementations pre-amplifiers may be required to reduce the inherent insertion losses. Additional GD control may also be possible by further element tuning or by the inclusion of other active devices in the shunt or series branches of the compact CMOS circuit.

Acknowledgment

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TABLE II
Investigated Filters and Group Delay Minimization with the Proposed Passive CMOS Equalizer in Cascade

Filter Details	Specification
	Low Pass Filter
Filter Type	Ideal Chebyshev
Passband Edge Freq.	21.0 GHz
Stopband Edge Freq.	24.0 GHz
Passband Ripple	1.0 dB
Stopband Edge Atten.	20.0 dB
Filter Group Delay	ΔGD=183 ps, 10-30 GHz
Equalized Group Delay	ΔGD=123 ps, 10-30 GHz
ΔGD Reduction	60 ps, 10-30 GHz
Cascade Performance	$\lvert S_{21}\rvert \leq$ -7.9 dB
	High Pass Filter
Filter Type	Ideal Chebyshev
Passband Edge Freq.	21.7 GHz
Stopband Edge Freq.	18.4 GHz
Passband Ripple	1.0 dB
Stopband Edge Atten.	20.0 dB
Filter Group Delay	ΔGD=173 ps, 10-30 GHz
Equalized Group Delay	ΔGD=106 ps, 10-30 GHz
ΔGD Reduction	67 ps, 10-30 GHz
Cascade Performance	$\lvert S_{21}\rvert \leq$ -15.1 dB
	Bandpass Filter
Filter Type	Ideal Butterworth
Center Freq.	22.6 GHz
Passband Bandwidth	1.4 GHz
Stopband Bandwidth	6.2 GHz
Stopband Edge Atten.	20.0 dB
Passband Edge Atten.	3.0 dB
Filter Group Delay	ΔGD=394 ps, 10-30 GHz
Equalized Group Delay	ΔGD=279 ps, 10-30 GHz
ΔGD Reduction	115 ps, 10-30 GHz
Cascade Performance	$\lvert S_{21}\rvert \leq$ -23.1 dB

References

[1] S. Lucyszyn, I. D. Robertson, and A. H. Aghvami, "Negative Group Delay Synthesiser, *IET Electronic Letters*, vol. 29, no. 9, pp. 798-800, Apr.1993.

[2] C.D. Broomfield and J.K.A. Everard,"Broadband Negative Group Delay Networks for Compensation of Microwave Oscillators and Filters," *IET Electronic Letters*, vol. 36, no. 23, pp. 1931–1933, Nov. 2000.

[3] B. Ravelo, A. Prennec, M. Le Roy, and Y.G. Boucher, "Active Microwave Circuit With Negative Group Delay," *IEEE Micro. and Wire. Comp. Lett.*, vol. 17, no. 12, pp. 861–863, Dec. 2007.

[4] R. Schaumann and M.E. Van Valkenburg *Design of Analog Filters*. Cambridge University Press, New York, 2001.

[5] G. V. Eleftheriades and K.G. Balmain, *Negative-Refraction Metamaterials*. John Wiley and Sons Inc. New Jersey: Wiley-Interscience, 2005.

[6] C. Caloz and T. Itoh, *Electromagnetic Metamaterials: Transmission Line Theory and Microwave Applications*. John Wiley and Sons Inc. New Jersey: Wiley-Interscience, 2006.

[7] O.F. Siddiqui, M. Mojahedi, and G. V. Eleftheriades, "Periodically Loaded Transmission Line With Effective Negative Refractive Index and Negative Group Velocity," *IEEE Trans. Antenn. and Prop.*, vol. 51, no. 10, pp. 2619–2625, Oct. 2003.

[8] S.J. Erickson, M. Khaja, and M. Mojahedi,"Time- and Frequency-Domain Measurements for an Active Negative Group Delay Circuit," *APS 2005*.

[9] D. Solli and R.Y. Chiao, "Superluminal Effects and Negative Delays in Electronics, and Their Applications," *Phys. Rev. E*, no. 5, pp. 56601.1-056601.4, Nov. 2002.

[10] K. Murase, R. Ishikawa, and K. Honjo, "Group Delay Compensation Technique for UWB MMIC Using Composite Right/Left-Handed Circuit, *Asia-Pacific Microw. Conf.*, Yokohama, Japan, 2006, pp. 1409-1412.

[11] H. Noto, K. Yamauchi, M. Nakayama, and Y. Isota,"Negative Group Delay Circuit for Feed-Forward Amplifier," *IEEE APS 2007*, pp. 1103–1106, Jun. 2007.

[12] M. Kandic and G. Bridges, "Active Gain Compensated Negative Group Delay Circuit, *URSI General Assembly*, Chicago, UL., USA, Aug. 2008.

[13] M. Abdalla, K. Phang, and G. V. Eleftheriades, "A 0.13-μm CMOS phase shifter using tunable positive/negative refractive index transmission lines," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 12, pp. 705–707, Dec. 2006.

[14] ——, "Printed and integrated CMOS positive/negative refractive-index phase shifters using tunable active inductors," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 8, pp. 1611–1623, Aug. 2007.

[15] T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits, 2nd. Edition*. Cambridge University Press, New York, 2004.