High Speed Metamaterial-Inspired Negative Group Delay Circuits in CMOS for Delay Equalization

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Abstract—Two metamaterial-inspired CMOS integrated circuits for millimetre-wave frequencies of operation are investigated that utilize lumped element components and tuneable varactors in an LC ladder configuration for negative group delay (NGD) values. Measurement and simulation results of a passive, fixed transmission line (TL) structure are presented along with an equivalent circuit model. Realized NGD values are observed from 20 to 24 GHz with a minimum value of -84 ps. By the addition of an accumulation-mode varactor the proposed circuit can be made tuneable; measured NGD values from 13.3 to 26.2 GHz are observed. These high speed circuits may be useful to minimize group delay (GD) variations generated by active and passive devices and thus can act as delay equalizers when placed in cascade. Concepts are illustrated by reducing GD in lowpass (LP), highpass (HP) and bandpass (BP) filters. The proposed circuits can be useful to reduce unwanted dispersion effects in silicon-based devices and systems and high speed interconnects at millimetre-wave frequencies.

I. INTRODUCTION

In high speed telecommunications, unwanted dispersion effects are problematic and can degrade overall system performance. Linear phase or flat group delay (GD) values are necessary to avoid distortion of high frequency signals. In the electrical domain, or more specifically in microelectronic circuit systems, equalizers can be used to compensate and minimize GDs introduced by transistor latency, transmission line (TL) interconnects, and circuit elements such as amplifiers, filters and oscillators [1]-[3].

Traditional equalization techniques using phase compensation have shown much promise [4] in reducing delay. But achieving negative GD values using low order designs may be difficult and thus the potential range of equalization can be limited. More recently printed, delay compensation circuits using metamaterial-based TL structures have been proposed [5], [6]. These design exhibit abnormal group velocities and negative group delays (NGDs) and thus offer new methods for GD equalization below 5 GHz [7], [8], [9]. Unfortunately, such passive metamaterial TL structures are generally limited by high insertion loss values, and in practice, amplifiers can be used to mitigate such losses [8], [10]-[12].

By the application of such metamaterial TL design concepts, two CMOS integrated circuits are presented in this work for millimetre-wave frequencies of operation. Other metamaterial-based TL structures have been implemented in CMOS [13], [14] but to the authors’ knowledge the proposed circuits are the first to offer NGD values in a standard CMOS technology. As shown in Fig. 1, passive metal-insulator-metal (MIM) capacitors and spiral inductors are placed in a TL configuration defining a single unit cell. By series loading of an RLC resonator, NGD values can be observed from 20 to 24 GHz. The proposed 0.18µm CMOS circuit can be made tuneable by inclusion of an active accumulation-mode NMOS varactor (within the RLC resonator) and measured NGD values are observed from 13.3 to 26.2 GHz. Losses can be reduced by the addition of a pre-amplifier and additional GD control may also be possible by further element tuning using active devices in the shunt or series branches of the compact CMOS circuit.

When placed in cascade with TL interconnects and common active or passive devices, the proposed CMOS circuits may be used as delay equalizers to minimize GD as illustrated in Fig. 2. For example, gain peaking in amplifiers or high Q filters may increase unwanted GD variations and thus the...
proposed NGD circuits may mitigate such effects. In addition, the presented CMOS circuits could also be placed at the termination of a network offering a low cost solution for GD reduction and correction in constructed high speed circuit systems. This equalization technique is investigated in a circuit example by reducing GDs of ideal lowpass (LP), highpass (HP) and bandpass (BP) filters [4] using an equivalent circuit model developed for the passive NGD circuit (Fig. 3). When GD is of concern the presented high speed CMOS circuits may offer some advantages over common allpass filters, delay equalization and phase compensation techniques [4] in terms of compactness, tunability and ease of design for silicon-based devices and high speed systems.

II. NEGATIVE GROUP DELAY TL STRUCTURES

Metamaterial TL structures [5], [6] offering NGDs [7] have been theoretically analyzed in the literature. Their dispersion properties can be described by regions of phase compensation, defined by right- and left-handed TL components within a unit cell; \( L_R, C_R, L_L \) and \( C_L \). Essentially, by the addition of a parallel RLC resonator \((L_{res}, C_{res} \text{ and } R_{res} \text{ embedded in series within each unit cell})\) NGD values can be observed near the resonant frequency of the RLC, \( f_{res} = \frac{1}{2\pi \sqrt{L_{res}C_{res}}} \), but at the cost of high insertion losses due to absorption of the resonator [7], [8]. In addition, high Q values \((Q = \frac{R_{res}}{\sqrt{L_{res}/C_{res}}} \text{ and } R_{res} \text{ embedded in series within each unit cell})\) can be observed near \( f_{res} \) [15]. Multiple unit cells can be placed in cascade for increased NGD values producing a region of anomalous dispersion [7].

In the time domain such circuits cause the output peak of a wave packet or signal, to precede the input. This interesting phenomenon can be described by casual pulse reshaping in which the TL structure generates a copy of the incident signal from initial transients [5].

III. CMOS DESIGN, IMPLEMENTATION & APPLICATIONS

The passive CMOS structures were fabricated in a low cost 0.18\(\mu\)m thick metal 6 CMOS process as shown in Fig. 1. Spiral inductors \((L_R, L_L \text{ and } L_{res})\) and metal-insulator-metal (MIM) capacitors \((C_R, C_L \text{ and } C_{res})\) define the completely lumped circuit elements. The compact TL structure was contained within a large ground plane, allowing for simple integration with other high speed CMOS circuits.

An equivalent circuit model of the unit cell (Fig. 3) was developed using a commercial circuit simulator (Agilent ADS) and modeled values were verified using II/T extraction techniques. Results were compared with measurements and full-wave simulations as shown in Figs. 4-6. A good agreement is achieved. Lumped element component values and equivalent circuit details are described in Table I. Positive phase slope values can be realized from 21.0 - 23.5 GHz (near the resonant frequency of the RLC, \( f_{res} = 21.7 \text{ GHz} \)), and as expected, high insertion loss values \((|S_{21}| \leq -15 \text{ dB})\) are observed from 20-25 GHz.
A. RLC Resonator Design for Negative Group Delay

It should be noted that the RLC resonator was implemented without the addition of a parallel resistor, $R_{res}$, reducing the required components of the NGD device. In fact, the low series losses of the spiral inductor were increased (as required for NGDs) by $Q^2 + 1$ when placed in parallel with the MIM capacitor [15]. Thus the simple parallel connection of a MIM capacitor and spiral inductor (with low loss, 3.25 $\Omega$) can realize the required RLC resonator.

B. Active Tuning of the Negative Group Delay CMOS Circuit

By replacing the $C_{res}$ MIM capacitor with voltage controlled varactors as shown in Fig. 7 the resonant frequency of the RLC can be tuned and thus NGD values can be varied from 13.3 to 26.2 GHz as shown in Fig. 8. A singly tuned accumulation-mode N-MOS varactor (256 fingers for each $2C_{var}$, nominal value of approximately 0.5 pF for zero bias) was utilized in the CMOS circuit. It is interesting to note that the active varactor elements introduced a positive delay (variation ≤ +65 ps) lowering the overall NGD when compared to the passive CMOS device. Additional varactors can be used in the TL sections and thus increased NGD tuning is possible. Such millimeter-wave active CMOS designs may be useful as tunable equalizers in high speed circuit systems when high GD variations are of concern.

C. Application to Delay Equalization

The proposed NGD CMOS circuits can also be placed in cascade with interconnects and common active and passive devices, and thus may be used as delay equalizers [4] to minimize GD variations in high speed circuit systems. Ideal LP, HP and BP filters [4] were designed in ADS and results were compared with and without the additional equalization circuit (in cascade) for GD reduction. Results and details of the investigated filters are shown in Figs. 9 and Table II. As expected the NGD circuit reduced GD variations for all three designs by more than 61.3%.

In addition, the LP Chebyshev filter response with and without delay equalization is shown in Figs. 9 (b) and (c). Reasonable insertion loss values are observed (with a maximum of 7.9 dB for the cascade configuration, while 15 dB for the passive NGD circuit) along with reduced group delay.

<table>
<thead>
<tr>
<th>Value</th>
<th>Design Notes</th>
<th>Circuit Detail</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{res}$</td>
<td>MIM Capacitor</td>
<td>8 x 12</td>
</tr>
<tr>
<td>$L_{res}$</td>
<td>Symmetrical Inductor</td>
<td>47 x 50</td>
</tr>
<tr>
<td>$C_R$</td>
<td>MIM Capacitor</td>
<td>8 x 12</td>
</tr>
<tr>
<td>$L_R$</td>
<td>Spiral Inductor</td>
<td>34 x 45</td>
</tr>
<tr>
<td>$L_L$</td>
<td>Symmetrical Inductor</td>
<td>37 x 40</td>
</tr>
</tbody>
</table>

| $C_{res}$ | 0.02075 pF | |
| $L_{res}$ | 0.2592 nH | $R_{res} = 382 \Omega$ |
| $C_R$ | 0.6672 pF | |
| $C_L$ | 0.8128 pF | |
| $L_R$ | 0.0902 nH | $R_{LR} = 33.5 \Omega$ |
| $L_L$ | 0.1187 nH | $R_{LR} = 4.8 \Omega$ |
The authors would like to thank CMC Microsystems for their assistance in fabrication.

ACKNOWLEDGMENT

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REFERENCES