A POSITIVE/NEGATIVE REFRACTIVE INDEX COPLANAR TRANSMISSION LINE IN CMOS FOR CONTROLLED INSERTION PHASE

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ABSTRACT: *A positive/negative refractive index coplanar transmission line is presented and used for phase control in CMOS circuits. Good performance has been achieved.* © 2008 Wiley Periodicals, Inc. Microwave Opt Technol Lett 50: 2227–2230, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23622

Key words: *metamaterials; coplanar waveguide (CPW); positive refractive index (PRI)/negative refractive index (NRI); phase; compensation; complementary metal oxide semiconductor (CMOS)*

1. INTRODUCTION

Periodic positive refractive index/negative refractive index (PRI/NRI) transmission line (TL) structures have been demonstrated for linear phase shifting, series power dividing, and antenna array feeding networks [1–4]. Such composite metamaterial lines are achieved by periodically loading a host TL with series capacitors and shunt inductors. By the addition of appropriate loaded elements, cascaded PRI/NRI TL structures have been designed for phase compensation below 5.6 GHz [5–11].

In this work, a low loss 3-unit cell PRI/NRI TL structure is presented offering zero insertion phase at 12.7 GHz with an insertion loss of ~0.6 dB/cell. The proposed design (see Fig. 1) consists of a host coplanar waveguide (CPW) PRI TL periodically loaded with low loss capacitive and inductive elements (C_0 and L_0) optimized for high frequencies of operation. These dominant NRI sections accrue a positive phase shift which compensates the phase lag inherent to the PRI CPW TL sections providing low loss continuous phase compensation above 5 GHz. Furthermore, a negligible variation in group delay is observed ($\Delta\tau_g = 0.1$ ns) above the Bragg cutoff frequency ($f_b = 2.06$ GHz). These results may be reasonable for such a high speed device in silicon and suggest that design methodologies previously implemented for similar low frequency devices can be applied at millimeter wave frequencies for low loss CMOS integrated circuits.

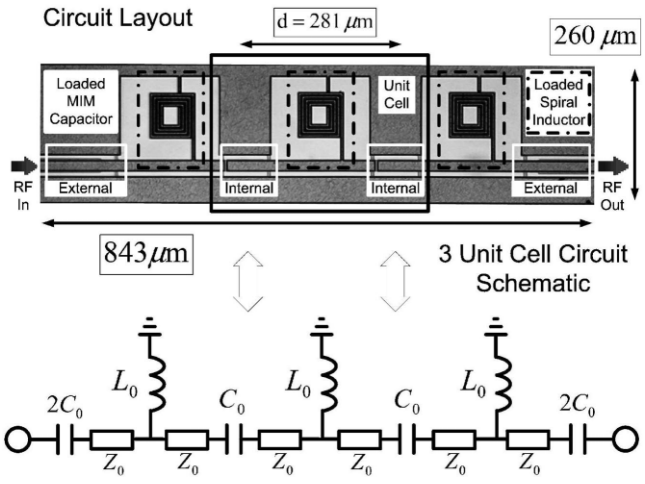

Figure 1 Layout and equivalent circuit schematic of the PRI/NRI 3-unit cell TL structure. Series MIM capacitors and shunt spiral inductors are periodically loaded within a host CPW TL. The total integrated circuit design was 843 by 260 μm (excluding pads) while each unit cell had a length of 281 μm

Specifically, a host CPW TL is loaded with four series metal-insulator-metal (MIM) capacitors and three lumped shunt spiral inductors in a standard CMOS process as shown in Figure 1. The entire circuit size, including all lumped elements but excluding pads, is 843 by 260 μm thus allowing for simple on-chip integration with very high speed analog circuits and digital components. In addition, the loaded lumped elements can be efficiently tuned for controlled low loss phase compensation at a desired frequency.

2. CONVENTIONAL PRI/NRL TL THEORY AND DISPERSIVE PROPERTIES

PRI/NRI TL structures have been theoretically analyzed in the literature and their dispersion properties are well known. The Bragg cutoff frequency defined in [1] for this unit cell configuration is

$$f_b = \frac{1}{4\pi\sqrt{L_0C_0}}, \tag{1}$$

with an additional stopband defined by cutoff frequencies

$$f_{c1} = \frac{1}{2\pi\sqrt{LC_0d}} \tag{2}$$

and

$$f_{c2} = \frac{1}{2\pi\sqrt{L_0Cd'}} \tag{3}$$

where L and C are the equivalent inductance and capacitance per unit length of the host TL which defines the characteristic impedance $\left(Z_0 = \sqrt{\frac{L}{C}}\right)$ and d is the unit cell length [12].

Positive phase advance is realizable between f_b and f_{c1} defining a high pass (HP) region. Physically, a backward traveling wave with a negative phase velocity ($v_\phi < 0$) and NRI can be observed in this region. Conversely, inherent phase lag occurs above f_{c2} and describes the low pass (LP) nature of conventional PRI TLs. Furthermore, by equating f_{c1} and $f_{c2'}$, stopband closure can be achieved providing zero insertion phase at a desired frequency, f_0. If a negligible phase shift is assumed in the PRI TL sections, a matching condition can be derived, as shown in [1],

$$Z_0 = \sqrt{\frac{L_0}{C_0}}. \tag{4}$$

The total insertion phase of such a matched structure ($\phi_{\text{structure}}$) for frequencies near f_0 is provided in [9],

$$\phi(\omega)_{\text{structure}} \approx N[\phi_{\text{HP}}(\omega) + \phi_{\text{LP}}(\omega)] \tag{5}$$

where the high pass (ϕ_{HP}) and low pass (ϕ_{LP}) phase contributions are defined by

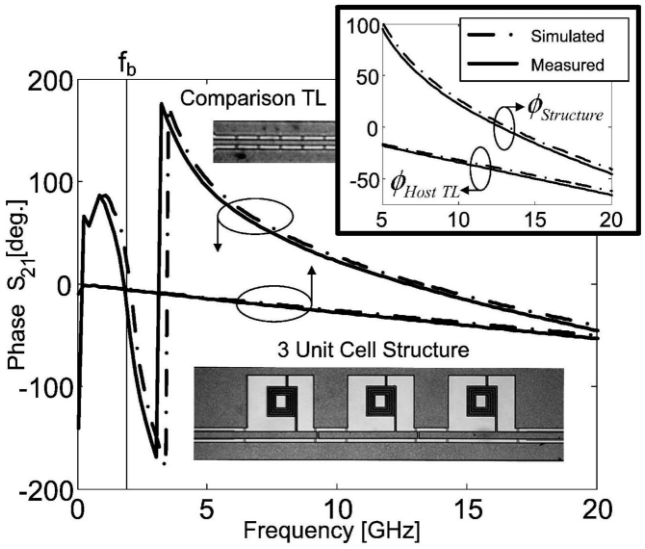

Figure 2 Simulated and measured insertion phase of the CMOS 3-unit cell TL structure with zero insertion phase observed at 12.7 GHz. The cutoff frequency f_b is shown illustrating the $v_\phi < 0$ region. (Note: Photos shown with inconsistent scales)

$$\phi_{HP}(\omega) \approx -\frac{1}{\omega\sqrt{L_0C_0}}, \tag{6}$$

$$\phi_{LP}(\omega) = \phi_{HostTL} \approx \beta_{TL}d \tag{7}$$

and N is the number of unit cells, $\beta_{TL} = \omega\sqrt{LC}$ is the propagation constant of the host TL and d is the length of one unit cell.

3. DESIGN AND EXPERIMENTAL IMPLEMENTATION

The host CPW TL standard and phase compensating structure were fully integrated in a typical 0.18-μm thick metal 6 CMOS process. For this structure, C_0 =1.1 pF, L_0 = 1.356 nH, Z_0 = 35 Ω, d = 281 μm, and $\beta_{TL}d$ = 0.426 rad. The low loss host CPW TL (−1.025 dB/mm) was designed for a good match to the loaded elements with a center strip width of 20 μm and separation of 10 μm. The proposed phase compensating structure is shown in Figure 1 and is composed of 3-unit cells of total size 843 by 260 μm (excluding pads). The two 1.1 pF internal MIM capacitors (C_0) have a size of 20 by 70 μm. To achieve a good input and output match, the internal MIM capacitors were approximately doubled in length to implement the two external MIM capacitors ($2C_0$]). Three 1.356 nH (simulated Q of 7.2) shunt spiral inductors (L_0) were periodically embedded within one of the host CPW TLs ground planes, having a footprint of 85 by 85 μm, each with 4.25 loops, a trace width of 5 μm and trace separation of 1.5 μm.

4. RESULTS AND DISCUSSION

The proposed phase compensating structure and CPW TL standard were initially designed using a full-wave Method of Moments simulator and then fabricated in a standard CMOS process. The phase compensating chip and CPW TL standard were measured using an HP 8510 vector network analyzer and pads were de-embedded using short, open and through calibration test structures. The simulated and measured insertion phases are in good agreement, as shown in Figure 2. The phase compensating structure offered zero insertion phase at f = 12.7 GHz.

The phase advancing nature of the high pass loaded elements is observed in Figure 3 for the 3-unit cell circuit (by calculating

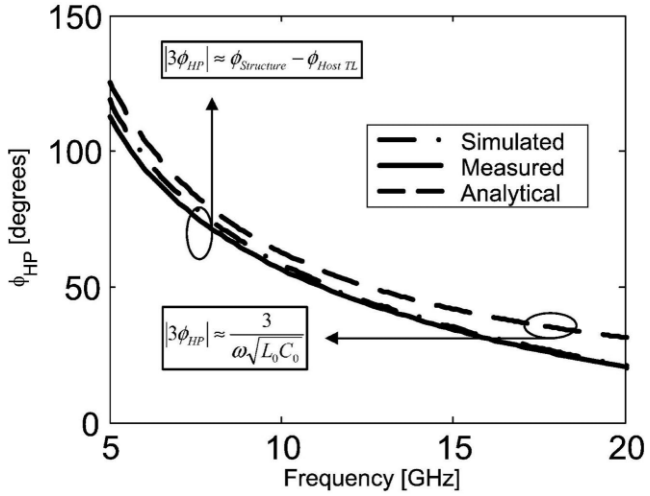

Figure 3 The high pass response of the loaded elements is shown for the 3-unit cell circuit (by calculating $|3\phi_{HP}| \approx \phi_{Structure} - \phi_{HostTL}$) illustrating the phase advancing nature. A comparison is made to Eq. (**6**) for C_0 = 1.1 pF and L_0 =1.356 nH and simulated and measured values are in good agreement for the 3-unit cells

$|3\phi_{HP}| \approx \phi_{Structure} - 3\phi_{LP} \approx \phi_{Structure} - \phi_{HostTL}$ from measured values) and a comparison is made to Eq. (6) for the loaded elements (C_0 = 1.1 pF and L_0 = 1.356 nH), with simulated and measured values in good agreement. This phase advance (−5°/GHz) was linear, implying flat group delay values with negligible group delay variation ($\Delta\tau_g$ = 0.1 ns) above 5 GHz as shown in Figures 2 and 4, respectfully.

The theoretical dispersion properties of Eq. (1) accurately predicted the theoretical Bragg cutoff frequency (2.06 GHz). For instance at 2.0 GHz, the insertion loss is greater than 10 dB, suggesting stopband behavior. Furthermore, the simulated and measured insertion and return loss values are in good agreement as shown in Figure 5 for the 3-unit cell structure. All return loss values are less than 10 dB for $f > 2.5$ GHz, with an insertion loss of ~1.80 dB at f = 12.7 GHz. Furthermore, an insertion loss of 2.15 dB (at worst) is observed in the high pass region for the phase

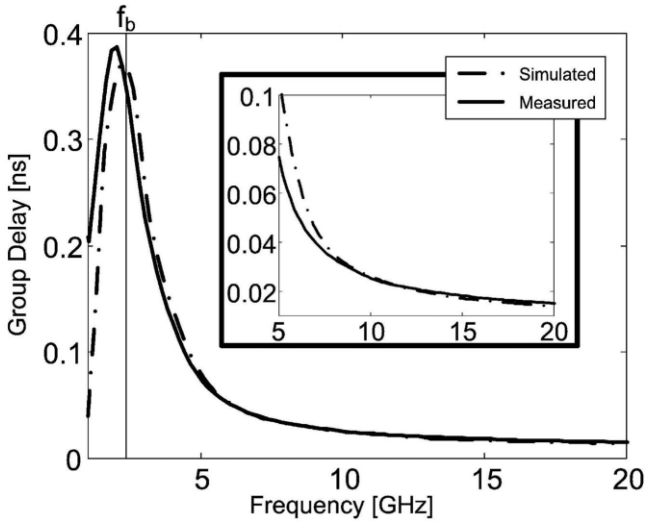

Figure 4 Simulated and measured group delay (τ_g) of the CMOS 3-unit cell TL structure. A negligible variation in group delay is observed ($\Delta\tau_g$ = 0.1 ns) above 5 GHz

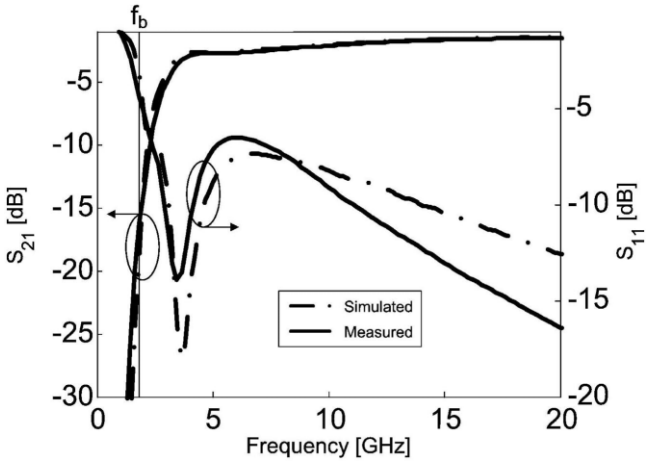

Figure 5 Simulated and measured insertion and return loss of the phase advance NRI TL structure. At worst, an insertion loss of 2.15 dB is observed (0.72 dB/cell), which may be acceptable for such a passive CMOS circuit at high frequencies

compensating device. By further tuning of the loaded elements and number of unit cells, additional high frequency low loss designs can be implemented for controlled insertion phase with flat group delay values.

5. CONCLUSION

In this work, a completely integrated continuous phase compensating TL structure is presented using low loss PRI/NRI TL metamaterials for high frequency applications. Loaded series MIM capacitors and shunt spiral inductors within a host CPW TL have led to a practical CMOS structure offering suitable phase advance and flat group delay values above 5 GHz. Specifically, the proposed 3-unit cell structure offers zero insertion phase at 12.7 GHz with an insertion loss of ~0.6 dB/cell. In addition, the dominant high pass response of the loaded elements is compared to analytical insertion phase values and results are in good agreement.

Similar PRI/NRI TL designs have been presented in the literature [1–11] offering phase compensation below 5.6 GHz. Thus the novelty of the proposed design is that PRI/NRI TL structures can be designed at millimeter wave frequencies for low loss CMOS integrated circuits.

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NOVEL BAND-NOTCH UWB ANTENNA DESIGN WITH SLIT GROUND PLANE

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ABSTRACT: *A newly designed microstrip feed, octagonal-shaped ultra-wideband printed antenna is proposed. The UWB operation within the required 3.1–10.6 GHz band is achieved by simply embedding in the ground plane a small rectangular slit, located below the feed line of an octagonal patch. With the dimensions (length and height) of the slit carefully tuned, a notched band of around 5.1–6.4 GHz can be achieved, without applying the commonly recommended techniques of loading the radiating patch with a slot or an open-ended slit.* © 2008 Wiley Periodicals, Inc. Microwave Opt Technol Lett 50: 2229–2233, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23621

Key words: *UWB; band-notch; monopole antenna*

1. INTRODUCTION

In recent years, there has been an elevated interest in the antenna design for ultra-wideband communication systems, which operate between 3.1 and 10.6 GHz. For printed UWB monopole antenna design, besides the most common shapes such as the circular and rectangular ones, many other peculiar monopole antenna shapes have also been reported recently [1, 2]. Since the wireless local-area network (WLAN) system operating band for IEEE 802.11 a/b/g is between 5.15 and 5.825 GHz, to avoid interferences, a desirable band-notch function within this 5-GHz band will be necessary. A number of techniques have been recommended in the literature to excite a band-notch function for a printed UWB monopole antenna. Among these band-notched techniques, loading the radiating patch with a U-slot (or inverted U) is the most popular one [3]. Other new design methods such as loading a pair of symmetrical open-ended slits on the radiating patch [4, 5], inserting a pair of symmetrical parasitic strips [5, 6], and embedding a $\lambda/4$ resonant circuit (small slot) on the feed line [7], can also lead to a band-notch function within the 5-GHz range. In [5], three