# Composite Right/Left Handed Artificial Transmission Line Structures in CMOS for Controlled Insertion Phase at 30 GHz

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*Received 2 January 2008; accepted 20 April 2008*

**ABSTRACT: Two CMOS integrated circuits are presented that utilize metamaterial composite right/left handed (CRLH) transmission lines (TLs) for zero insertion phase at 30 GHz. Specifically, 2 and 3 unit cell structures are presented with controlled insertion phase that is achieved by cascading lumped element capacitors and spiral inductors in an LC network configuration defining the TL unit cells. Furthermore, the fixed TL structures suggest the possibility of zero, advanced or delayed insertion phases by element variation, or by the use of simple active components. Simulation and measured results are in good agreement with CRLH TL theory, and display a linear insertion phase and flat group delay values that are dependent on the number of unit cells with an insertion loss of ~0.8 dB per cell. These findings suggest that such high speed CRLH TLs structures can be implemented for linear array feeding networks and compact antenna designs in CMOS at millimeter wave frequencies.** © 2008 Wiley Periodicals, Inc. Int J RF and Microwave CAE 19: 163–169, 2009.

**Keywords:** composite right and left handed (CRLH); transmission lines (TLs); right-handed (RH); left-handed (LH); group delay (GD); metal-insulator-metal (MIM); complementary metal oxide semiconductor (CMOS)

## I. INTRODUCTION

Composite, right and left handed (CRLH) metamaterial transmission lines (TLs) have been utilized in the design of many guided and radiated wave applications [1–5]. Such devices are achieved by cascading right-handed (RH) and left-handed (LH) TLs sections in an LC ladder configuration defining a unit cell [6, 7]. By using appropriate CRLH TLs, many passive and active microwave circuits have been designed for linear phase shifting in various circuit topologies for operation below 17 GHz [8–15]. Such structures can offer zero, leading or lagging insertion phases over a specific frequency span with flat group delay values. Recently, the completely integrated design described in Ref. 15 suggested an active tuning range from $-35^\circ$ to $+59^\circ$ at 2.6 GHz, with a bandwidth of 1.9 GHz in a 0.13-$\mu$m CMOS process. This design offered commendable results with an insertion loss of 3.8 dB (at worst) for a single unit cell with a footprint of $380 \times 960$ $\mu$m.

By the application of CRLH TL theory, 2 and 3 unit cell CMOS integrated circuits are presented in

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DOI 10.1002/mmce.20336
Published online 20 August 2008 in Wiley InterScience (www.interscience.wiley.com).

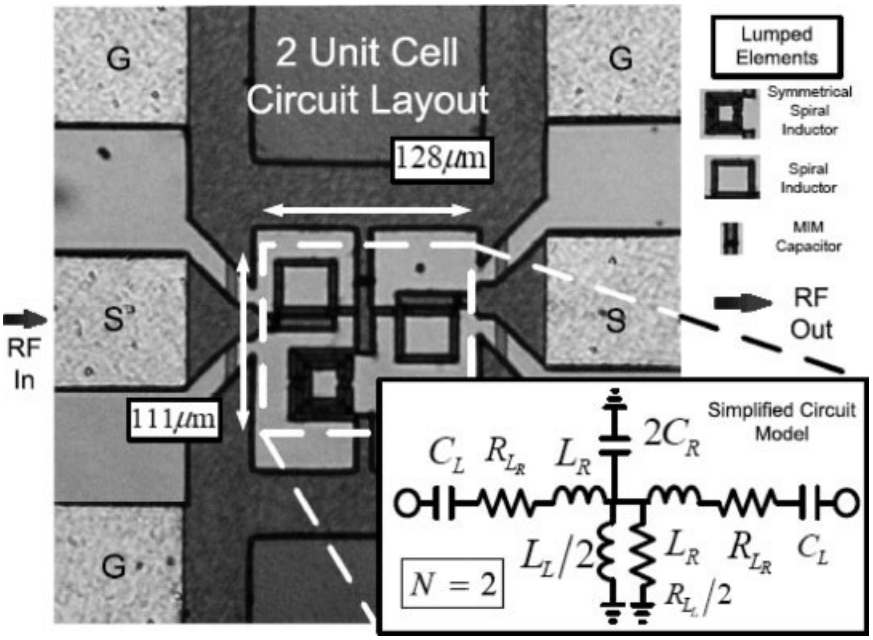


**Figure 1.** Fully integrated 2 unit cell CMOS circuit designed for zero insertion phase at 30 GHz. Square and symmetrical inductors and MIM capacitors define the metamaterial CRLH TL unit cell. A simplified circuit model was employed to analyze the TL structures.

this work with more than an order of magnitude increase in center frequency when compared to Ref. 15. The proposed structures offer zero insertion phase at 30 GHz with an insertion loss of ~0.8 dB per unit cell. Reflection loss values are below 15 dB from 20 to 40 GHz for the presented 2 and 3 unit cell designs (respective size: 111 × 128 $\mu$m and 111 × 192 $\mu$m, excluding pads, in a standard 0.18 $\mu$m CMOS process). In addition, a theoretical group delay (GD) analysis is also developed from standard CRLH TL theory and verified with measured and simulated results. Knowledge of such GD variation is essential in such high speed integrated circuits. Specifically, a GD of 5.8 ps/cell is observed at 30 GHz with a GD variation of 9.4 ps/cell from 15 to 35 GHz. Thus, the investigated TLs also offer flat GD values that are proportional to the number of unit cells. Furthermore, the TL structures suggest the possibility of zero, advanced or delayed insertion phases with flat GD values for such high frequencies of operation. In addition, these passive structures can be extended to include simple active components (such as varactors or tunable inductors) for varied insertion phase values at a single frequency.

The fixed 2 and 3 unit cell structures, shown in Figures 1 and 2 are experimentally investigated and verified against CRLH TL theory and equivalent circuit models. Results are in good agreement for such simple analytical equations and straightforward circuit representations. All fabricated circuit elements are completely lumped, defining a CRLH unit cell design. The RH TL sections are implemented by series spiral inductors and shunt metal-insulator-metal (MIM) capacitors. Conversely, shunt symmetrical inductors and series MIM capacitors define the LH TL segments. The fabricated circuits are contained within a large ground plane allowing for easy integration with conventional high speed CMOS circuits.

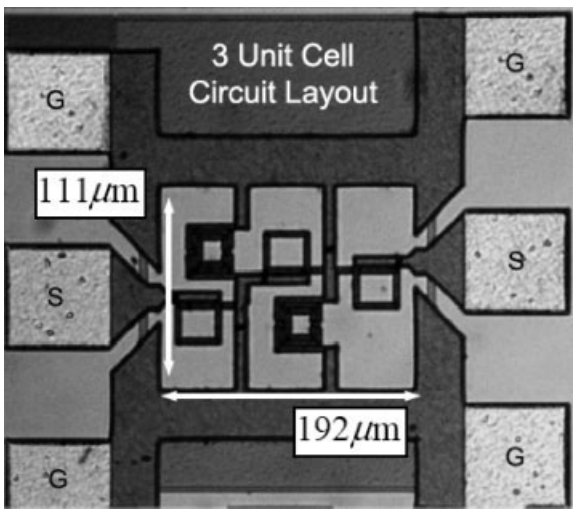


**Figure 2.** Fabricated 3 unit cell CMOS metamaterial TL.

## II. CRLH TL THEORY

CRLH metamaterial TL structures have been theoretically analyzed in the literature. Their dispersion properties describe a bandpass filter offering phase compensation confined by RH lowpass and LH highpass cutoff frequencies [16],

$$f_{\mathrm{C}}\mathrm{RH} = \frac{1}{\pi\sqrt{L_{\mathrm{R}}C_{\mathrm{R}}}} \tag{1}$$

and

$$f_{\mathrm{C}}\mathrm{LH} = \frac{1}{4\pi\sqrt{L_{\mathrm{L}}C_{\mathrm{L}}}}. \tag{2}$$

For zero insertion phase the RH and LH TL characteristic impedances, $Z_{\mathrm{O}}\mathrm{R}$ and $Z_{\mathrm{O}}\mathrm{L}$, should be matched as described in Ref. 3,

$$Z_{\mathrm{O}}\mathrm{R} = Z_{\mathrm{O}}\mathrm{L} = \sqrt{\frac{L_{\mathrm{R}}}{C_{\mathrm{R}}}} = \sqrt{\frac{L_{\mathrm{L}}}{C_{\mathrm{L}}}}. \tag{3}$$

For this matched condition, the total insertion phase of the CRLH unit cell can be determined by the addition of the RH and LH TL phase contributions,

$$\phi(\omega) \approx \phi(\omega)^{\mathrm{RH}} + \phi(\omega)^{\mathrm{LH}}. \tag{4}$$

The insertion phase can be defined for near zero values at a specific center frequency ($f_{\mathrm{O}}$) as described in Ref. 16,

$$\phi(\omega = 2\pi f[f \to f_{\mathrm{O}}]) \approx -2\pi f\sqrt{L_{\mathrm{R}}C_{\mathrm{R}}} + \frac{1}{2\pi f\sqrt{L_{\mathrm{L}}C_{\mathrm{L}}}}, \tag{5}$$

where

$$f_{\mathrm{O}} = \frac{1}{2\pi\sqrt[4]{L_{\mathrm{R}}C_{\mathrm{R}}L_{\mathrm{L}}C_{\mathrm{L}}}}. \tag{6}$$

Thus, zero insertion phase ($\phi \approx 0$) can be achieved at a desired frequency, $f_{\mathrm{O}}$, by variation of $L_{\mathrm{R}}$, $C_{\mathrm{R}}$, $L_{\mathrm{L}}$, and $C_{\mathrm{L}}$ assuming eq. (3) is satisfied. The total insertion phase for an $N$ unit cell structure can be defined [4],

$$\Phi(\omega) \approx N\phi(\omega), \tag{7}$$

and characterized within a bandwidth region, by $Y(f) = \frac{\Phi(\omega)}{2\pi} = \frac{N\phi(\omega)}{2\pi}$, in °/GHz.

The GD for a single unit cell, $\tau_{\mathrm{g}}(\mathrm{f})$, can also be derived from eq. (5)

$$\tau_{\mathrm{g}}(\mathrm{f}) = -\frac{\partial\phi(\omega = 2\pi f)}{\partial\omega} = \sqrt{L_{\mathrm{R}}C_{\mathrm{R}}} + \frac{1}{(2\pi f)^2}\frac{1}{\sqrt{L_{\mathrm{L}}C_{\mathrm{L}}}}. \tag{8}$$

Furthermore, for high frequencies the $L_{\mathrm{R}}$ and $C_{\mathrm{R}}$ terms dominate and $\tau_{\mathrm{g}}(\mathrm{f})$ approaches that of a purely RH TL with flat GD values,

$$\tau_{\mathrm{g}} \approx \sqrt{L_{\mathrm{R}}C_{\mathrm{R}}}. \tag{9}$$

Thus the total $\tau_{\mathrm{g}}(\mathrm{f})$ for an $N$ unit cell structure can be defined, $T_{\mathrm{g}} = N\tau_{\mathrm{g}} = N\sqrt{L_{\mathrm{R}}C_{\mathrm{R}}}$.

## III. CMOS DESIGN AND IMPLEMENTATION

The CMOS CRLH TL unit cells were defined by RH and LH lumped elements. Specifically, the 2 and 3 unit cell structures were designed for zero insertion phase at $f_0 = 30$ GHz and were fully integrated in a low cost 0.18-$\mu$m thick metal 6 CMOS process as shown in Figures 1 and 2. Series spiral inductors, $L_{\mathrm{R}}$, and shunt MIM capacitors, $C_{\mathrm{R}}$, define the RH sections, while shunt symmetrical inductors, $L_{\mathrm{L}}$, and series MIM capacitors, $C_{\mathrm{L}}$, represent the LH sections. The LH TLs accrual a positive phase shift which compensates the phase lag apparent from the RH TL segments [4]. By a periodic configuration of RH and LH TL sections, zero insertion phase can be achieved at a desired frequency, $f_0$, by variation of $L_{\mathrm{R}}$, $C_{\mathrm{R}}$, $L_{\mathrm{L}}$, and $C_{\mathrm{L}}$ and assuming eq. (3) is satisfied.

### A. Design Process

A goal of zero insertion phase was set at $f_0 = 30$ GHz. Then, to assist in the design, a simple circuit model (Fig. 1) was employed. Individual component values were determined using eq. (5) and then applied to the 2 and 3 unit cell designs. With the assistance of a full wave method of moments simulator, the required lumped elements were realized and values were verified with standard $\Pi/T$ parameter extraction techniques [17]. Next, the determined lumped elements were appropriately arranged in silicon and the 2 and 3 unit cell CRLH TL structures were fabricated.

The realized 2 and 3 unit cell designs are described as follows. The shunt 0.0357 and series 0.29 pF MIM capacitors have a footprint of 8 × 10

**TABLE I. Realized CRLH TL Characteristics**

| Unit Cell Value | | Design Notes | Circuit Detail |
|---|---|---|---|
| | | Lumped element | Size [$\mu$m] |
| $C_R$ | 0.0715 pF | MIM capacitor | 8 × 10 |
| $C_L$ | 0.29 pF | MIM capacitor | 8 × 32 |
| $L_R$ | 0.094 nH | Spiral inductor | 34 × 35 |
| $L_L$ | 0.383 nH | Symmetrical inductor | 37 × 40 |
| | | Characteristic Impedance | RH/LH TL Size [$\mu$m] |
| $Z_O$R | 36.26 Ω | $Z_O$R/$Z_O$L = 0.99772 | 58 × 69 |
| $Z_O$L | 36.34 Ω | $Z_O$L/$Z_O$R = 1.0023 | 86 × 101 |
| | Theory | Filter Properties | Measured |
| $f_O$ | 30.45 GHz | Design frequency | 30 GHz |
| $f_C$RH | 122.8 GHz | RH lowpass cutoff | Not Av. |
| $f_C$LH | 7.55 GHz | LH highpass cutoff | 8 GHz |
| $T_g$ | 10.5 ps | GD ($N$ = 2), at $f_0$ | 10.6 ps |
| $T_g$ | 15.8 ps | GD ($N$ = 3), at $f_0$ | 18.2 ps |

and 32 × 8 $\mu$m, respectively. While the shunt 0.766 and 0.094 series nH spiral inductors have a footprint of 39.5 × 37 and 34 × 35 $\mu$m, respectively. The 2 and 3 unit cell structures have a total size of 111 × 128 and 111 × 192 $\mu$m (excluding pads), respectively.

Square spiral inductors were utilized in the series branches each with 1.25 loops, a trace width of 5 $\mu$m and trace separation of 1.5 $\mu$m. For the shunt branches, symmetrical spiral inductors with two loops were employed with similar trace widths and separations to that of the series inductors. Also, simulated results suggest inductor quality values of 4.8 and 7.9 for the square and symmetrical inductors, respectively.

## B. CRLH Unit Cell Component Values

By additional extraction analysis, the component values were determined as shown in Table I. The RH and LH TL sections are described by $C_R$ = 0.0715 pF, $L_R$ = 0.094 nH, $C_L$ = 0.29 pF and $L_L$ = 0.383 nH. By eq. (3), these values imply a relatively matched design, $Z_O R \approx Z_O L$ (ratio $\frac{Z_O R}{Z_O L} = 0.998$), suggesting a linear phase response and flat GD values for the CRLH TL structures.

## C. Equivalent Circuit Representation

The CRLH TL structures were modeled by equivalent circuits (Fig. 1) using the Agilent-Advanced Design System (ADS) microwave circuit simulator. Appropriate losses were introduced using 0.18 $\mu$m CMOS lumped element models. Simulated, analytical and measured results are in good agreement as shown in Figures 3, 4, 5, and 7, displaying the insertion phase, return loss values, and regions of phase wrapping.

## IV. MEASURED RESULTS AND DISCUSSION

The two proposed CMOS circuits were measured using a HP 8510 vector network analyzer and pads de-embedded using short, open and through calibra-

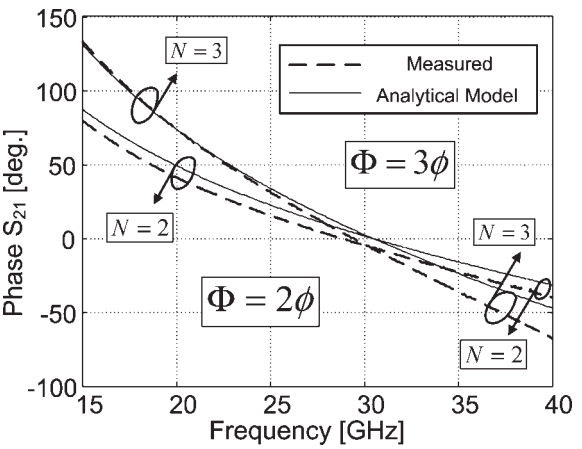


**Figure 3.** Measured insertion phase for the 2 and 3 unit cell structures and comparison to analytical model of eq. (5). The phase was linear and proportional to the number of unit cells, $N$, suggesting flat GD values. Negligible insertion phase was observed near the design frequency, $f_O$, suggesting phase advance from $f_C$LH → $f_O$ and phase lag from $f_O$ → $f_C$RH. Deviations between the measured and simulated values could be minimized if second and third order parasitics were included in the CRLH TL analytical model.

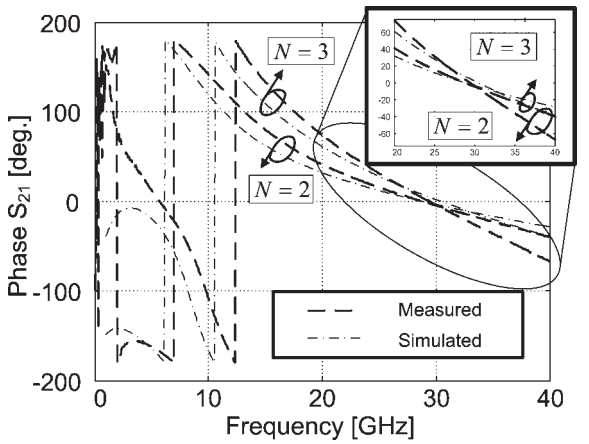


**Figure 4.** Simulated and measured insertion phase for the investigated structures.

tion test structures. Realized CRLH TL characteristics are described for the unit cell in Table I. Measured results were compared to the analytical and simulated values (Figs. 3–7), and are in good agreement. A noticeable passband was realized suggesting phase lead below $f_O$ and phase lag above the design frequency. In addition, the total linear insertion phase ($Y \approx -2.3\ N^\circ$/GHz) and flat GD values ($T_g \approx 5.8\ N$ ps at $f_O$ with a variation, $\Delta T_g \approx N\ 9.4$ ps from 15–35 GHz) were proportional to the number of unit cells, $N$ as shown in Figures 3–6.

## A. Insertion Phase

The zero insertion phase point, $\Phi \approx 0$, was accurately predicted by the calculated center frequency [eq. (6)], with atmost 450 MHz variation in the simulated and measured results as shown in Figure 7b. Such inaccuracies may have developed since second order parasitics were omitted in the analysis for simplicity. Similar inconsistencies are seen in the return and insertion loss values as shown in Figure 7. Regardless, all results are in good agreement suggesting the analytical and equivalent circuit models are reasonable for a first order approximation and that these simple models may be used to predict the response of higher order unit cell structures.

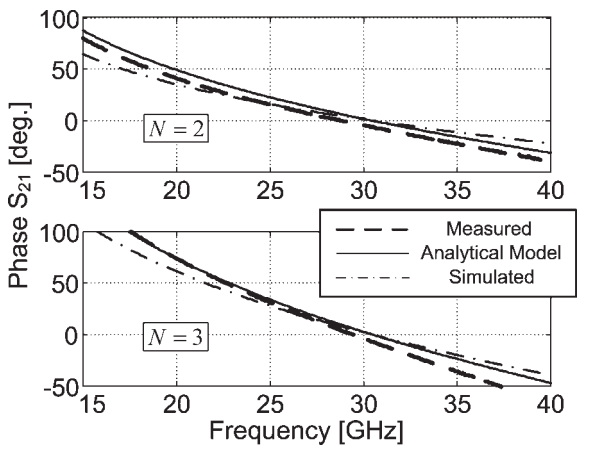


**Figure 5.** The measured and simulated insertion phase for the 2 and 3 unit cell structures and comparison to the analytical model.

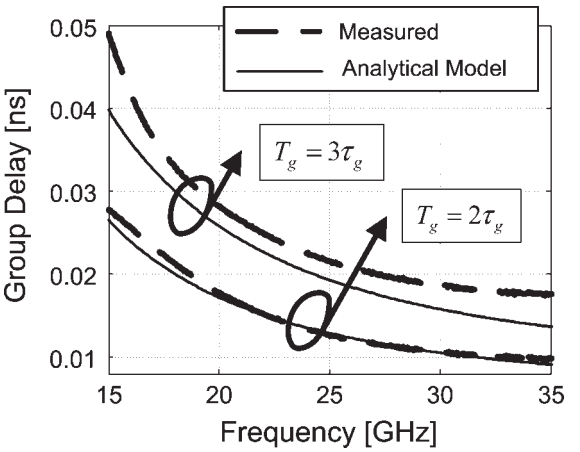


**Figure 6.** Measured GD for the 2 and 3 unit cell structures and comparison to analytical model of eq. (8). The GD variation was proportional to the number of unit cells, $\Delta T_g \approx N\ 9.4$ ps from 15–35 GHz. Deviations are observed for the 3 unit cell device and can be attributed to the simple group delay model; at 30 GHz the deviation is less than 15% and thus the suggested first order approximation of the group delay may be suitable.

## B. High Frequency Modeling

Slight deviations can be observed between the analytical and measured values for the 3 unit cell structure as shown in Figures 3 and 6. For instance, the deviation in the group delay for the 3 unit cell device at 30 GHz is less than 15%. Such deviations can be minimized if element coupling and second and third order parasitics are included in the CRLH TL analytical model. For instance, in the fabricated 2 [three] unit cell design there are 3 [five] spirals inductors that are closely packed and thus element coupling may occur realizing an effective value for the lumped element components. Thus the analytical model is useful for a first order approximation for small unit cell devices, but full wave electromagnetic simulation tools may be needed for increased accuracy in higher order designs.

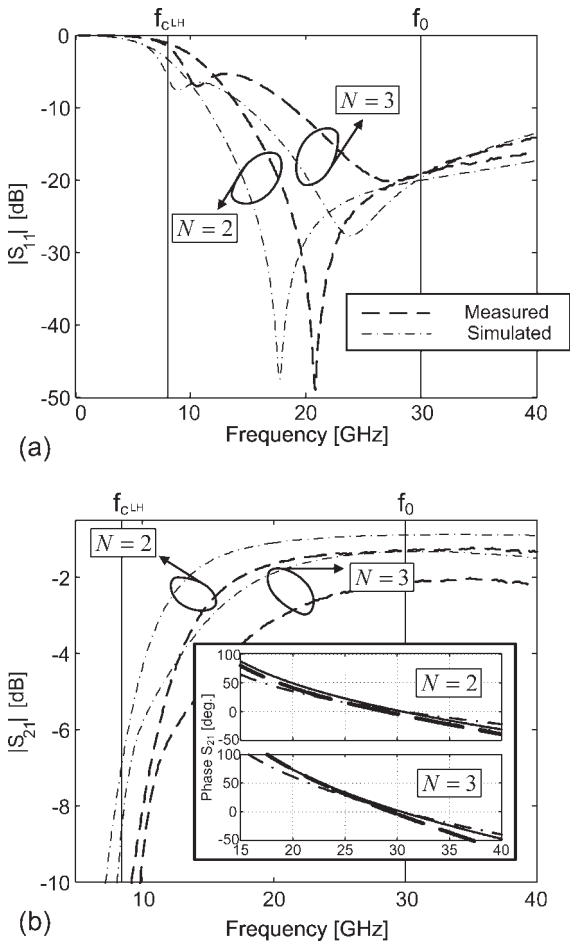


**Figure 7.** Comparison of measured and simulated return loss (a) and insertion loss (b) for the 2 and 3 unit cells. The measured (—) and simulated (–·–) insertion phase is also compared to the analytical model (–) as shown in (b).

## C. Dispersion Characteristics and Filter Response

The theoretical dispersion properties of eqs. (2)–(6) accurately predicted the LH highpass cutoff frequency ($f_C$LH = 7.55 GHz). For frequencies below 5 GHz, the insertion loss was greater than 10 dB, suggesting stopband behavior. The RH lowpass cutoff frequency ($f_C$RH = 122.8 GHz) could not be verified due to measurement device limitations. Regardless, a considerable passband was realized using the CRLH TL structures, suggesting phase advance from $f_C$LH $\rightarrow f_O$, zero insertion phase at $f_O$ and phase lag from $f_O \rightarrow f_C$RH. In addition, the total insertion phase slope was linear and dependent on the number of unit cells.

The simulated and measured reflection losses are shown in Figure 7a for the 2 and 3 unit cell TL structures. Measured values less than −18 dB at the design frequency of 30 GHz are obtained for the 3 unit cell design. In addition, simulated and measured insertion loss values are in good agreement as shown in Figure 7b. At worst, a loss of 2 dB is measured at $f_O$ for the 3 unit cell TL structure. These results are reasonable and may be acceptable for such high frequency passive structures in silicon.

## V. INTEGRATED ANTENNA APPLICATIONS

Similar metamaterial structures have been utilized in the design of various antenna configurations [1, 3, 5]. In addition, such phase shifters have been suggested for linear array feeding networks [4, 18]. Thus, the presented CRLH TL structures are applicable to comparable integrated circuit designs for compact and high frequency applications.

## VI. CONCLUSION

A completely integrated linear insertion phase structure is presented using low loss metamaterial CRLH TLs. An LC ladder network of series MIM capacitors and spiral inductors has led to the development of practical CMOS structures offering zero insertion phase at 30 GHz. Particularly, 2 and 3 unit cell CMOS structures were fabricated and verified against CRLH TL theory and equivalent circuit models. Such TL structures have applications for compact antenna designs and array feeding networks in CMOS. Results are in good agreement and display a linear insertion phase and flat group delay values that are dependent on the number of unit cells.

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