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Fabrication and characterization of pentacene-based transistors with a room-temperature mobility of 1.25 cm^2/Vs

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Abstract

Pentacene-based transistors produced by a novel neutral cluster beam deposition method were characterized, and the effects of the surface pretreatments were examined. Atomic force microscopy and X-ray diffraction showed that the cluster beams were quite efficient in growing high-quality, crystalline thin films on SiO_2 substrates at room-temperature without any thermal post-treatment, and that an amphiphilic surfactant, octadecyltrichlorosilane (OTS), enhances the packing density and crystallinity significantly. The observed field-effect mobilities (μ_{eff}) were among the best reported thus far: 0.47 and 1.25 cm^2/Vs for the OTS-untreated and -pretreated devices, respectively. The device performance was found to be consistent with the estimated trap density and activation energy, which were derived from the transport characteristics for the temperature dependence of μ_{eff} in the range of 10–300 K.

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Keywords: Pentacene; Neutral cluster beam deposition (NCBD); Organic thin-film transistor; Octadecyltrichlorosilane (OTS); Temperature dependence of field-effect mobility (μ_{eff})

1. Introduction

The recent advances in organic-based semiconductor electronics have led to them being viewed as potential alternatives to traditional silicon-based devices. The macroscopic properties of organic crystalline solids formed by weak van der Waals interactions are governed by the individual molecules, which makes the concept of molecular engineering feasible. The promising applications of these solids include optoelectronic devices such as thin-film transistors, light emitting diodes, photovoltaic cells, etc. Some of these transistors have comparable performance to that of hydrogenated amorphous Si devices. This is well illustrated by the devices fabricated using fused-ring polycyclic aromatic hydrocarbons such as pentacene, a π-conjugated molecule consisting of five aligned condensed benzene rings [1–13].

The preparation of good thin-film crystals is essential for fabricating high-quality, organic thin-film transistors. The neutral cluster beam deposition

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(NCBD) method used in this study is a less popular, but quite useful deposition scheme [14]. In recent years, we have reported a series of optoelectronic devices fabricated using the NCBD approach [15–20]. Neutral cluster beams consisting of weakly bound molecules (Fig. 1) are produced when organic molecules evaporated by resistive heating undergo adiabatic expansion in a high vacuum. The unique characteristics of these beams are their high translational kinetic energy and directionality. The collision of cluster beams with a room-temperature substrate induces facile decomposition of the clusters into individual molecules and the subsequent energetic migration of these molecules results in the formation of smooth, uniform thin films. The NCBD scheme allows for a significant improvement in the surface morphology, crystallinity, and packing density of these films. In particular, the distinctive advantage of this method lies in the fact that thin-film formation proceeds on a substrate maintained at room temperature. The absence of thermal post-treatment is of very practical significance in terms of the device fabrication. Such a favorable procedure cannot be achieved by conventional vapor deposition techniques.

This paper reports our characterization study of pentacene-based, top-contact transistors prepared on room-temperature SiO_2 substrates using a novel NCBD method. The pretreatment effects of an amphiphilic surfactant, octadecyltrichlorosilane (OTS), on the device performance as well as the transport mechanisms in the temperature range of 10−300 K are reported. The transistor characteristics, which were found to be among the best reported thus far, are also discussed.

2. Experimental

For the fabrication of the top-contact transistors, a highly doped, n-type Si wafer coated with an Al layer was used as the gate electrode, and a thermally grown 2000 Å-thick SiO_2 layer was used as the gate dielectric [15]. Fig. 1 shows a schematic diagram of the process. The substrates were first cleaned by a series of successive ultrasonic treatments in acetone, hot trichloroethylene, acetone, HNO_3, methanol and deionized water in order and then blown with dry N_2 [21]. The substrates were finally exposed to UV (wavelength of 254 nm) for 15 min. For the OTS pretreatment, the cleaned substrates were

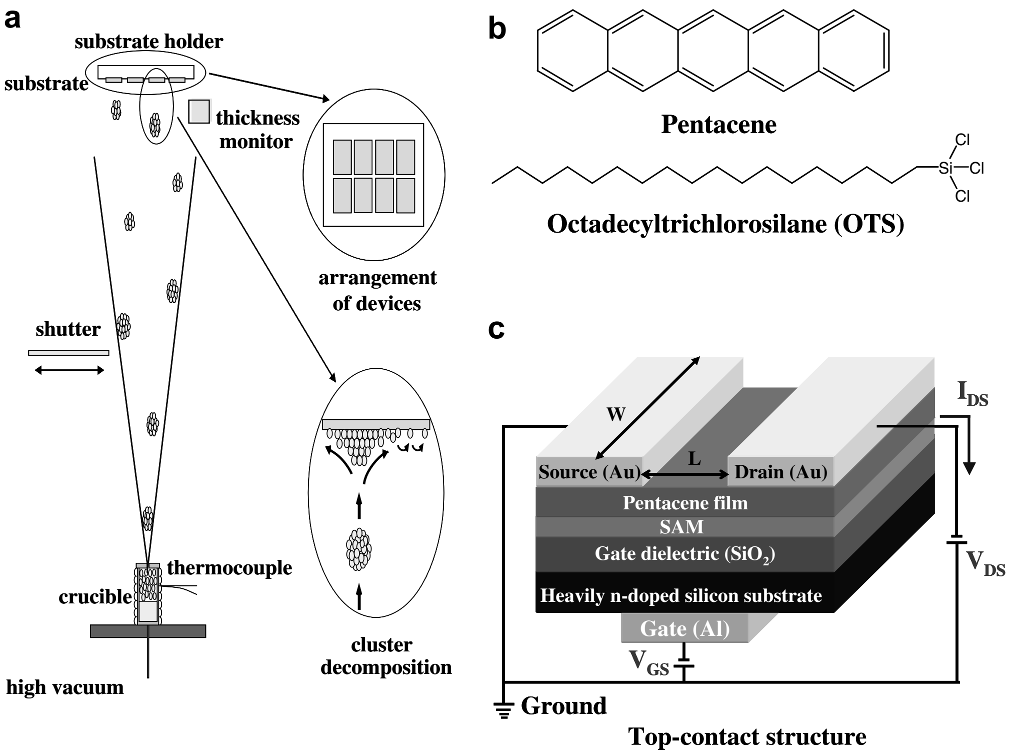

Fig. 1. (a) A schematic diagram of the NCBD apparatus. (b) Molecular structures of the pentacene and octadecyltrichlorosilane (OTS). (c) A schematic cross-sectional view of the top-contact transistor with its bias condition.

immersed in a 1×10^{-4} M solution of OTS (Aldrich Co.) in *n*-hexane [22]. Pentacene (TCI Co.) was deposited using a homemade NCBD apparatus. The system is described in detail elsewhere [14]. The chamber consisting of an evaporation crucible, a drift region, and a substrate was pumped by a 10 in. baffled diffusion pump. The pentacene sample was placed inside the enclosed cylindrical crucible cell with a diameter of 1.0 mm and a 1.0 mm-long nozzle, and sublimated at 460 K by resistive heating. The pentacene vapor then underwent adiabatic supersonic expansion into the drift region at a working pressure of about 3×10^{-6} Torr. The resultant neutral pentacene cluster beams were deposited directly onto the room-temperature SiO_2 layers with an average thickness of ca. 500 Å at a deposition rate 1 Å/s.

The thickness, morphology, crystallinity and contact angle were examined using an alpha step surface profile monitor, atomic force microscopy (AFM), X-ray diffraction (XRD) and a contact angle goniometer, respectively. The current–voltage characteristics and their temperature dependence were measured using an optical probe attached to an HP4140B *p*A meter-dc voltage source unit, and a 10 K-closed cycle refrigerator for more than 100 devices over a wide range of temperatures from 300 K down to 10 K.

3. Results and discussion

3.1. Morphological and structural properties

Fig. 2 shows 2-dimensional AFM micrographs of the OTS-untreated and -pretreated pentacene films at a nominal thickness of 500 Å. Both films were covered completely with grain crystallites with a dendritic structure. The diameter distributions and square roughness ranged from 0.25 to 0.30 μm and ~55 Å for the OTS-untreated films, respectively and 0.16 to 0.26 μm and ~30 Å for the OTS-pretreated films, respectively. The pretreated pentacene films showed a lower roughness and a higher packing density, which indicates that the amphiphilic OTS surfactant creates favorable deposition conditions for the non-polar pentacene cluster beams at the interface. This result is also consistent with the contact angle measurements. The OTS pretreatment increased the surface contact angle with water from 44° to 108°. This remarkable increase indicates that the pretreated surface becomes highly non-polar after the surfactant pretreatment. Therefore, the unfavorable lattice mismatch is significantly reduced through interactions with the OTS molecules, which are capable of simultaneously forming bonds with the hydrophobic pentacene and the hydrophilic SiO_2 at the interface.

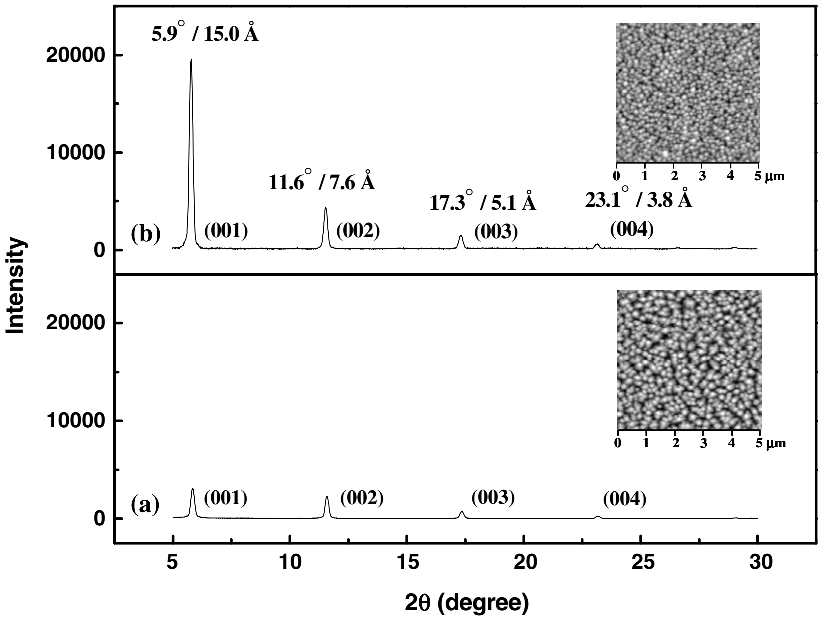

Fig. 2. Comparison of the XRD patterns and 2-D AFM micrographs (5×5 μm^2) of 500 Å-thick pentacene thin films prepared on the (a) untreated and (b) OTS-pretreated SiO_2 substrates at room temperature.

The effect of the surface pretreatment was examined by XRD. The diffraction patterns shown in Fig. 2 were assigned to the triclinic thin-film phase, which corresponds to a kinetically favored, metastable phase. The peaks could be fitted to a series of $(0\,0\,l)$ reflection lines, and the interplanar spacing, d_{00l}, was determined to be 15.0 Å for both films. The more distinctive first- and higher-order multiple peaks with excellent signal-to-noise ratio in Fig. 2b indicate the presence of enhanced crystallinity in the OTS-pretreated films. Furthermore, compared with recent studies carried out by several groups using thermal evaporation [22,23], the superior surface morphology and crystallinity observed in this study demonstrate the unique capacity of the NCBD scheme to produce uniform, smooth films consisting of submicrometer-sized crystallites on room-temperature substrates without any thermal annealing processes.

3.2. Device performance

A comparative characterization of the performance of NCBD-based devices was carried out. The pentacene active layers exhibited a p-type behavior: the majority carriers were holes. The transistors were examined in accumulation mode. Fig. 3a demonstrates the typical plot of the drain-source current (I_{DS}) as a function of the drain-source voltage (V_{DS}) at various gate voltages (V_{GS}). The overall characteristics are well described by the standard field-effect transistor equations. The inset in Fig. 3a shows the I_{DS} at low V_{DS}, and the observed linear behavior indicates good ohmic contact between the gold electrodes and pentacene active layers [24]. From the $I_{DS}^{1/2}$ vs. V_{GS} and $\log(I_{DS})$ vs. V_{GS} plots, several device parameters such as the μ_{eff}, current on/off ratio (I_{on}/I_{off}), threshold voltage (V_T) and subthreshold slope $SS = V_{GS}/\log(I_{DS})$ can be derived. Here, μ_{eff} can be calculated in the saturation regime from the following equation:

$$\mu_{eff} = \frac{2L(I_{DS})}{WC_i(V_{GS} - V_T)^2} \text{ (saturation regime)},$$

where C_i is the capacitance per unit area of the SiO_2 gate dielectric insulator (for a thermally grown 2000-Å-thick SiO_2, $C_i = 17.25$ nF/cm^2) and the transistor dimensions have a channel width (W) of 500 μm and a length (L) of 660–1400 μm.

Table 1 lists the various parameters derived. In particular, the observed mobilities were among the best reported thus far: 0.47 and 1.25 cm^2/Vs for the OTS-untreated and -pretreated devices, respectively. In contrast, Pernstich et al. and Zhang et al. recently reported an effect of organosilane surfactants on the device performance and obtained room-temperature carrier mobilities of 0.4 and 0.6 cm^2/Vs for the OTS-pretreated devices prepared on the SiO_2 substrates, respectively, [12,13].

One of the critical factors determining the performance is the quality of the as-deposited thin films. The formation of active layers with higher structural organization will definitely result in more efficient charge-carrier transport through a face-to-face intermolecular interaction between the π–π stacks. The excellent mobilities observed were attributed mainly to the formation of such high-quality, NCBD-based thin films. Here, it should be noted that although the NCBD scheme was applied to room-temperature substrates, the cluster beams resulted in the growth of closely packed, nanometer-sized grain crystallites without any thermal post-treatment. Especially, after the OTS pretreatment, the amphiphilic surfactant enhanced the degree of molecular ordering and the resulting π–π overlap, leading to a significant increase in hydrophobicity, packing density and crystallinity of the films, as demonstrated by the contact angle, AFM and XRD results. Such favorable improvement was reflected in the outstanding device characteristics. Another desirable feature of the OTS pretreatment is the reduction of the subthreshold slope. The SS value is generally governed by the material properties, and the lower SS value observed indicates that the pretreatment improves the quality of the NCBD-based pentacene active layers.

3.3. Transport characteristics

The temperature dependence of the field-effect mobility (μ_{eff}) and the total trap density also support the aforementioned device features. Fig. 3b represents the typical plot of the mobility over a wide range of temperatures from 300 K down to 10 K for the NCBD-based transistors. μ_{eff} tends to be temperature-independent as the temperature is increased in region I ($10\text{ K} < T < 40\text{ K}$), whereas μ_{eff} increases exponentially in region II ($40\text{ K} < T < 300\text{ K}$). Region I can be described by a so-called tunneling mechanism occurring at the Au–pentacene interfaces. On the other hand, region II corresponds to an activated transport mechanism, where the conduction of hole carriers is governed by the

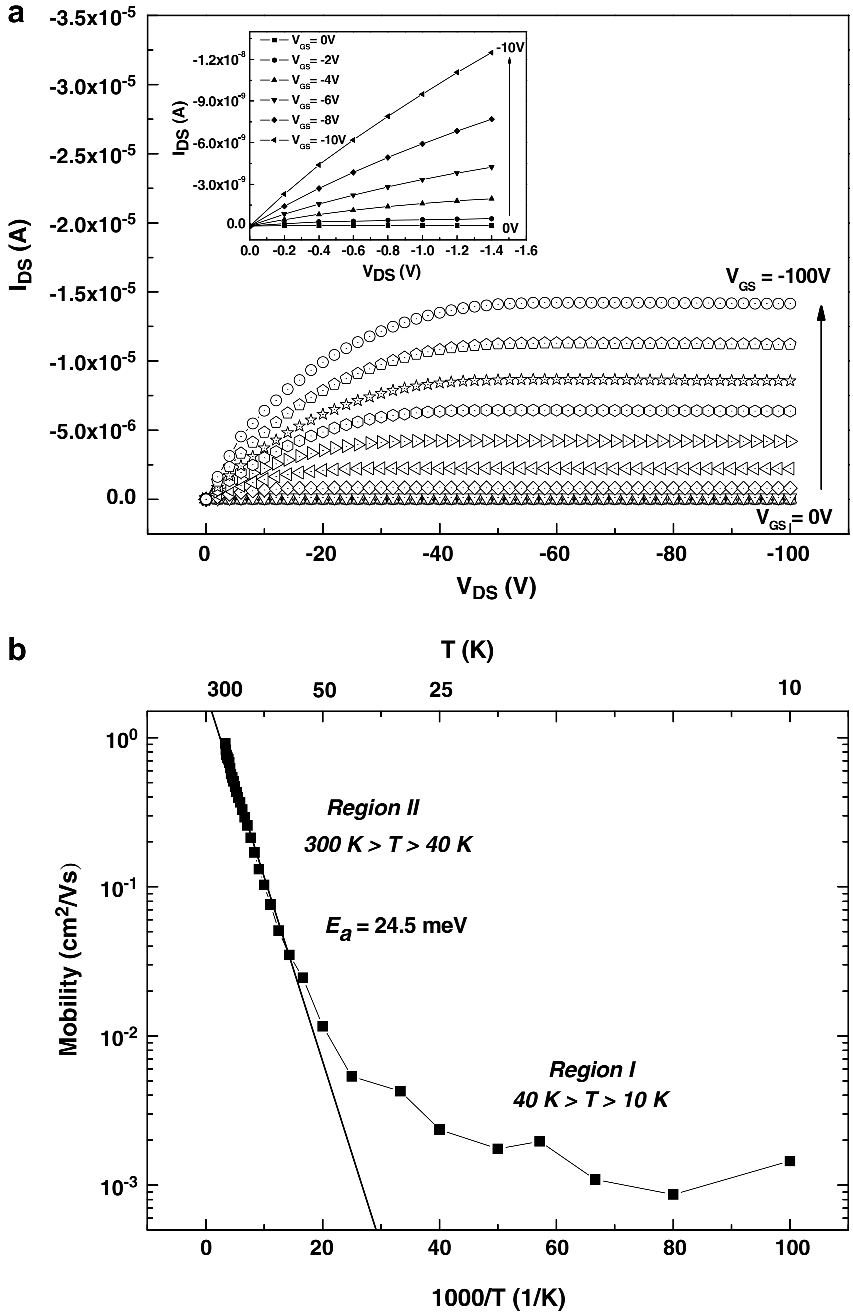

Fig. 3. (a) Current–voltage characteristics at various gate voltages for the OTS-pretreated pentacene-based transistors prepared using the NCBD method. The inset shows the I_{DS} in the low V_{DS} region. (b) An Arrhenius plot of the saturation mobility of the OTS-pretreated transistors in the temperature range of 10–300 K.

overcoming of shallow traps present in the pentacene active layer.

As shown by the solid line, region II is well fitted by the Arrhenius relation $\mu_{eff} \propto \exp(-E_a/kT)$, where E_a and k are the activation energy and Boltzmann constant, respectively. From the slope of the logarithmic plot, E_a was estimated to be 45.7 and 24.5 meV for the OTS-untreated and -pretreated devices, respectively (Table 1). The activation energies in this study were relatively lower than those

Table 1
Summary of the NCBD-based transistor characteristics for root-mean-square roughness (R_{rms}), field-effect mobility (μ_{eff}), threshold voltage (V_T), subthreshold slope SS = V_{GS} /log(I_{DS}), current on/off ratio (I_{on}/I_{off}), activation energy (E_a) and trap density (N_{trap})

	R_{rms} (Å)	μ_{eff} (cm^2/Vs)	V_T (V)	SS (V/dec)	I_{on}/I_{off}	E_a (meV)	N_{trap} (10^{12}/cm^2)
OTS-untreated	55	0.47	−19.6	5.7	10^4	45.7	1.7
OTS-pretreated	30	1.25	−35.5	3.4	10^5	24.5	0.8

The transistor dimensions have a channel width (W) of 500 μm and a length (L) of 1400 μm.

reported elsewhere, particularly in the OTS-pretreated system. Minari et al. reported an E_a of 54.8 meV in OTS-pretreated pentacene devices prepared by thermal evaporation [24]. The low E_a is also consistent with the estimated total trap densities N_{trap} of 1.7×10^{12} and 0.8×10^{12}/cm^2 for the OTS-untreated and -pretreated devices, respectively. Here, N_{trap} is expressed by the following relationship:

$$N_{trap} = \frac{C_i|V_T - V_{TO}|}{e},$$

where V_{TO} is the turn-on voltage and e is the elementary charge [12]. Those low densities are in sharp contrast with the higher density of 5.2×10^{12}/cm^2 reported by Zhang et al. in the OTS-pretreated devices [13]. The origin of the E_a lies mainly in the traps produced by the structural disorders and/or defects in the thin films [25]. It was clearly demonstrated that the lower E_a and trap density observed were strongly correlated with the improved quality of the as-deposited NCBD-based films, ultimately leading to the efficient carrier transport in the well-connected intergrains and the excellent mobilites in the pentacene-based transistors.

4. Conclusions

Pentacene-based, top-contact transistors were fabricated on two kinds of substrates, both at room temperature, using the NCBD method; OTS-untreated and -pretreated SiO_2. Both active layers without a thermal post-treatment consisted of high-quality, crystalline pentacene thin films with uniform, smooth surfaces. In particular, the total trap density and temperature dependence of μ_{eff} in the range of 10−300 K showed that the amphiphilic OTS pretreatment decreased the trap density and activation energy for carrier transport significantly by reducing the amount of structural disorder. The derived field-effect mobilities were among the best reported thus far: $\mu_{eff} = 0.47$ and 1.25 cm^2/Vs for the OTS-untreated and -pretreated devices, respectively. The fabrication of several organic-based transistor devices using various types of π-conjugated molecules and surfactants through the NCBD method is currently underway. These studies are expected to provide further insight into the interactions at the interfaces at the molecular level as well as the structure-performance relationship.

Acknowledgments

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[15] P.S. Abthagir, Y.-G. Ha, E.-A. You, S.-H. Jeong, H.-S. Seo, J.-H. Choi, J. Phys. Chem. B. 109 (2005) 23918, In comparison to the procedure described in the Ref. [15], there were three modifications in the present experiment. Firstly, we changed the procedure for cleaning the SiO_2

substrates as described in the text. Previously the substrates were simply cleaned by successive ultrasonic treatments in acetone, methanol and deionized water in order. Secondly, the thickness of thermally grown gate dielectric was changed from 1000 to 2000 Å. Thirdly, the channel length and width of the devices were changed from 1000 and 200 μm to 500 and 1400 μm, respectively. It was believed that all of those combined modifications increased the present device performance significantly.

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