Lecture 12
Continuous-Time ΔΣ ADCs

Trevor Caldwell
trevor.caldwell@awaveip.com

Lecture Plan

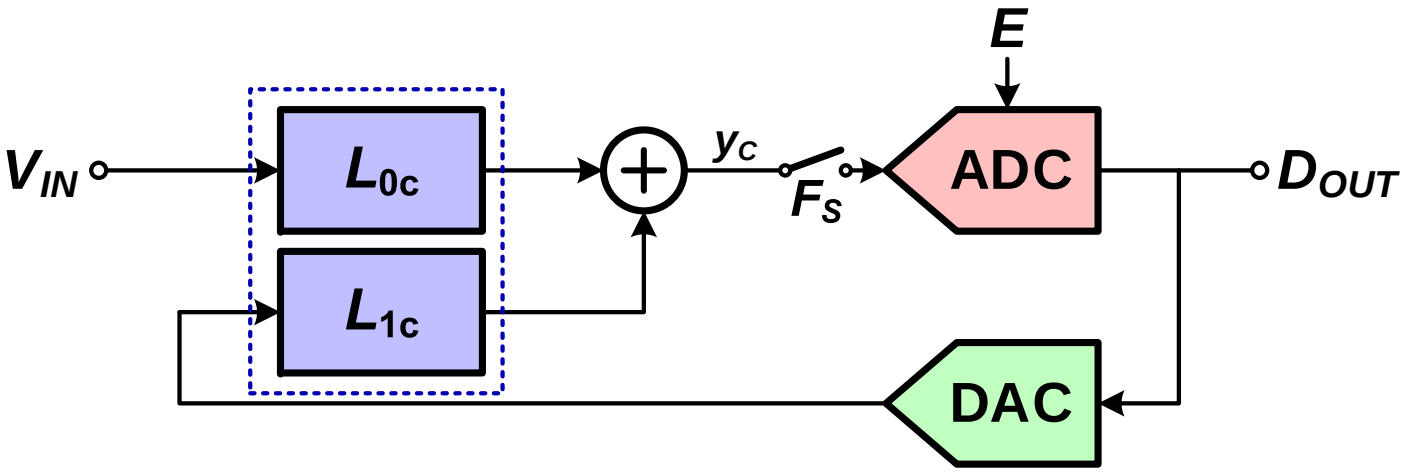
Date	Lecture (Wednesday 2-4pm)		Reference	Homework
2020-01-07	1	MOD1 & MOD2	PST 2, 3, A	1: Matlab MOD1&2
2020-01-14	2	MOD*N* + ΔΣ Toolbox	PST 4, B	2: ΔΣ Toolbox
2020-01-21	3	SC Circuits	R 12, CCJM 14	
2020-01-28	4	Comparator & Flash ADC	CCJM 10	3: Comparator
2020-02-04	5	Example Design 1	PST 7, CCJM 14	
2020-02-11	6	Example Design 2	CCJM 18	4: SC MOD2
2020-02-18	Reading Week / ISSCC			
2020-02-25	7	Amplifier Design 1		Project
2020-03-03	8	Amplifier Design 2		
2020-03-10	9	Noise in SC Circuits		
2020-03-17	10	Nyquist-Rate ADCs	CCJM 15, 17	
2020-03-24	11	Mismatch & MM-Shaping	PST 6	
2020-03-31	12	Continuous-Time ΔΣ	PST 8	
2020-04-07	Exam			
2020-04-21	Project Presentation (Project Report Due at start of class)			

What you will learn…

- **What is a Continuous-Time ΔΣ modulator**
- **Continuous-time circuits for ΔΣ ADCs**
  - **Loop filter, amplifiers, DACs, Direct Feedback**
- **Benefits of Continuous-Time circuits**
  - **… And a couple disadvantages**

What is a Continuous-Time ΔΣ?

- **General continuous-time ΔΣ ADC**



Filters L_{0c}, L_{1c} are continuous-time

Output is identical to discrete-time ΔΣ ADC as long as

$$y[n] = y_c(t)|_{t=nT_S}$$

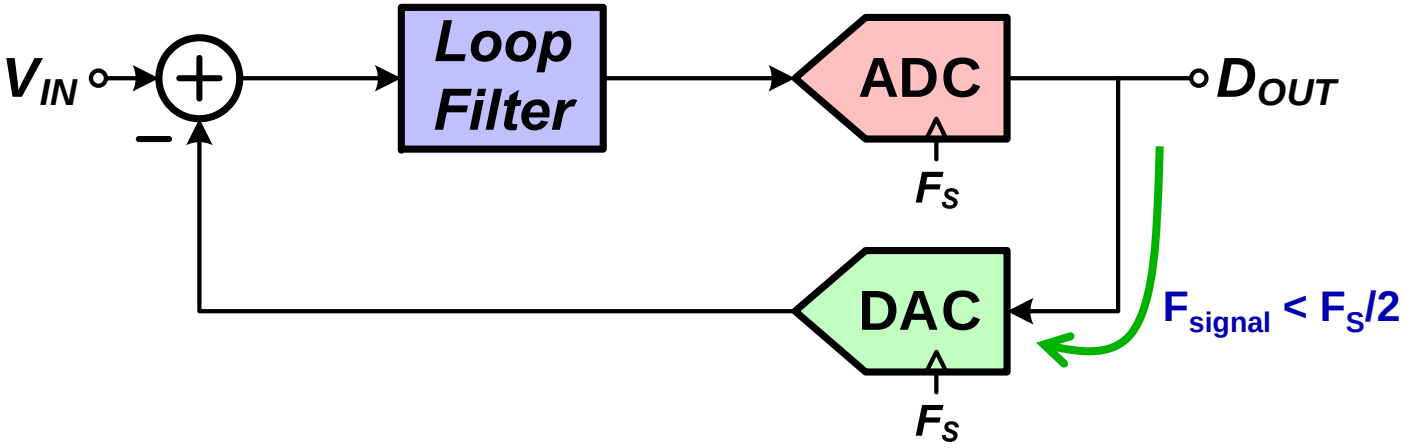
Satisfied if impulse responses are equal at nT_S

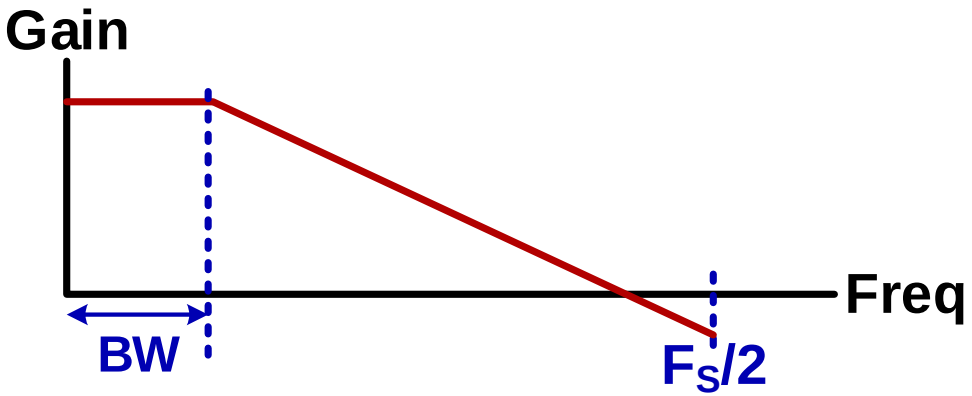
$$\mathcal{Z}^{-1}\{L_1(z)\} = \mathcal{L}^{-1}\{L_{1c}(s)\}|_{t=nT_S}$$

L_{1c}(s) includes DAC(s) and ADC(s)

What is a Continuous-Time ΔΣ?

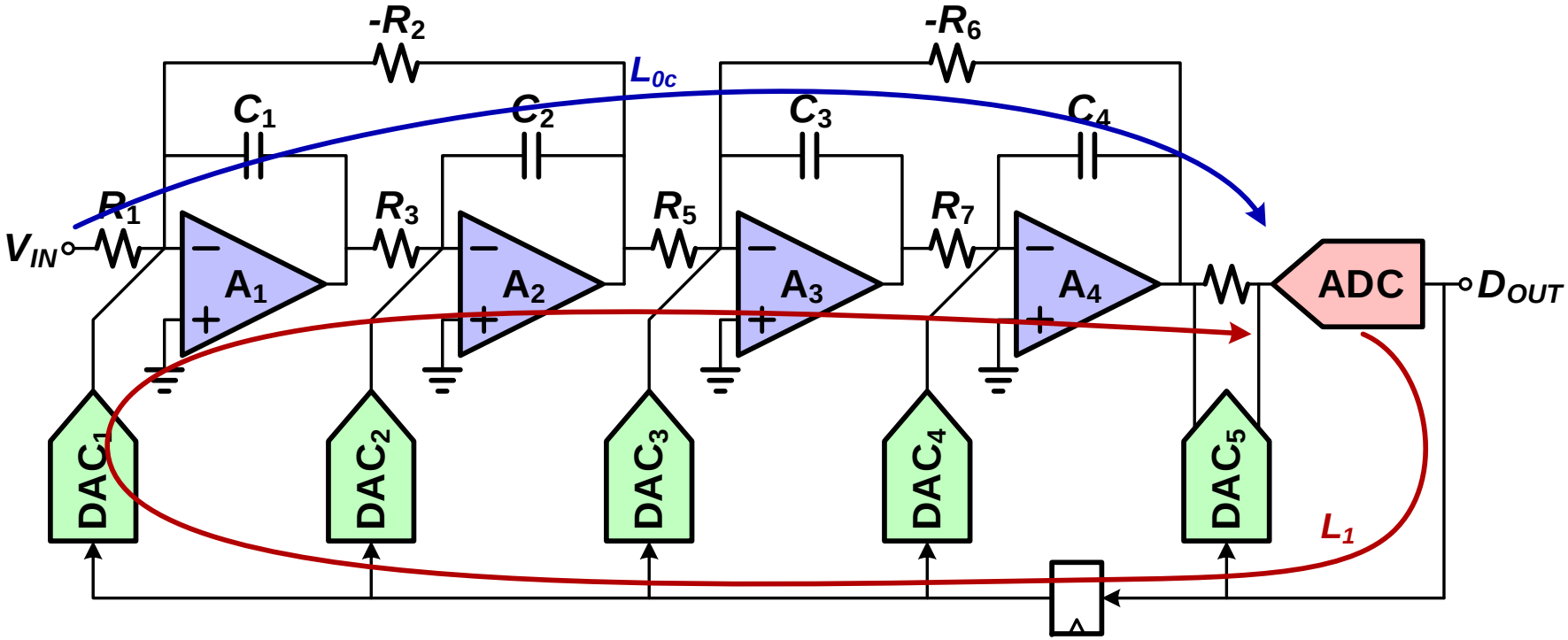
- **Design L_{1c} (Loop Filter) like any negative feedback system**





What is a Continuous-Time ΔΣ?

- **Example: 4th-order Continuous-Time FB ΔΣ ADC**



$$L_1\left(e^{j2\pi f}\right) = \sum_{n=-\infty}^{\infty} L_{1c}\left(j2\pi(f + nf_s)\right)$$

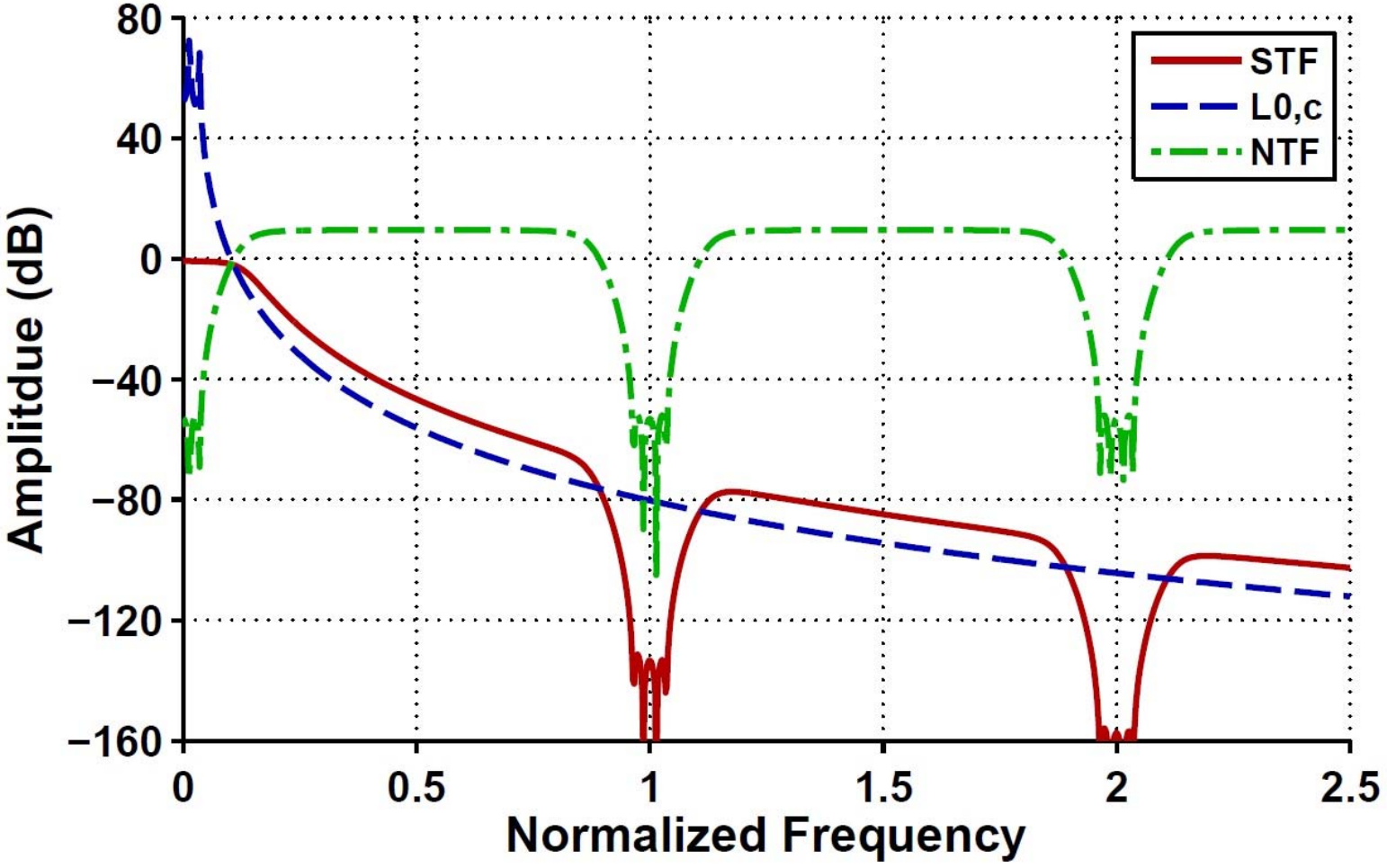
Includes DAC(s) and ADC(s)

$$NTF(z) = \frac{1}{1 - L_1(z)}$$

$$STF(s) = L_{0c}(s) \cdot NTF(e^s)$$

What is a Continuous-Time ΔΣ?

- **Example: 4th-order Continuous-Time FB ΔΣ ADC**

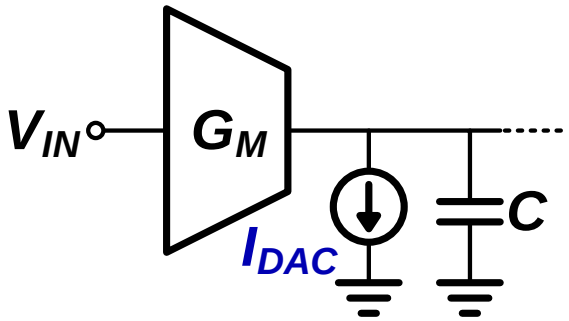


Circuit differences for CT ΔΣ ADC

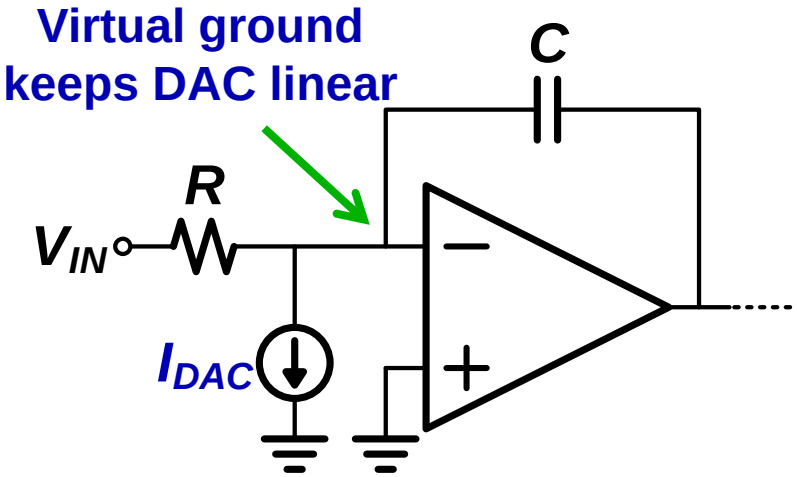
- **Loop Filter**
  - **Resistor (or G_M) and capacitor passives instead of only capacitors**
  - **No switches (no aliasing at loop filter front-end)**
  - **Amplifiers can be designed more efficiently: feed-forward amplifiers**
- **DACs**
  - **Typically current-mode instead of switched-capacitor**
  - **Choice of Return-to-Zero or Non-Return-to-Zero pulses**
- **Direct Feedback DAC**
  - **Additional DAC path to compensate for excess loop delay in CT loop filter**

Loop Filters in CT ΔΣ ADCs

- **Gm-C Integrator**
  - ☺ Higher speed
  - ☹ G_M variation causes G_M/C coefficient variation
  - ☹ Reduced linearity



- **RC Integrator**
  - ☺ R and C variation can be easily tuned
  - ☺ Feedback improves linearity of amplifier, DAC
  - ☹ Lower speed

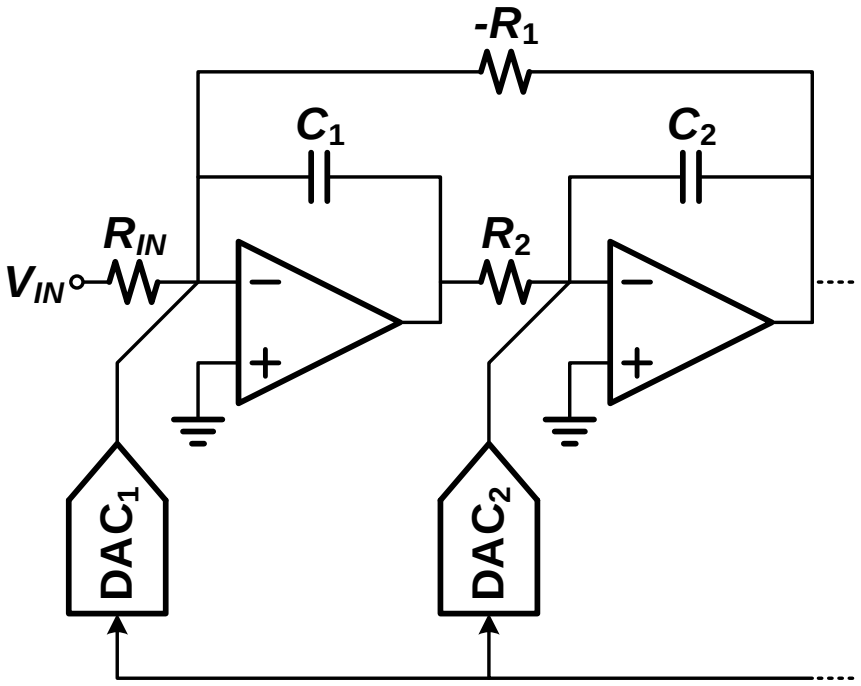


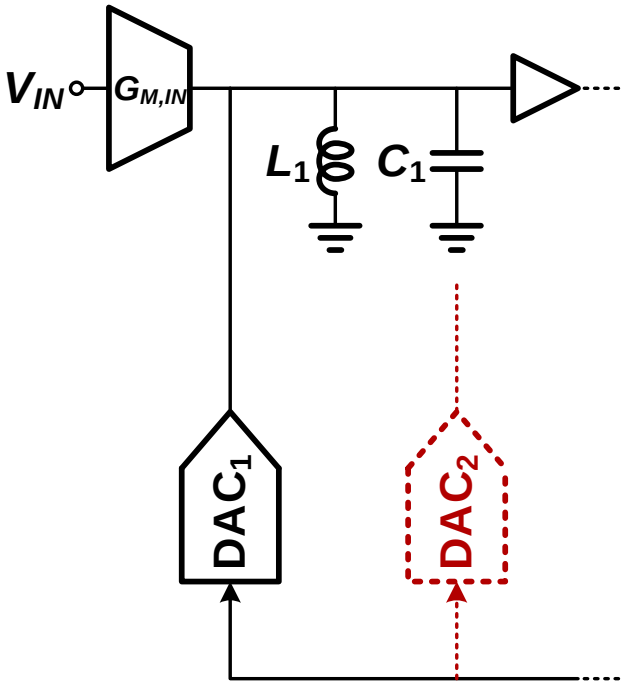
Loop Filters in CT ΔΣ ADCs

- **Resonators**

  RC integrators: easily programmable

  LC tank: lower noise, higher Q, fewer degrees of freedom, no virtual ground node



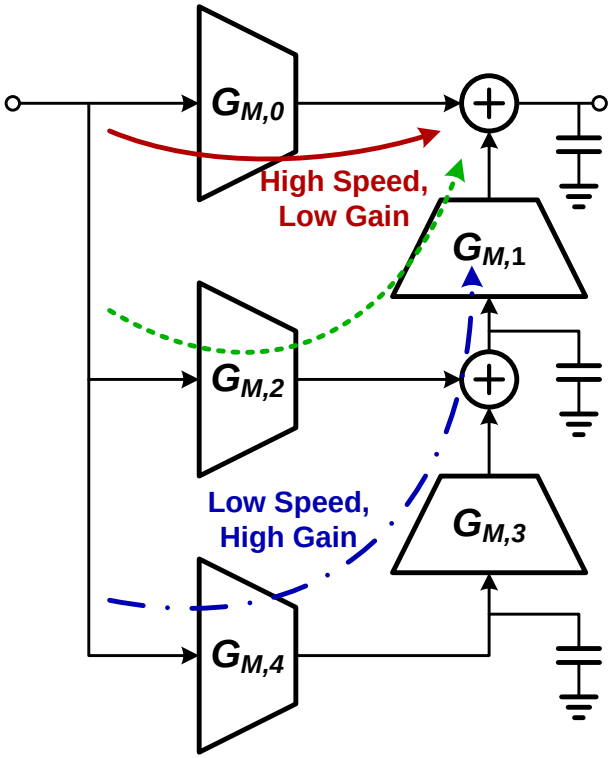


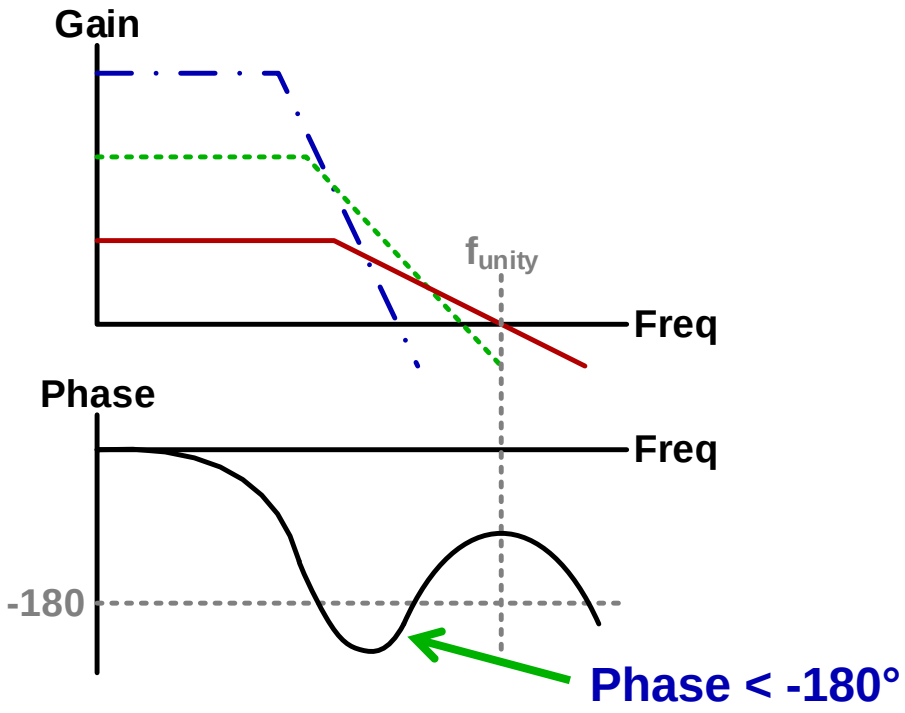
Loop Filters in CT ΔΣ ADCs

- **DT amplifier design (from Amp Design lecture)**
  - **Amplifier designed with 1st-order settling response, main concern is settling behavior (eg, no pole-zero doublets)**
  - **If amplifier settles to sufficient accuracy in ~T/2 seconds, NTF will be as expected**
- **CT amplifier design**
  - **Amplifier can be conditionally stable, 1st-order settling not required**
  - **Amplifier gain within signal band must be sufficiently high for NTF noise suppression in-band**
  - **Can use *feed-forward amplifiers***

Feed-forward Amplifiers

- **Efficient for continuous-time circuits**
  - **Lower unity-gain required for a given bandwidth**
  - **Conditionally stable: phase < -180° at f < f_{unity}**
    phase > -180° at f_{unity}

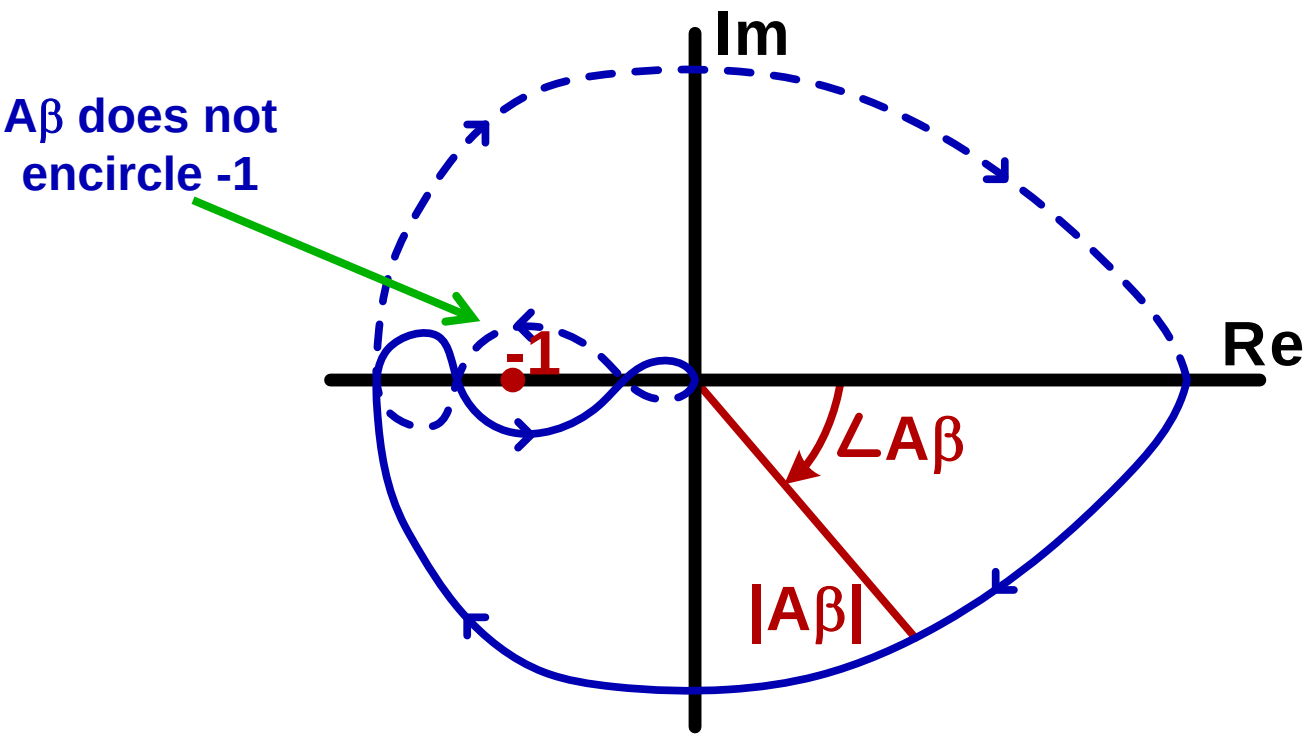




Feed-forward Amplifiers

- **Nyquist stability criterion**

  If the loopgain transfer function Aβ has no RHP poles, then it is closed-loop stable iff the Nyquist diagram has no encirclements of the -1 point



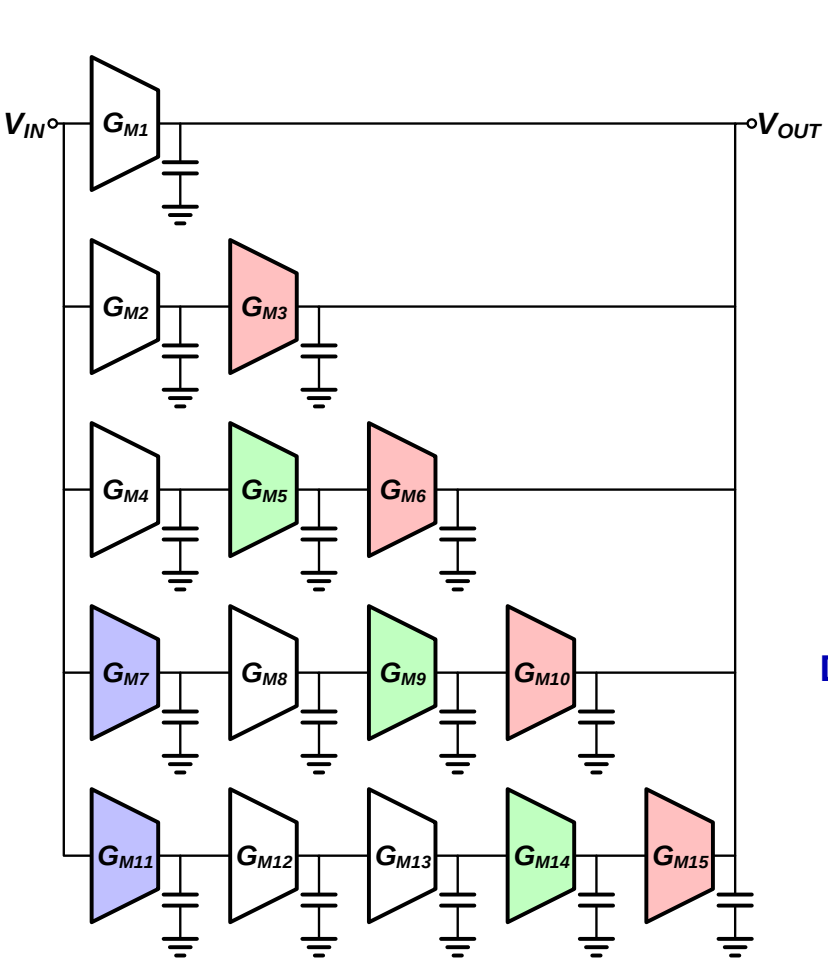
Feed-forward Amplifiers

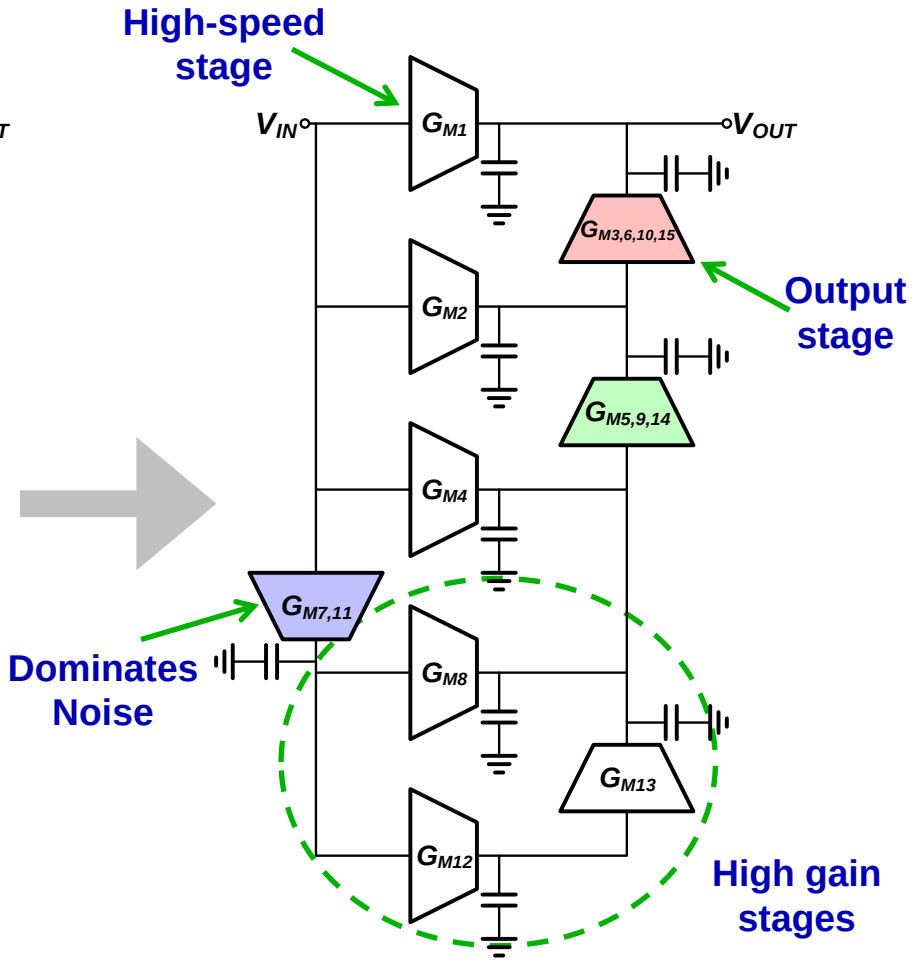
- **Efficient for continuous-time circuits**
  - **Cascaded gains rather than cascoded gains**
  - **Appropriate for new technologies with smaller $g_m r_{out}$**
  - **High-speed (low OSR) CT modulators almost exclusively use them**

- **Not appropriate for discrete-time circuits**
  - **Slow pole-zero settling**
  - **High-frequency noise aliases back in band**

Feed-forward Amplifiers

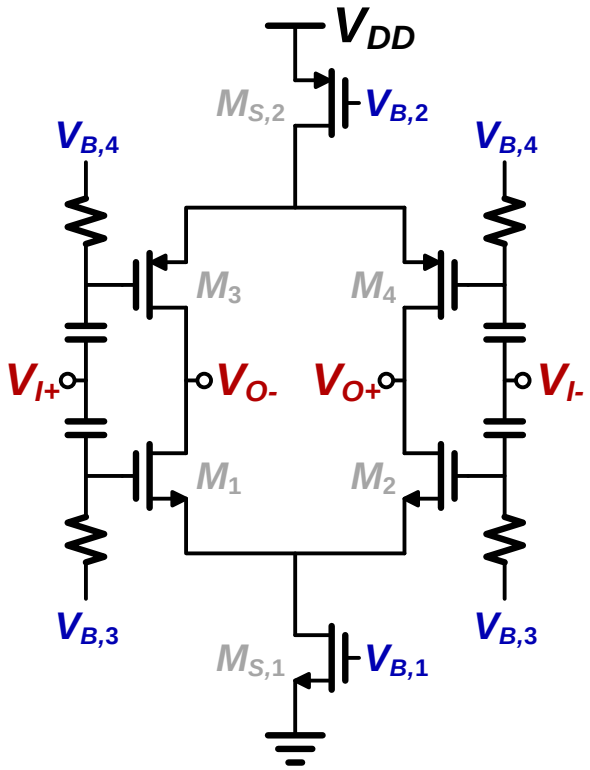
- **Fewest G_M stages: 2N-1 for N^{th}-order amplifier**

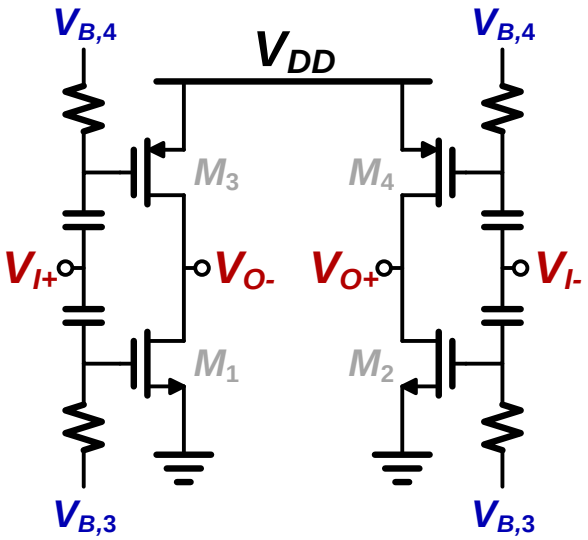




Feed-forward Amplifiers

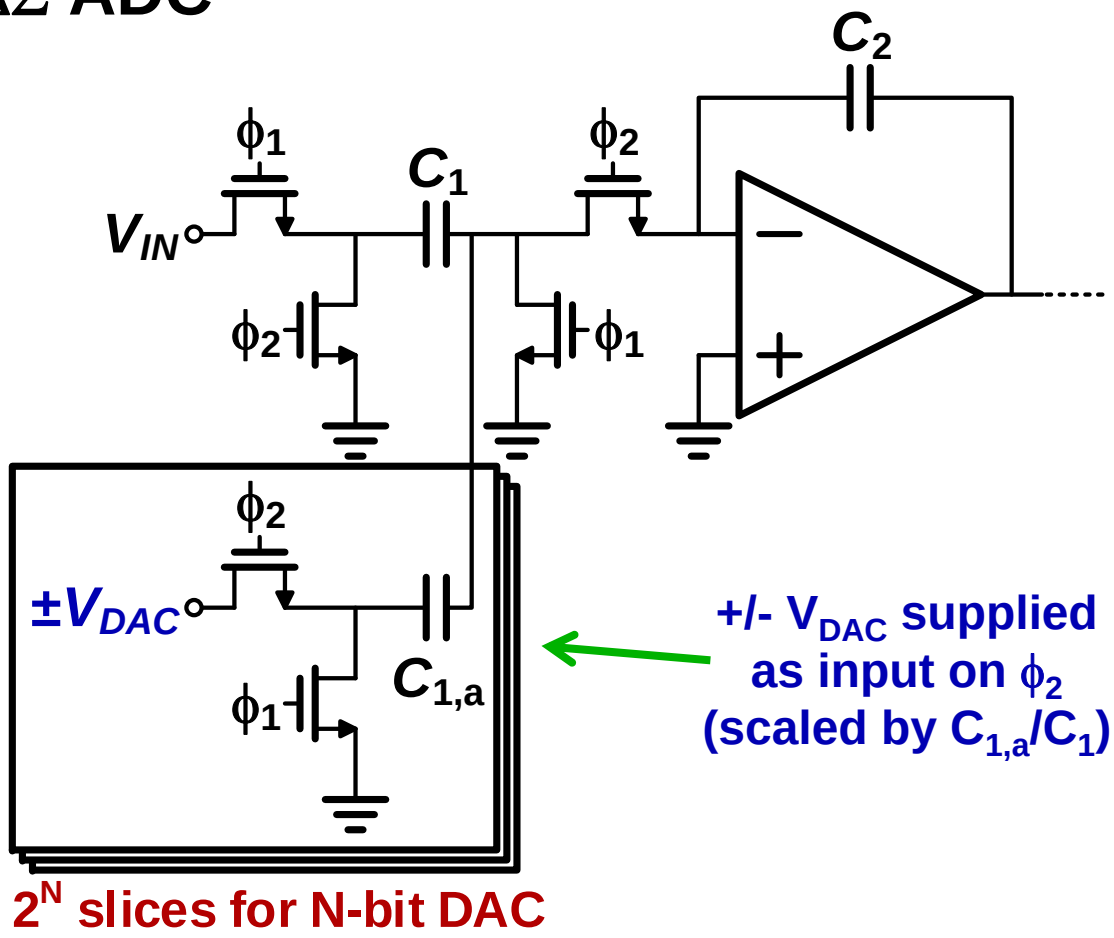
- **Individual G_M stages**
  - **First-order complementary stages for high G_M efficiency**
  - **Combination of differential + pseudo-differential pairs**
  - **Capacitive coupling used when necessary**





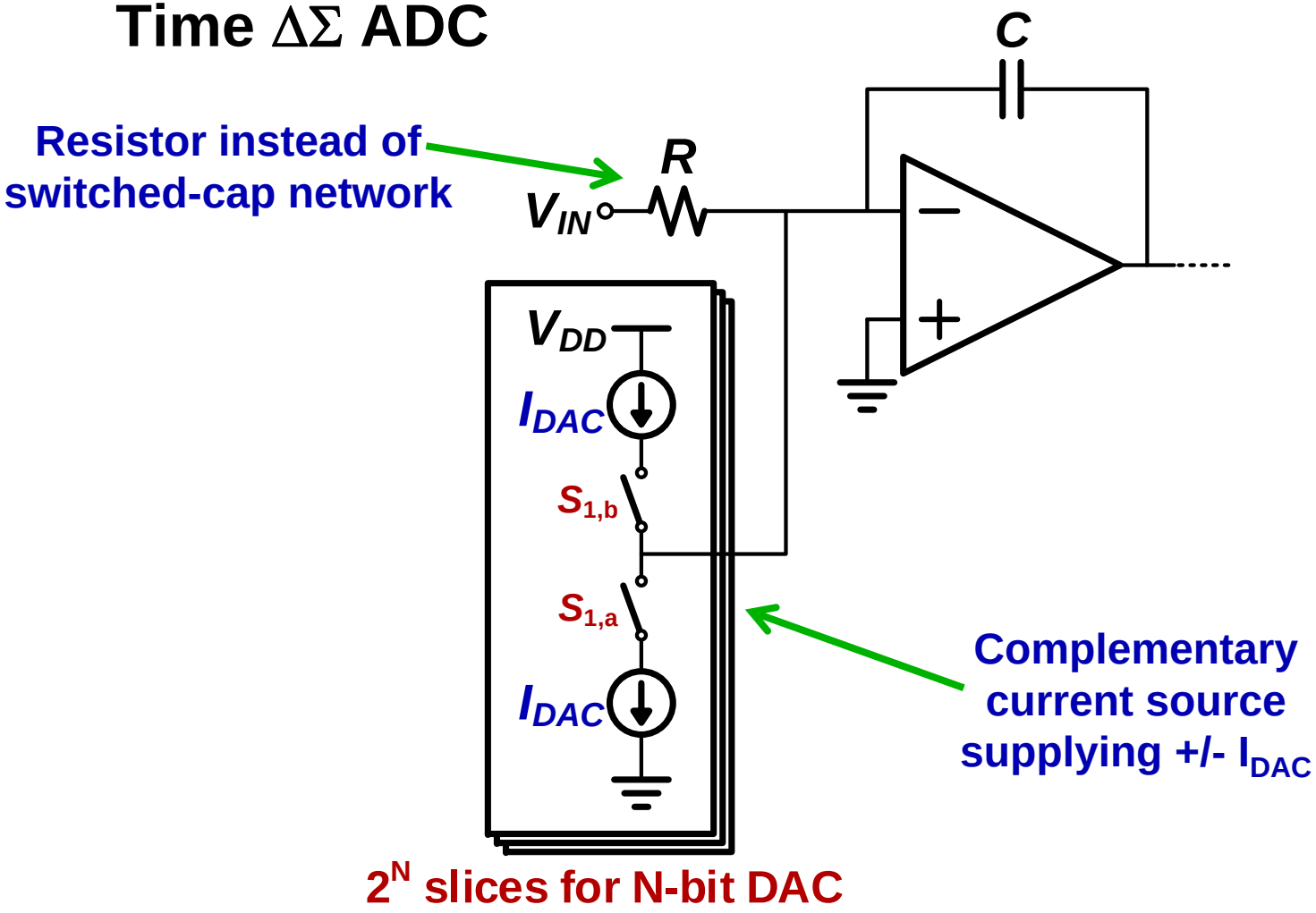
DACs in DT ΔΣ ADCs

- **Typical switched-capacitor DAC for a Discrete-Time ΔΣ ADC**



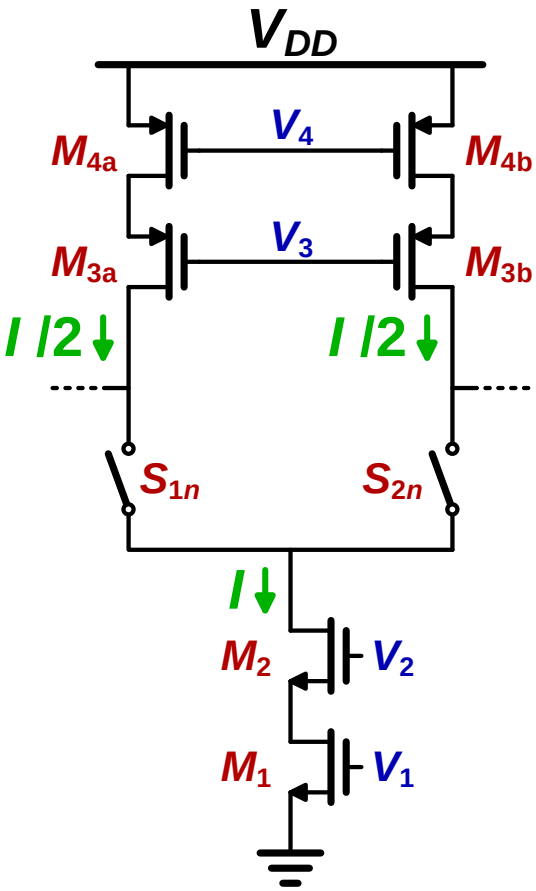
DACs in CT ΔΣ ADCs

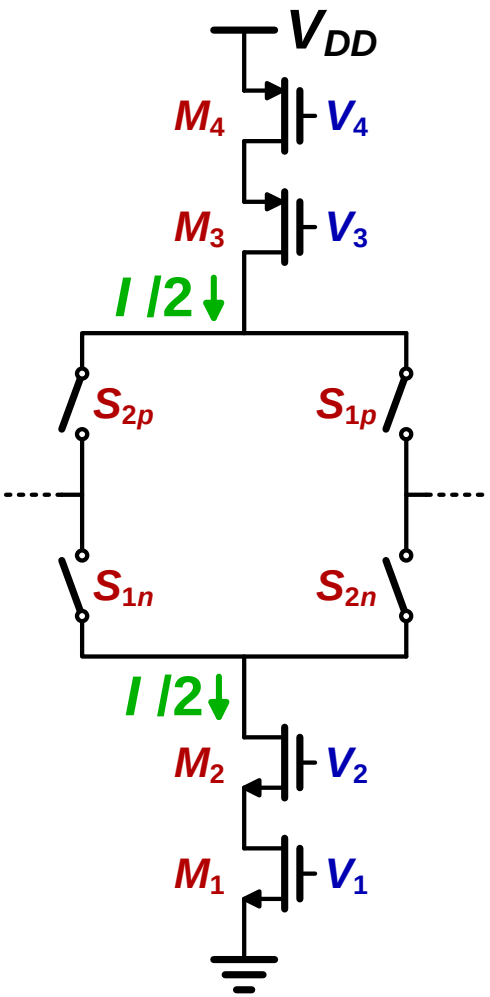
- **Typical current-mode DAC for a Continuous-Time ΔΣ ADC**



DACs in CT ΔΣ ADCs

- **NMOS (or PMOS) vs Complementary DAC**





DACs in CT ΔΣ ADCs

- **Benefits of complementary DAC**
  - All current used as signal current
  - Smaller g_m, smaller (3dB) noise current

$$\overline{I_n^2} = 4kT\gamma g_m$$

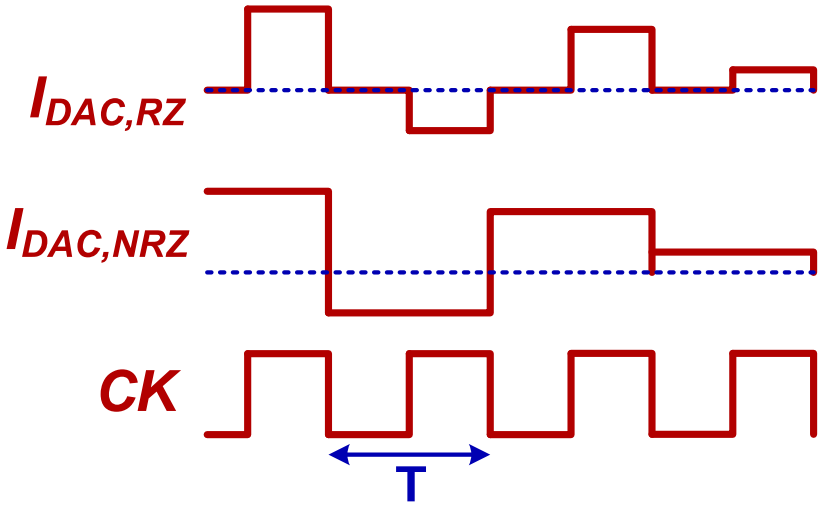
- **Benefits of NMOS (or PMOS) DAC**
  - Only NMOS (or PMOS) current sources are sized for matching, lower total area

$$\left.\frac{\sigma_I}{I}\right|_{VT} = \sigma_{VT}\frac{2}{V_{GS}-V_T} = \frac{A_{VT}}{\sqrt{WL}}\frac{2}{(V_{GS}-V_T)}$$

  - Fewer transistor in stack, more headroom for V_{EFF} in current sources (slightly lower noise)

DACs in CT ΔΣ ADCs

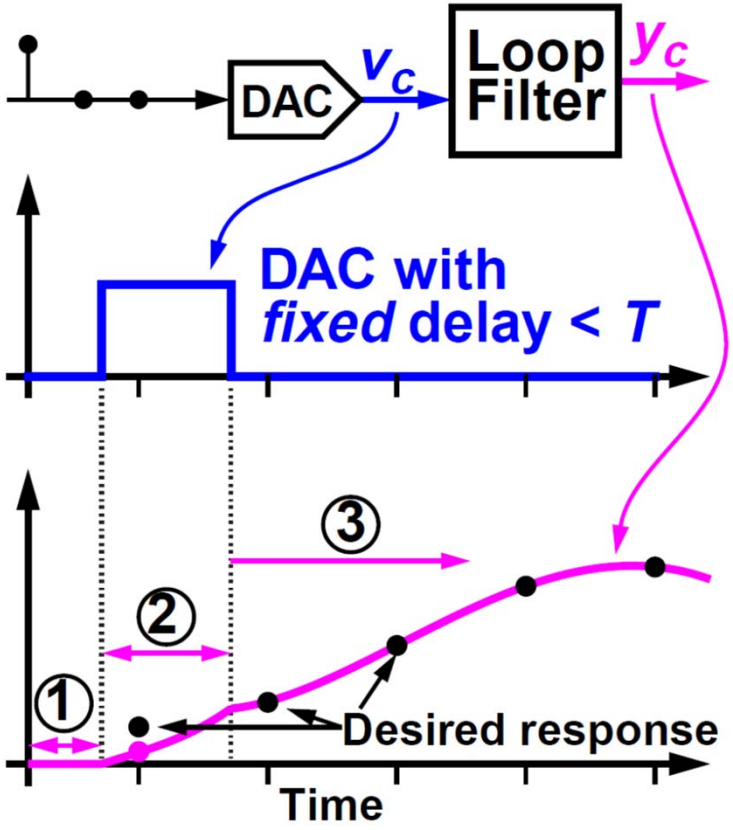
- **Return-to-Zero vs Non-Return-to-Zero**
  - **RZ: DAC pulse only lasts a fraction of the period T**
    Improved linearity, reduced jitter tolerance
  - **NRZ: DAC pulse lasts entire period T**
    Nonlinear due to mismatch in rise/fall time (even order), improved jitter tolerance



Flash/DAC Path in CT ΔΣ ADCs

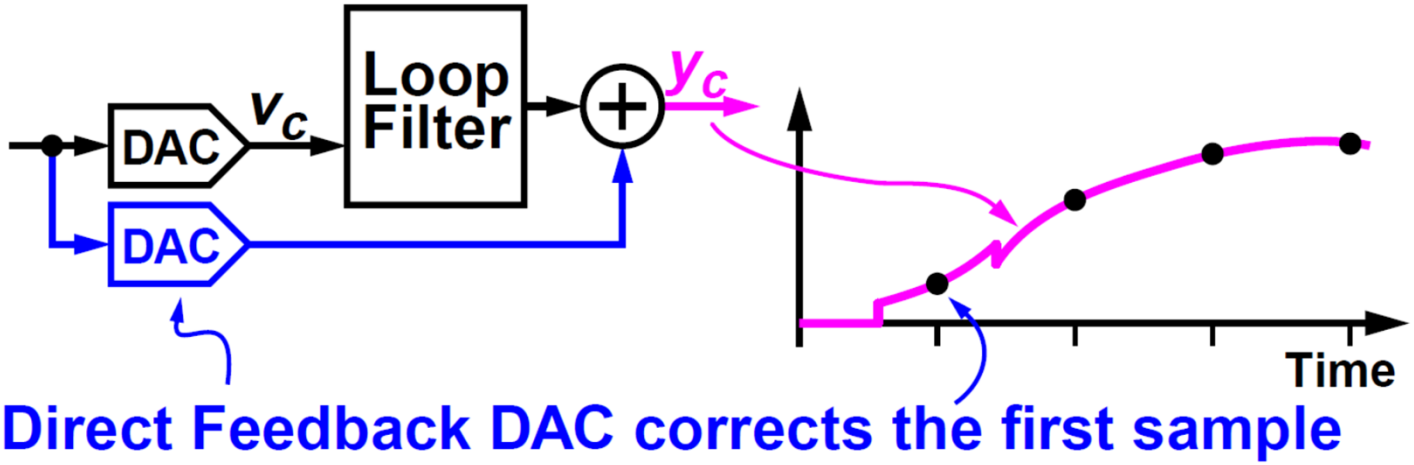
- **Effect of Quantizer/DAC Delay**
  1) **Loop outputs zero until DAC pulse begins**
  2) **Loop responds as if input were a step**
  3) **Loop follows trajectory of an n^{th}-order linear system with zero input but non-zero initial conditions**

→ Coefficients are adjusted so samples of pulse response match the desired impulse response except at the first point; The NTF will be wrong.



Flash/DAC Path in CT ΔΣ ADCs

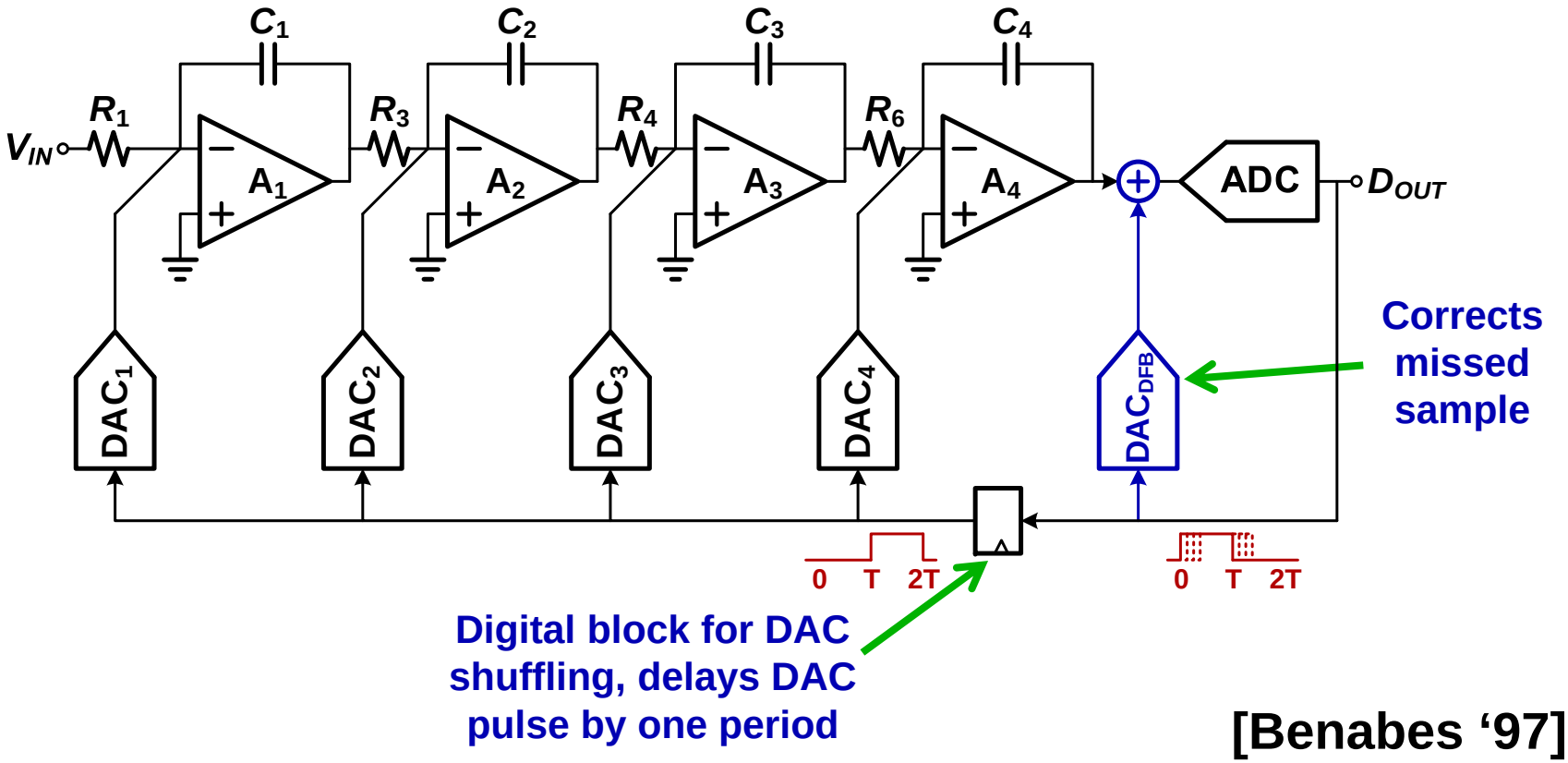
- **To compensate for the Feedback Delay and fix the first sample, add a direct feedback DAC**



- **With enough DACs, one for each errant sample, any finite number of points can be repaired**
  - **In principle, the delay of the main feedback path can be anything, but the system becomes sensitive to coefficient errors**

Flash/DAC Path in CT ΔΣ ADCs

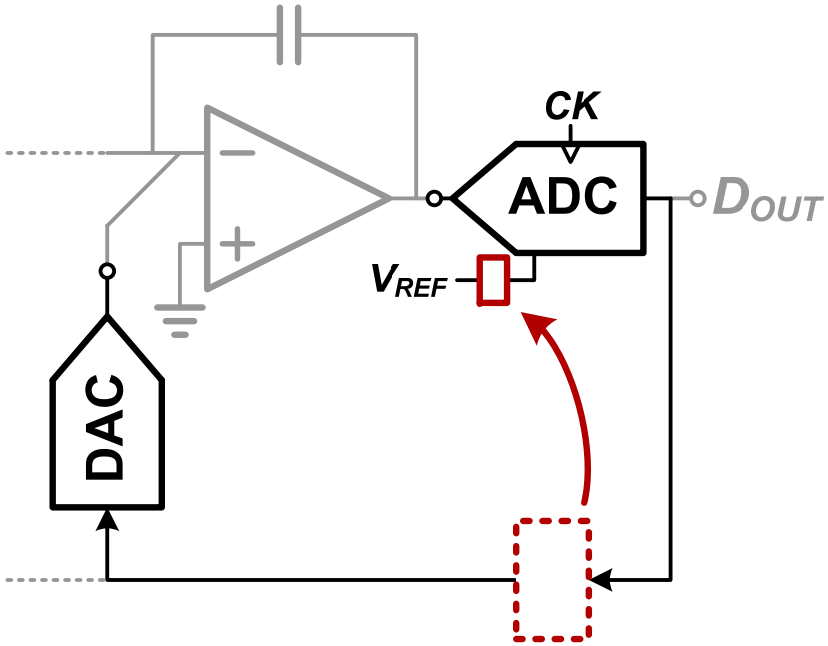
- **Direct Feedback Path**
  - **Full period for Flash/DAC path to resolve its output**
  - **Allows time for shuffling algorithms**



[Benabes '97]

Flash/DAC Path in CT ΔΣ ADCs

- **Flash/DAC path can limit speed of a CT ΔΣ ADC**
  - **Use flash reference shuffling**
  - **Removes shuffling delay from critical flash/DAC path and adds it to the flash ADC block**



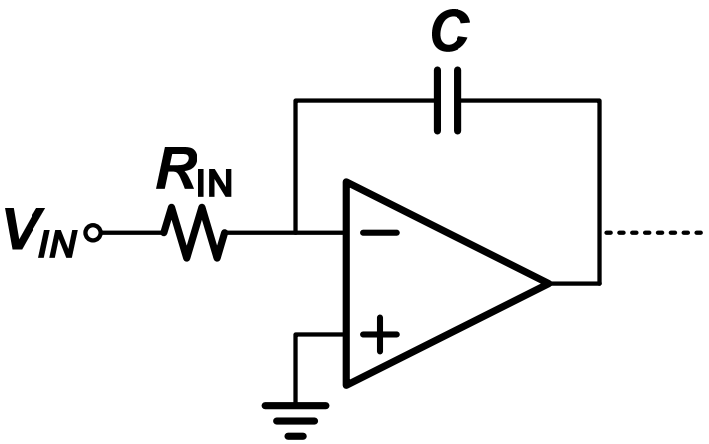
CT vs DT ΔΣ Modulators

- **Advantages of continuous-time circuits**
  - Ease of Integration
  - Anti-aliasing
  - Noise filtering
  - Amplifier current requirements (lower power)
  - Improved metastability
  - Bandpass ΔΣ ADC

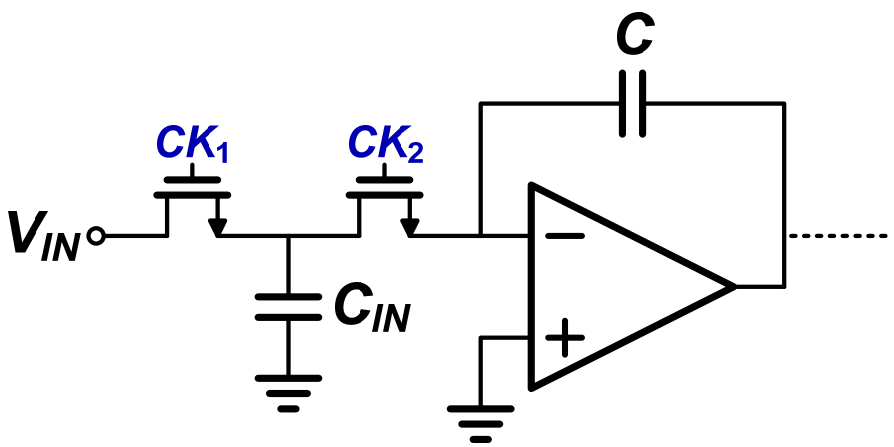
- **Disadvantages of continuous-time circuits**
  - Accurate TF regardless of F_{CK}
  - RC tuning
  - Jitter

Advantages of CT ΔΣ Modulators

- **Integration with other circuits**
  - **Easily interface with other CT circuitry**
  - **No power-hungry high-resolution input buffer required**



Continuous-Time

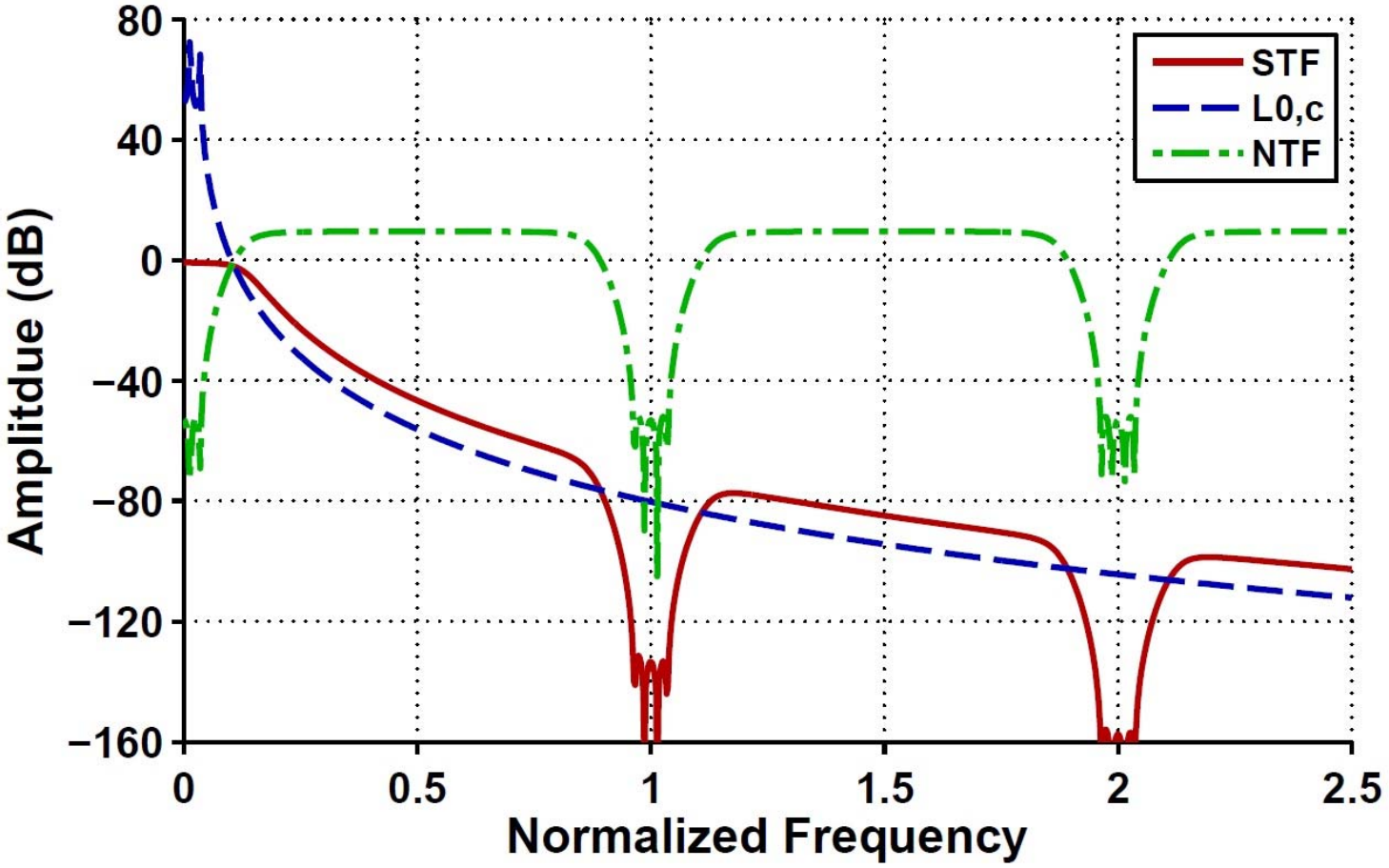


Discrete-Time

Advantages of CT ΔΣ Modulators

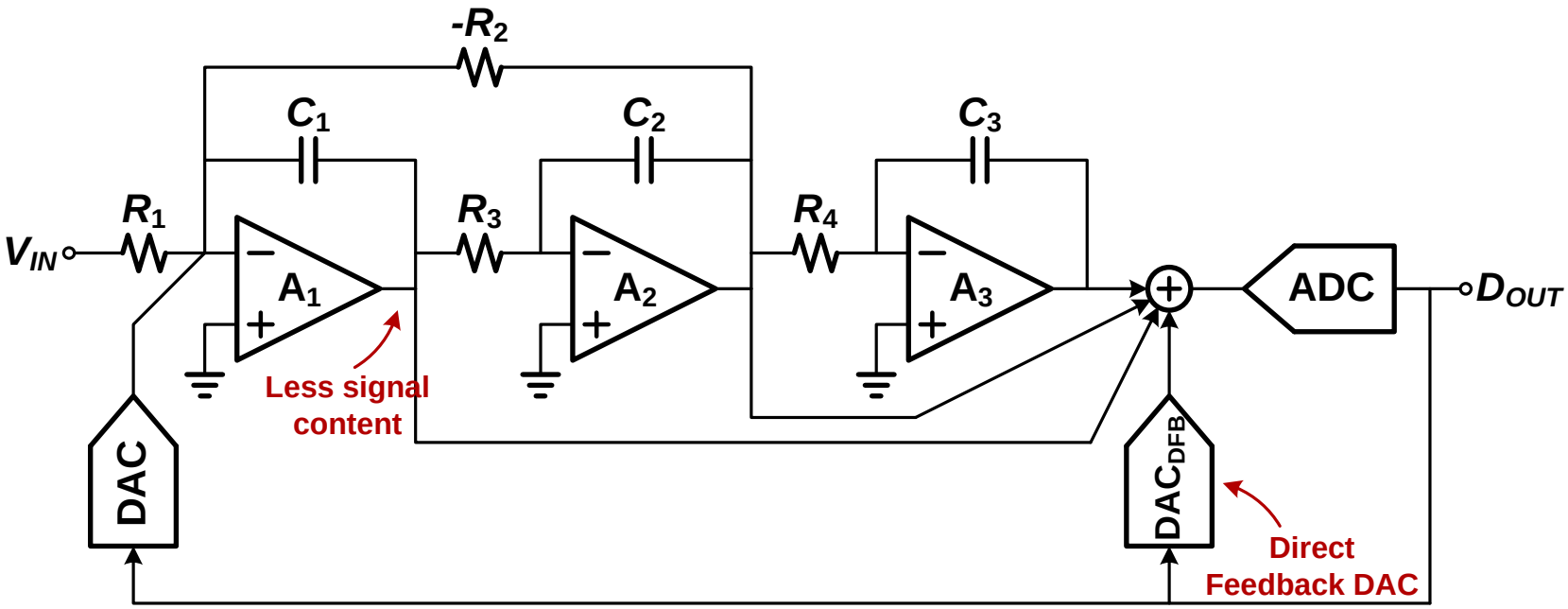
- **Inherent Anti-Aliasing**

  CT STF attenuates signals at multiples of F_S



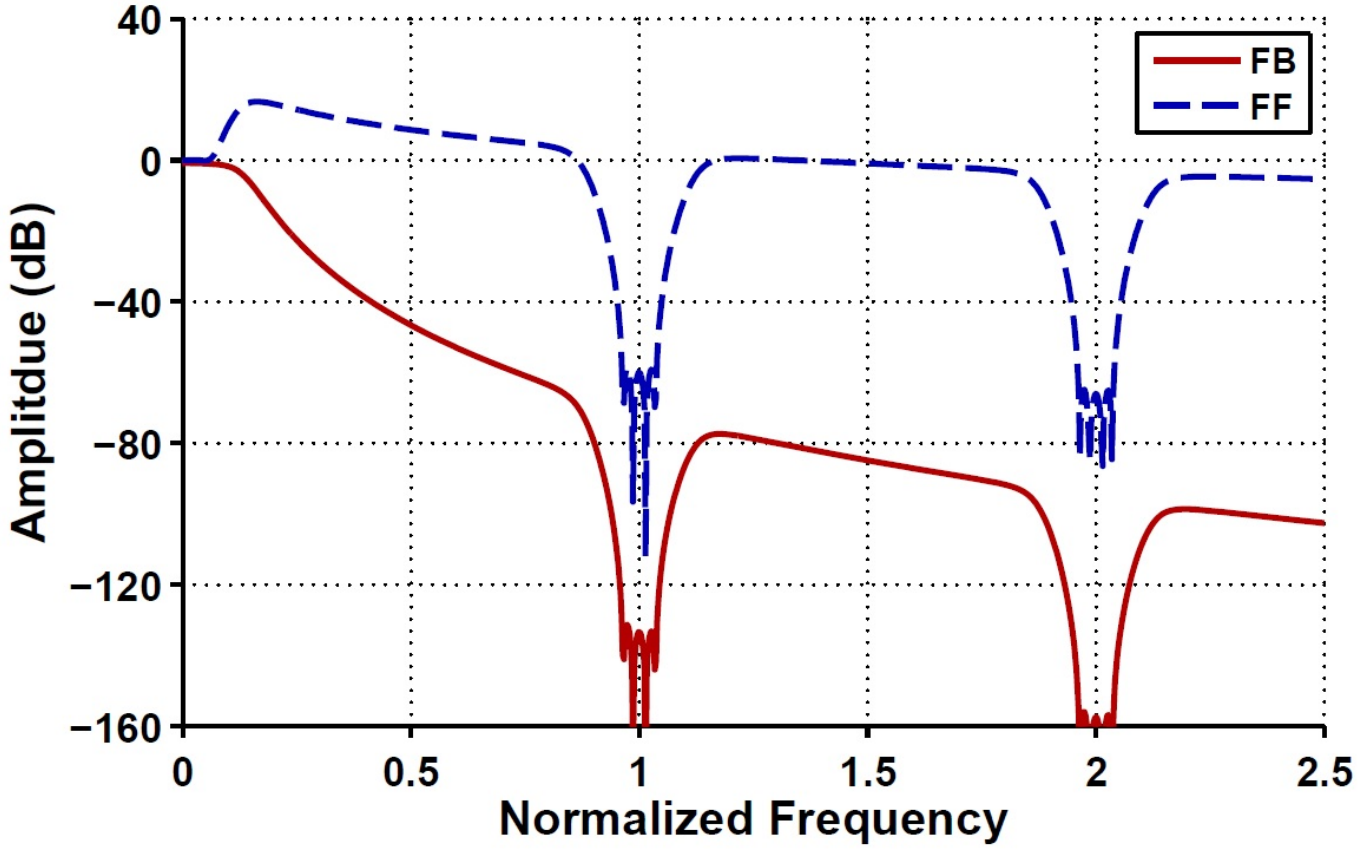
Advantages of CT ΔΣ Modulators

- **Anti-Aliasing with a feed-forward ΔΣ modulator**
  - ☺ **Power-efficient with higher front-end gain**
  - ☹ **Usually introduces out-of-band peaking in the STF**



Advantages of CT ΔΣ Modulators

- **Feed-forward and feedback STF comparison**
  - **Out-of-band peaking in FF STF, less immune to blockers**
  - **Reduced anti-aliasing in FF STF**

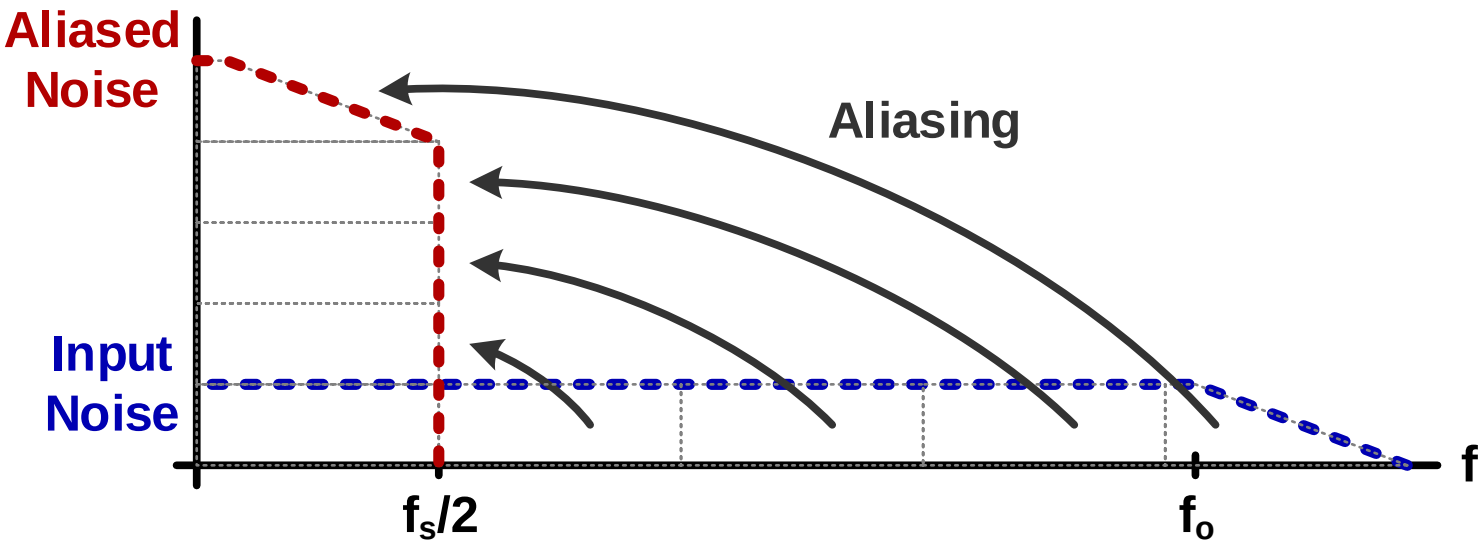


Advantages of CT ΔΣ Modulators

- **Noise Aliasing**

  In CT ΔΣ, sampling/aliasing occurs at the flash A/D input, some noise gets filtered before aliasing

  In DT ΔΣ, noise aliases at all stages in modulator and never gets filtered

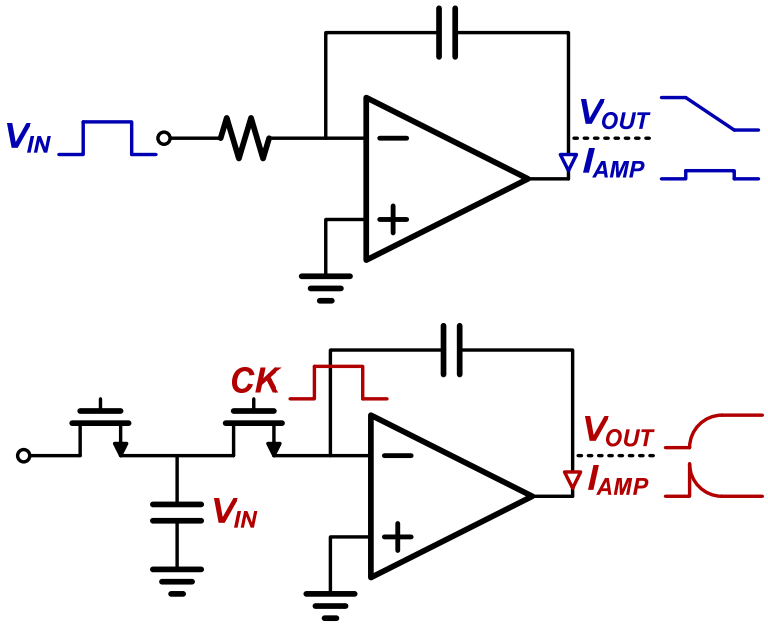


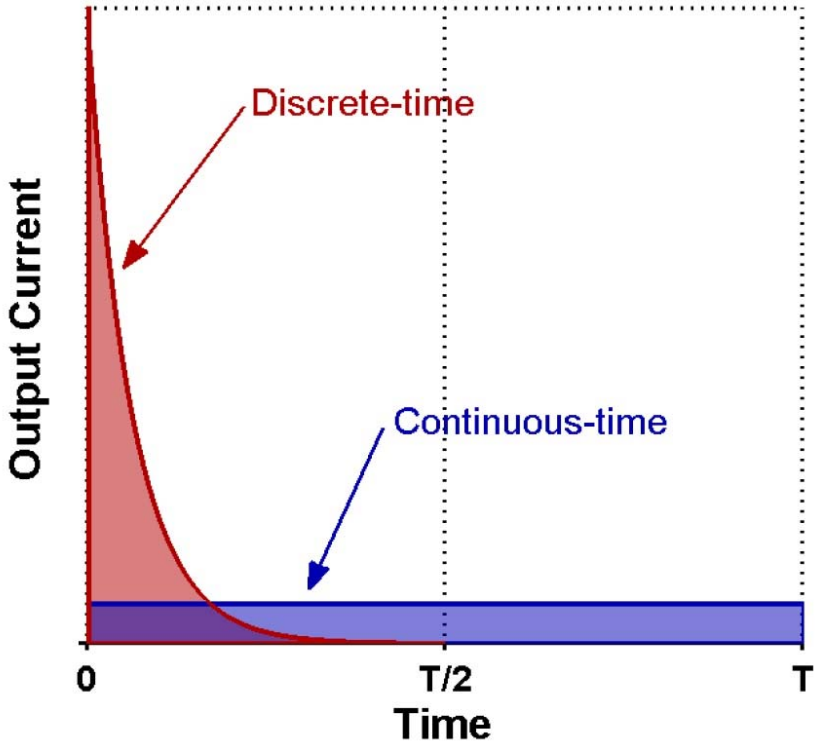
Advantages of CT ΔΣ Modulators

- **Maximum Amplifier Current**

  Continuous-time: Consistently low output current

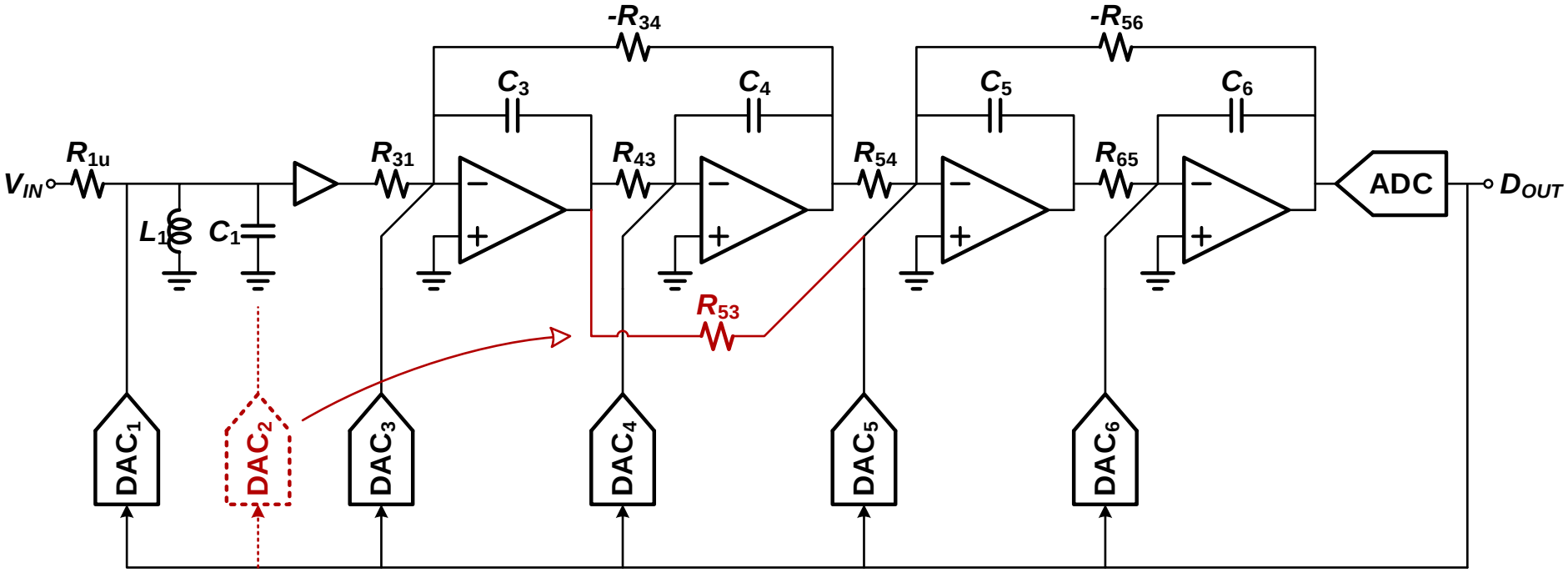
  Discrete-time: Same total charge, 16x peak current (assuming 5τ settling in T/2)





Advantages of CT ΔΣ Modulators

- **Bandpass ΔΣ ADCs**
  - **Same general structure as low pass CT ΔΣ ADC**
  - **Use LC or Active-RC resonators to move NTF zeros to frequencies other than DC**

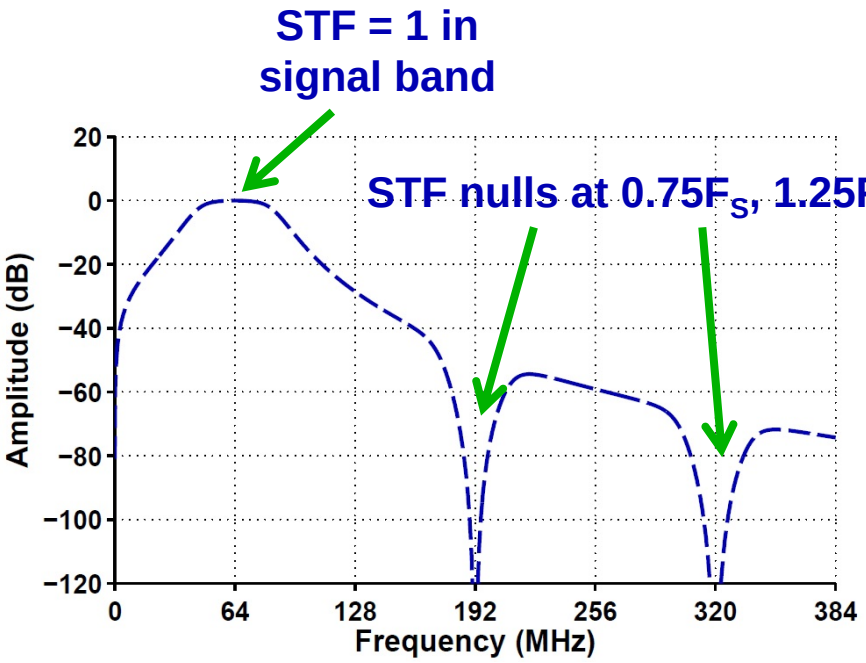


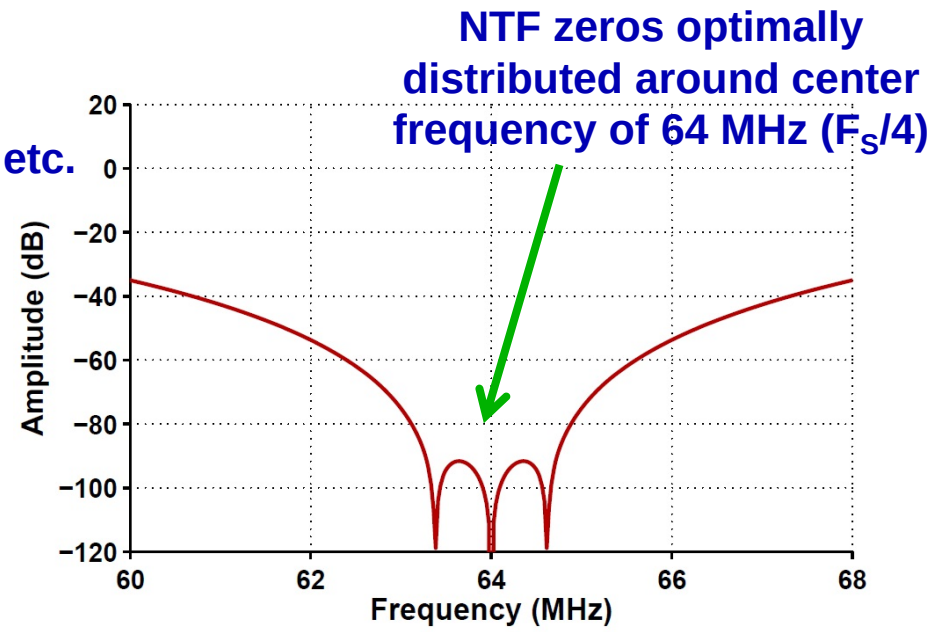
Advantages of CT ΔΣ Modulators

- **Bandpass ΔΣ ADCs**

  NTF becomes a bandpass transfer function

  Anti-aliasing preserved; STF has nulls at multiples of center frequency



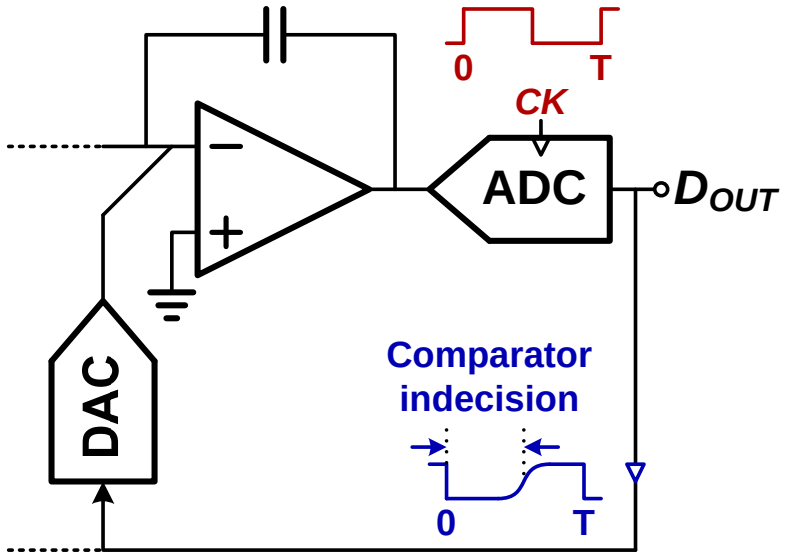


CT ADCs are faster than DT ADCs

- **DT switches are difficult in smaller technologies**
  - **DT needs bootstrapping**
  - **No switch settling required in CT $\Delta\Sigma$ ADCs**
- **CT amplifiers have higher bandwidths**
  - **Feed-forward amplifiers require lower unity-gain freqs, less peak current**
- **CT $\Delta\Sigma$ operations have a full period T**
  - **DT ADCs perform sample/integrate operations in T/2**
- **CT $\Delta\Sigma$ has lower metastability error**
  - **Metastability error can limit maximum frequency of ADC**
  - **In CT, full period T is available in feedback (with direct feedback path)**

Metastability

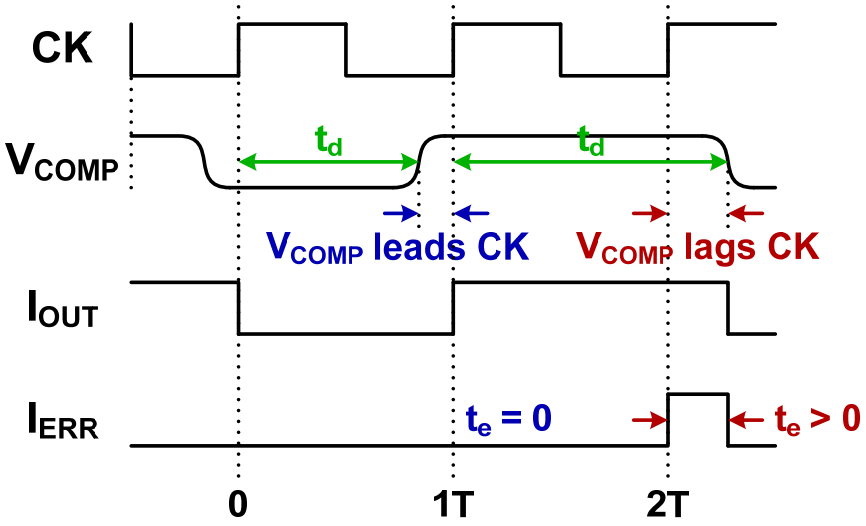
- **Indecision in comparator causes late DAC pulse**
  - **DAC signal is different from digital output D_{OUT}**
  - **Introduces error at input of $\Delta\Sigma$ modulator**
  - **Typically causes larger errors in DT $\Delta\Sigma$ over CT $\Delta\Sigma$**

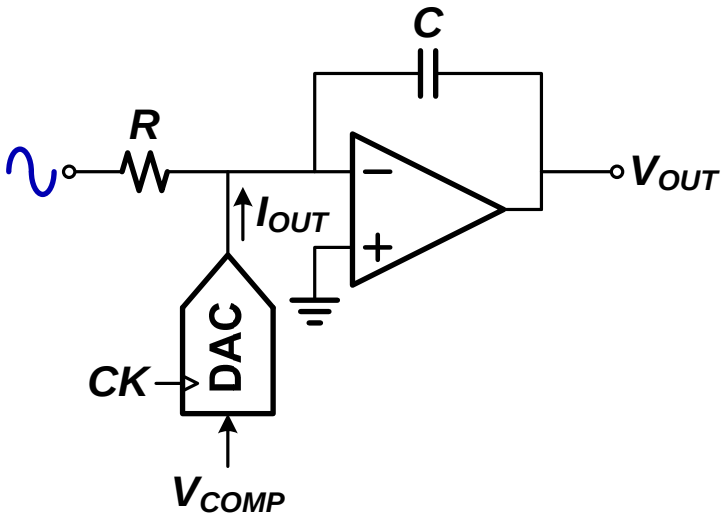


Metastability in CT ΔΣ

- **Continuous-Time Front-End**

  Error occurs when comparator metastability causes DAC pulse to arrive late





Metastability in CT ΔΣ

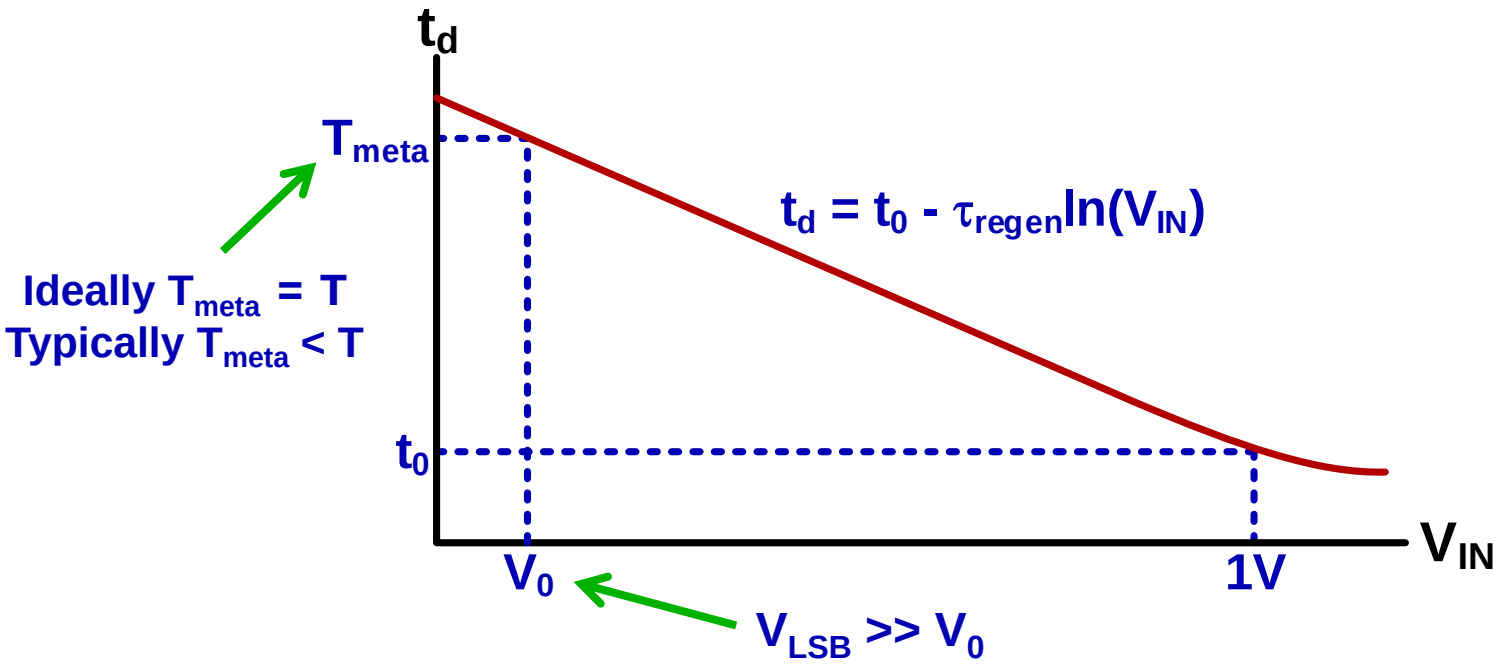
- **Comparator delay t_d depends on V_{IN}**

  τ_{regen}: latch regeneration time constant

  V_0: voltage below which metastability introduces error

  T_{meta}: delay above which metastability introduces error

  t_0: delay for an input of 1V (large signal delay)



Metastability in CT ΔΣ

- **Signal to Metastability Noise Ratio (SMNR)**

  M-element flash has only one comparator near threshold with a metastability error

  Oversampling advantage reduces metastability noise by OSR

$$SMNR = OSR\frac{M^2/2}{\sigma_{e_{meta}}{}^2}$$

$$\sigma_{e_{meta}}{}^2 = 2\left(\frac{2\tau_{regen}}{T}\right)^2 \cdot \frac{e^{-(T_{meta}-t_0)/\tau_{regen}}}{V_{LSB}}$$

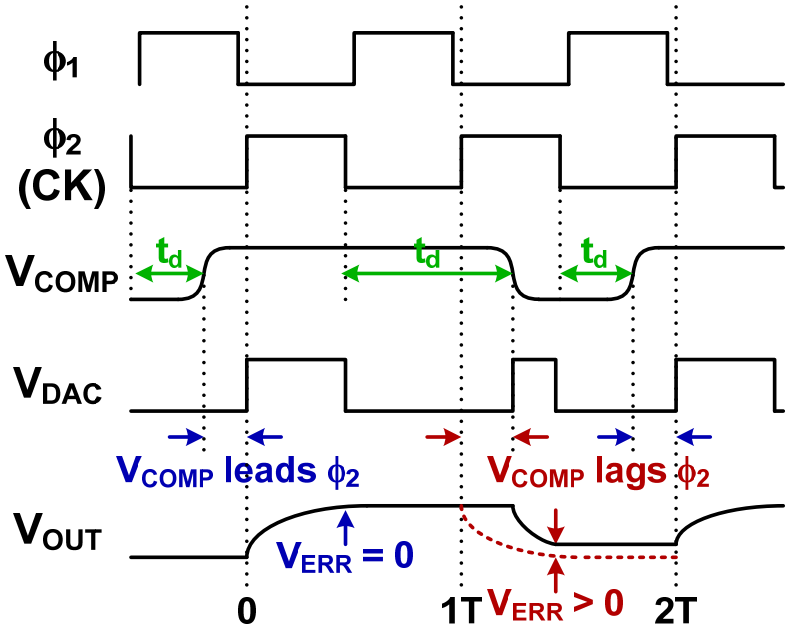
Ex: OSR = 8,M = 16,V_{LSB} = 25mV, τ_{regen} = 10ps, t_0 = 100ps

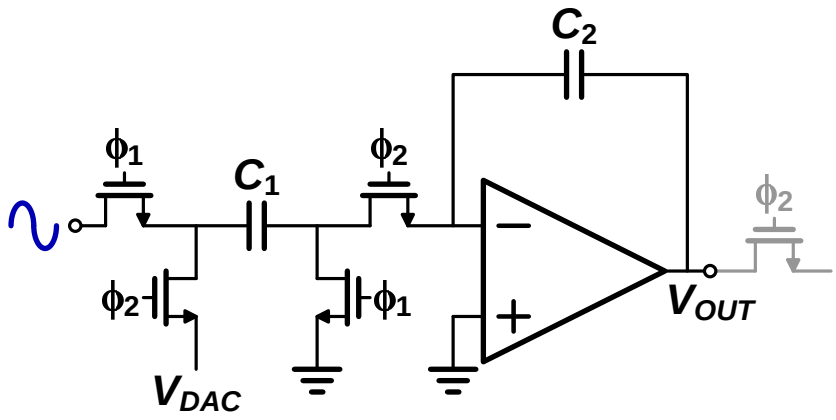
For SMNR > 80dB, 1 / T < 2.7GHz

Metastability in DT ΔΣ

- **Discrete-Time Front-End**

  Error occurs when comparator metastability gives amplifier less time to settle





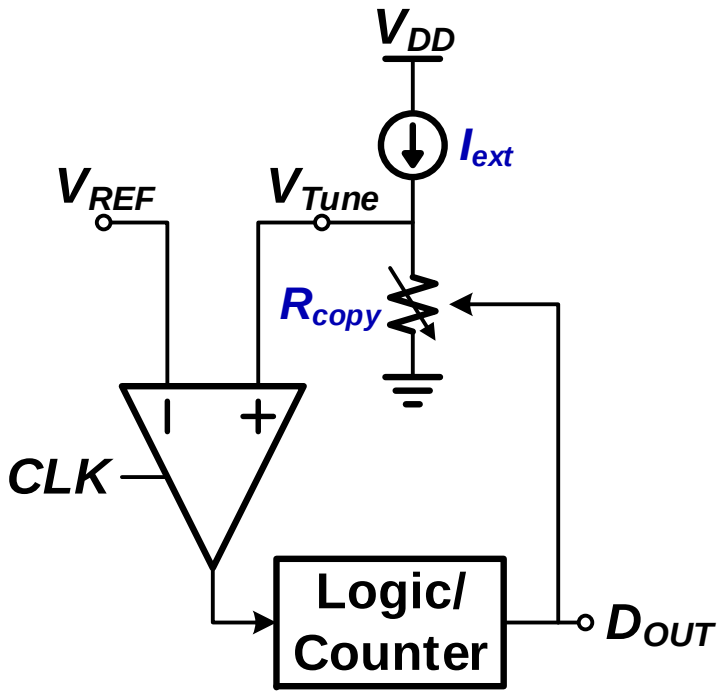
Recent High-Speed CT and DT ADCs

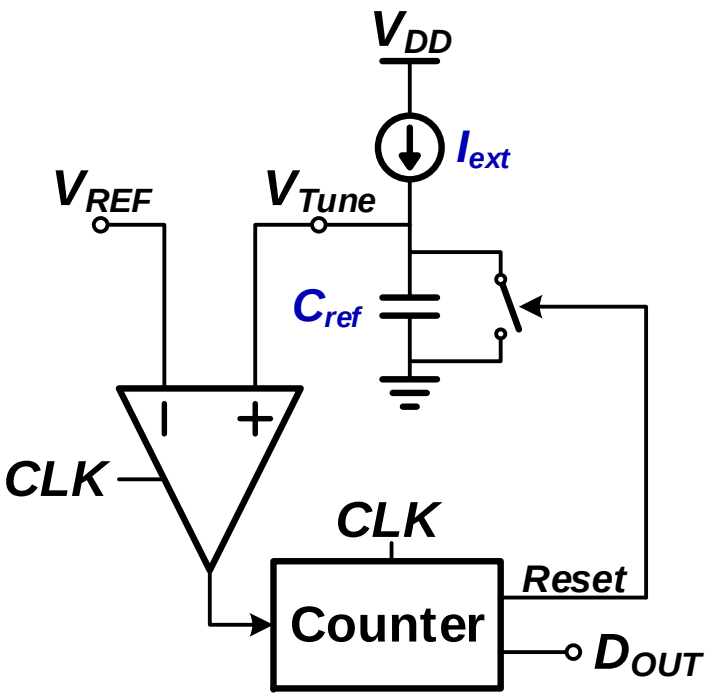
Continuous-Time	Architecture	Bandwidth	SNR/DR	Power	F_S	CMOS
Dong et al. ISSCC16	1-2 MASH (LP)	465 MHz	69 dB	930 mW	8 GHz	28 nm
Wu et al. ISSCC16	4^{th}-order FF (LP)	160 MHz	72 dB	40 mW	2.9 GHz	16 nm
Shibata et al. JSSC12	6^{th}-order FB (BP/LP)	150 MHz	74 dB	750 mW	4 GHz	65 nm
Bolatkale et al. JSSC11	3^{rd}-order FF (LP)	125 MHz	70 dB	260 mW	4 GHz	45 nm
Caldwell et al. CICC13	4^{th}-order FB (LP)	100 MHz	60 dB	95 mW	1.5 GHz	65 nm
Ho et al. VLSI14	4^{th}-order FF (LP)	80 MHz	73 dB	23 mW	2.2 GHz	20 nm
Srinivasan et al. ISSCC12	3^{rd}-order FF (LP)	60 MHz	62 dB	20 mW	6 GHz	45 nm
Dong et al. ISSCC14	0-3 MASH (LP)	53 MHz	83 dB	235 mW	3.2 GHz	28 nm
Yoon et al. ISSCC15	3-1 MASH (LP)	50 MHz	85 dB	78 mW	1.8 GHz	28 nm

Discrete-Time	Architecture	Bandwidth	SNR/DR	Power	F_S	CMOS
Ali et al. ISSCC14	Pipeline	500 MHz	69 dB	1200 mW	1 GHz	65 nm
Chen et al. VLSI11	TI Pipeline (x2)	1500 MHz	61 dB	500 mW	3 GHz	40 nm
Wu et al. ISSCC16	TI Pipeline (x4)	500 MHz	56 dB	300 mW	4 GHz	16 nm

Disadvantages of CT ΔΣ Modulators

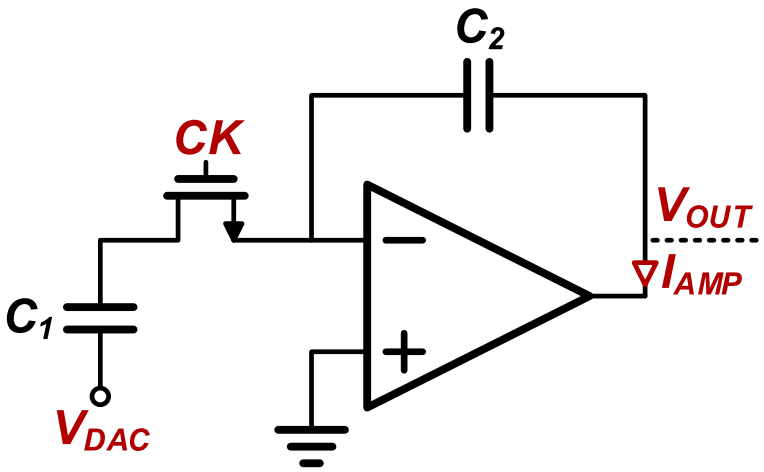
- **RC Tuning**
  - **CT ΔΣ transfer functions depend on RC time constants**
  - **Tuning required to match RC with sampling frequency**
  - **On-chip tuning is simple with modern technologies**

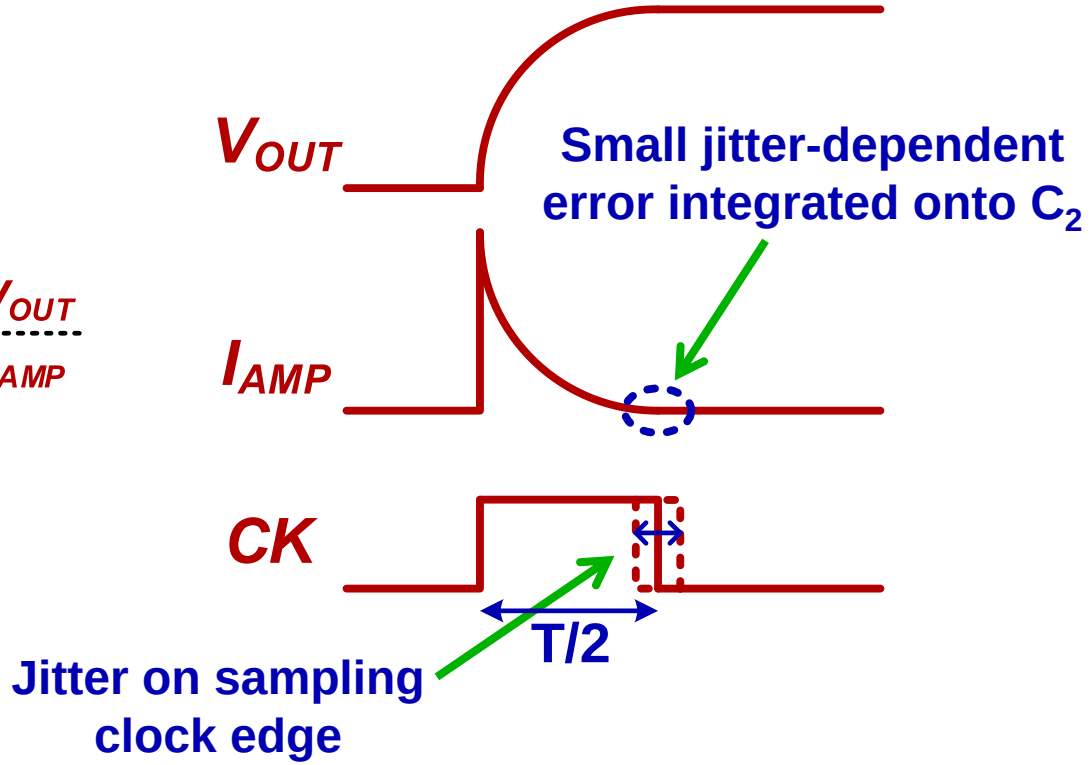




Disadvantages of CT ΔΣ Modulators

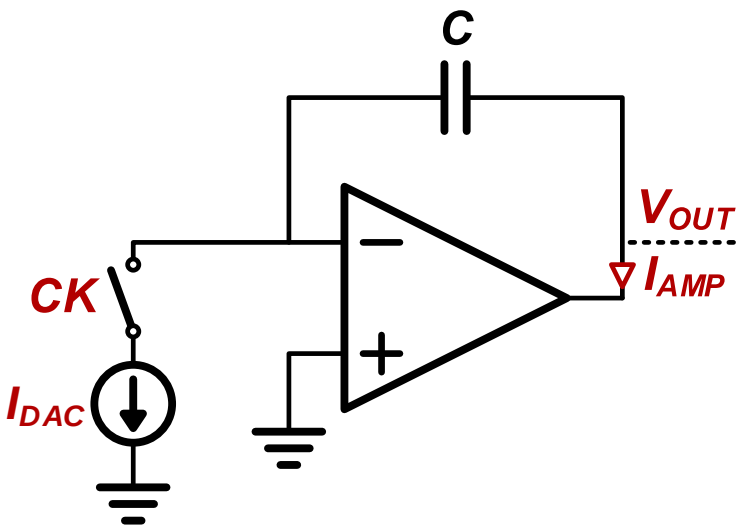
- **Jitter in DT feedback DAC**
  - **DAC signal is mostly supplied at start of clocking period**
  - **Error from jitter is small relative to total DAC signal**

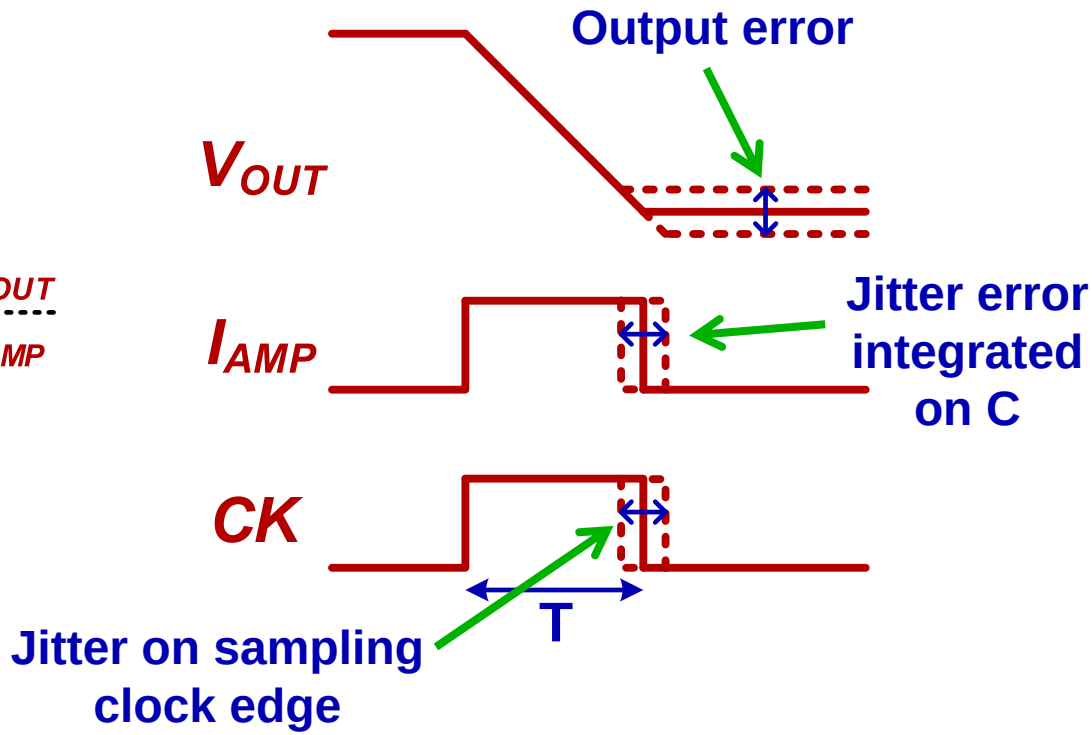




Disadvantages of CT ΔΣ Modulators

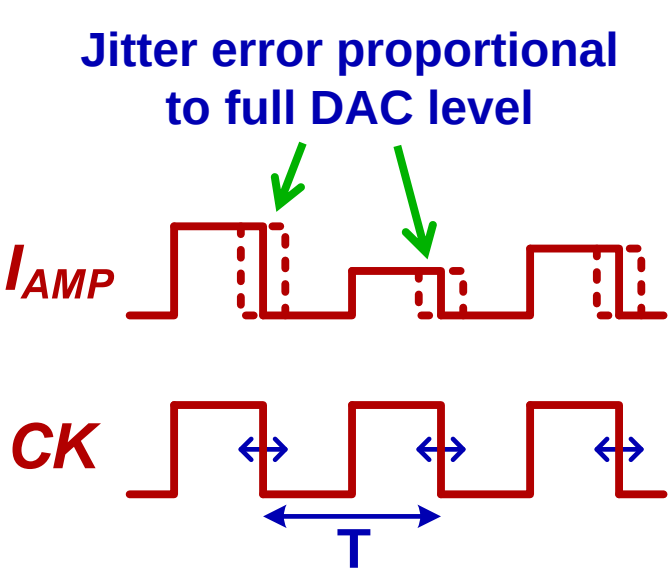
- **Jitter in CT feedback DAC**
  - **DAC signal is uniform throughout clocking period**
  - **Error from jitter is larger relative to total DAC signal**



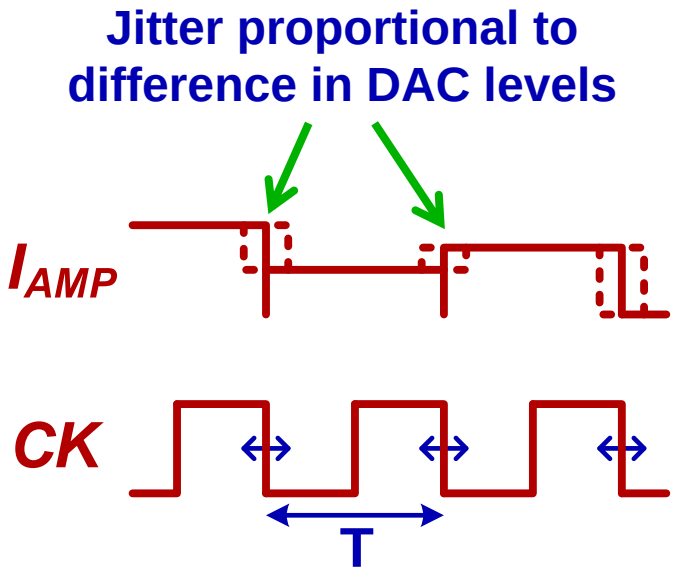


Disadvantages of CT ΔΣ Modulators

- **Return-to-Zero (RZ) vs Non-Return-to-Zero (NRZ)**
  - **NRZ has less jitter than RZ DAC pulses**
  - **Similarly, multi-bit DACs have less jitter than single-bit**



Return-to-Zero



Non-Return-to-Zero

What You Learned Today

- **Continuous-Time $\Delta\Sigma$ modulator**
- **Compare DT and CT $\Delta\Sigma$ ADCs**
  - **Differences in loop filter, amplifiers, DACs, DFB**
- **Advantages and disadvantages of CT circuits**
  - **CT $\Delta\Sigma$ ADCs are faster than DT**