Lecture 5
Example Design 1

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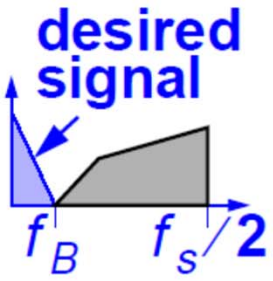
Lecture Plan

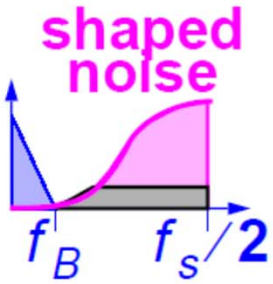
Date	Lecture (Wednesday 2-4pm)		Reference	Homework
2020-01-07	1	MOD1 & MOD2	PST 2, 3, A	1: Matlab MOD1&2
2020-01-14	2	MOD*N* + ΔΣ Toolbox	PST 4, B	2: ΔΣ Toolbox
2020-01-21	3	SC Circuits	R 12, CCJM 14	
2020-01-28	4	Comparator & Flash ADC	CCJM 10	3: Comparator
2020-02-04	5	Example Design 1	PST 7, CCJM 14	
2020-02-11	6	Example Design 2	CCJM 18	4: SC MOD2
2020-02-18	Reading Week / ISSCC			
2020-02-25	7	Amplifier Design 1		Project
2020-03-03	8	Amplifier Design 2		
2020-03-10	9	Noise in SC Circuits		
2020-03-17	10	Nyquist-Rate ADCs	CCJM 15, 17	
2020-03-24	11	Mismatch & MM-Shaping	PST 6	
2020-03-31	12	Continuous-Time ΔΣ	PST 8	
2020-04-07	Exam			
2020-04-21	Project Presentation (Project Report Due at start of class)			

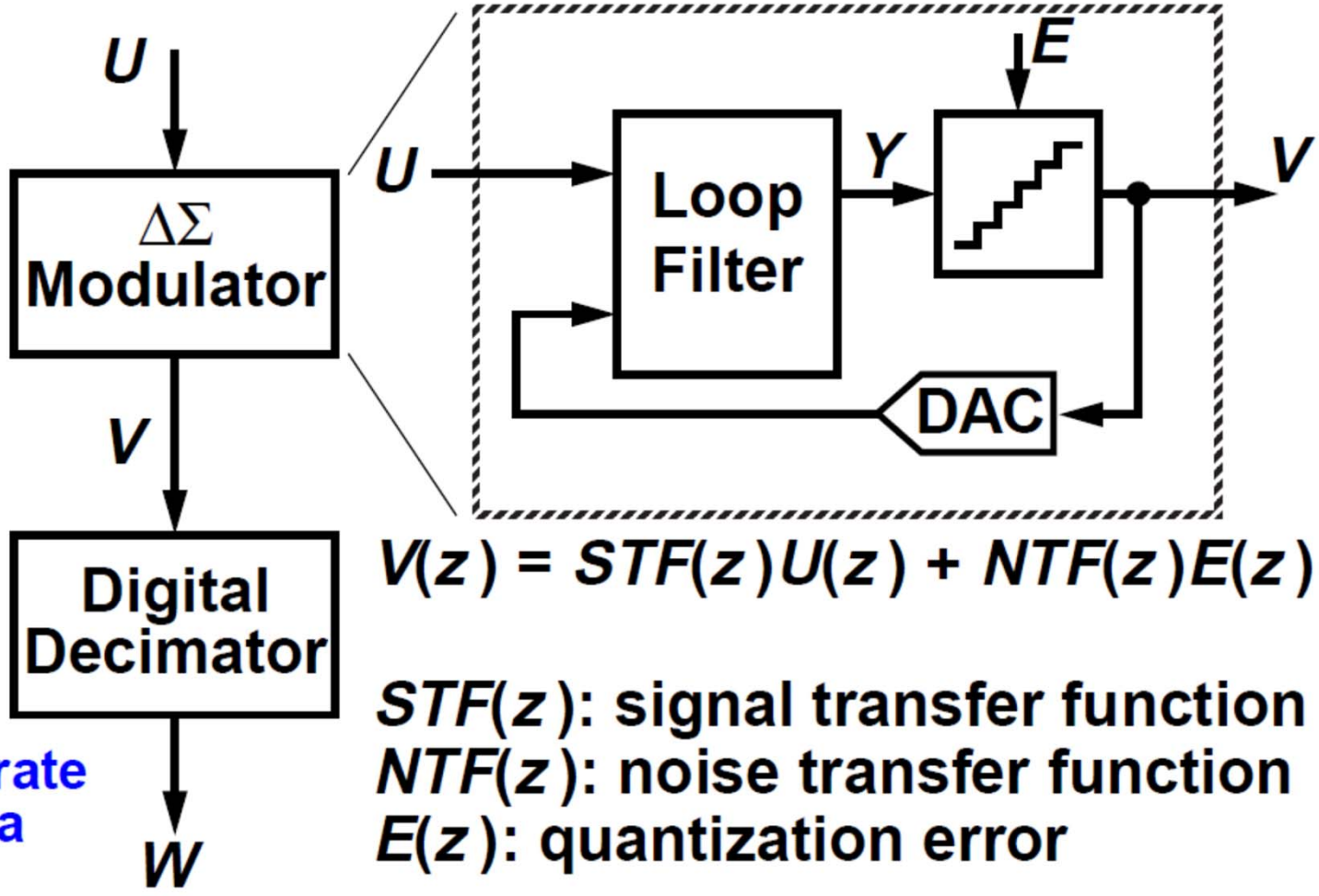
What you will learn…

- MOD2 implementation
- Switched-capacitor circuits
  - Switched-cap summer + DAC
- Dynamic-range scaling
- kT/C noise
- Verification strategy

Review: A ΔΣ ADC System



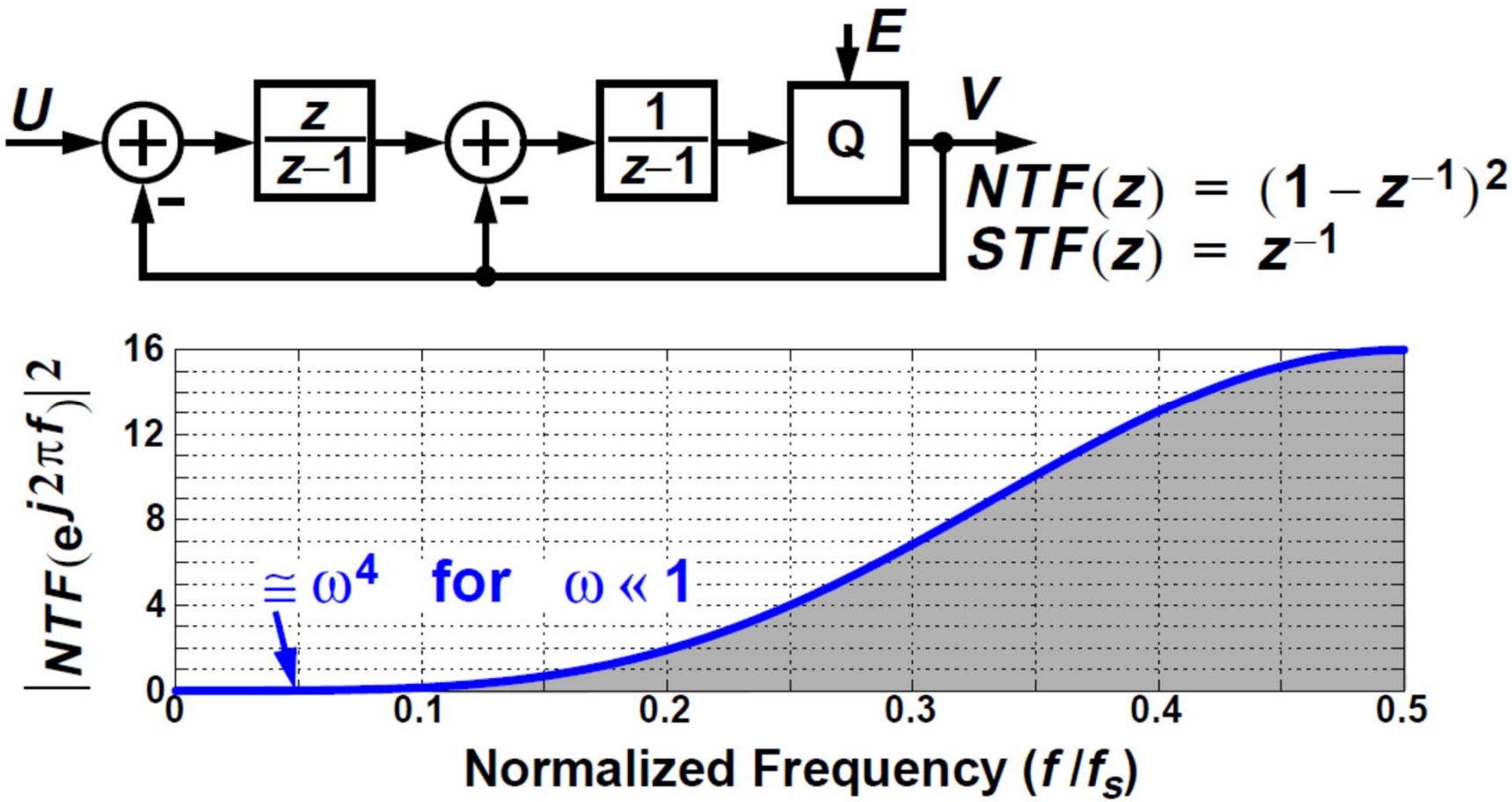




$$V(z) = STF(z)U(z) + NTF(z)E(z)$$

$STF(z)$: signal transfer function
$NTF(z)$: noise transfer function
$E(z)$: quantization error

Review: MOD2

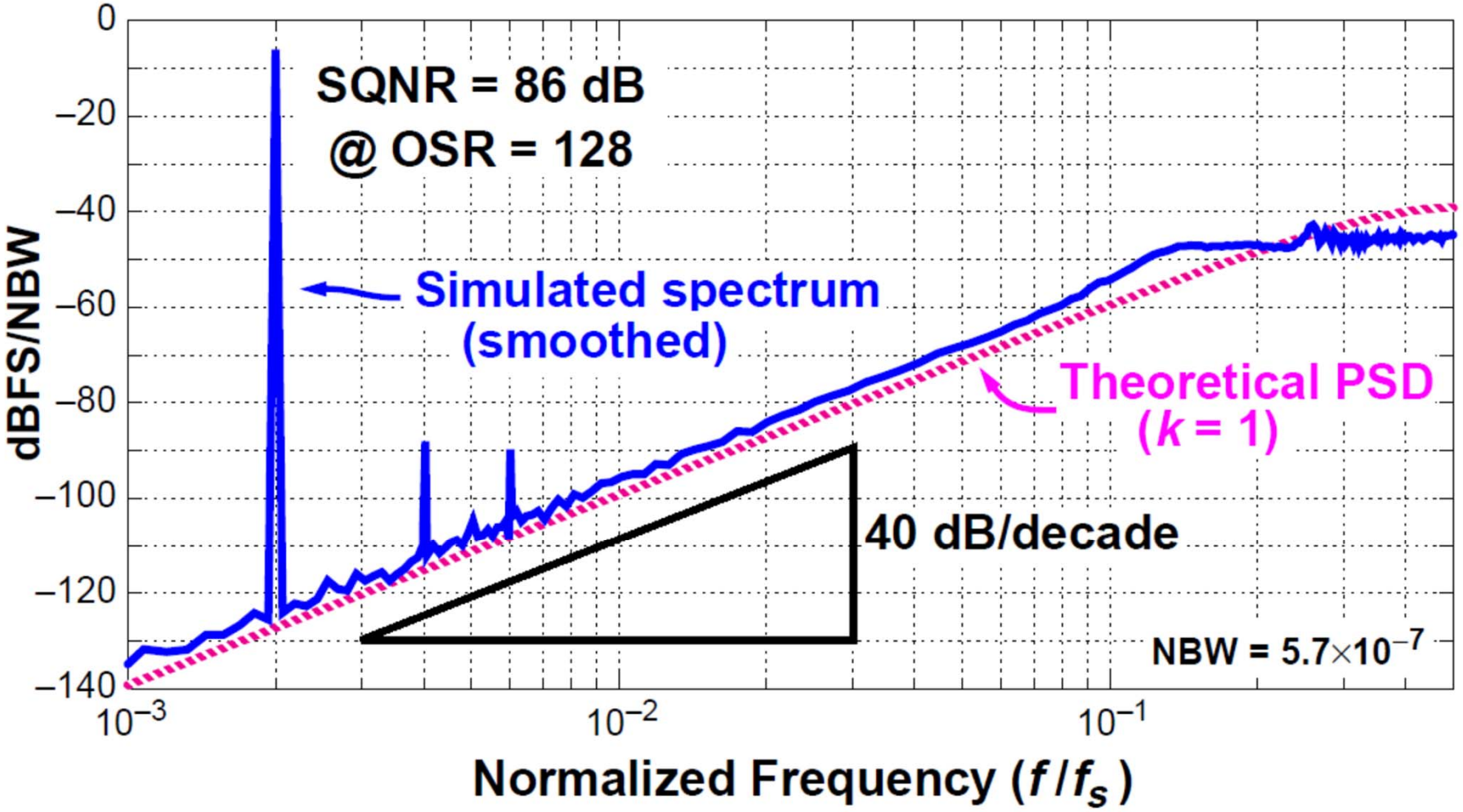


- **Doubling OSR improves SQNR by 15 dB**

  Peak SQNR ~ $10\log_{10}(5 \cdot OSR^5/\pi^4)$

Review: Simulated MOD2 PSD

- **Input at 50% of FullScale**



Review: Advantages of $\Delta\Sigma$

- **ADC: Simplified Anti-Alias Filter**
  - Since the input is oversampled, only very high frequencies alias to the passband
  - A simple RC filter often suffices
  - If a continuous-time loop filter is used, the anti-alias filter can be often eliminated altogether
- **Inherent Linearity**
  - Single-bit DAC structures can yield very high SNR
- **Robust Implementation**
  - $\Delta\Sigma$ tolerates sizable component errors

Let's Try Making One

- Clock at f_S = 1 MHz, assume BW = 1 kHz

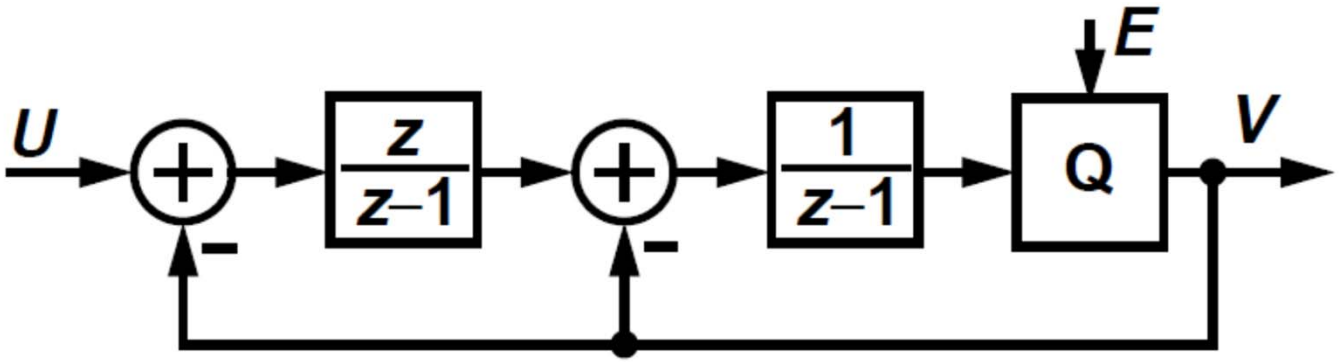
  → OSR = f_S / 2·BW = 500 ~ 2^9

- MOD1: SQNR ~ 9 dB/octave x 9 octaves = 81 dB
- MOD2: SQNR ~ 15 dB/octave x 9 octaves = 135 dB

  Actually more like 120 dB
- SQNR of MOD1 is not bad, but SQNR of MOD2 is very good

  In addition to MOD2's SQNR advantage, MOD2 is usually preferred over MOD1 because MOD2's quantization noise is more well-behaved

What Do We Need?

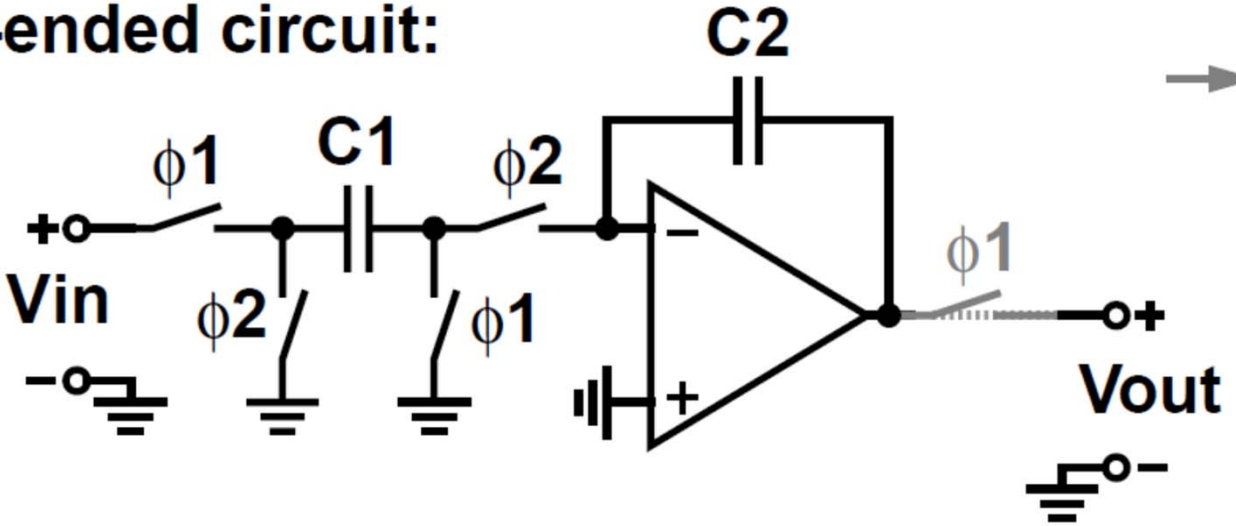


1. Summation blocks
2. Delaying and non-delaying discrete-time integrators
3. Quantizer (1-bit)
4. Feedback DACs (1-bit)
5. Decimation filter (not shown)

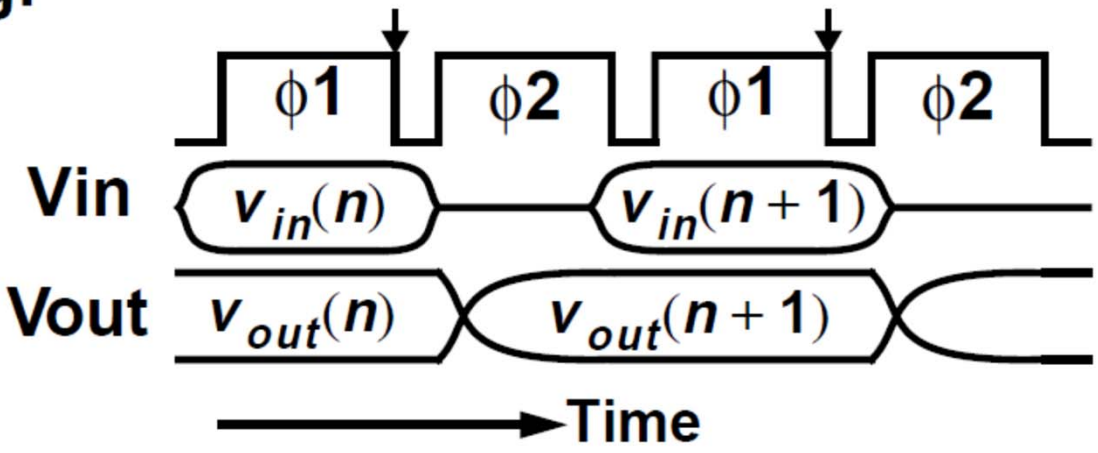
   Digital and therefore assumed to be easy

Switched-Capacitor Integrator

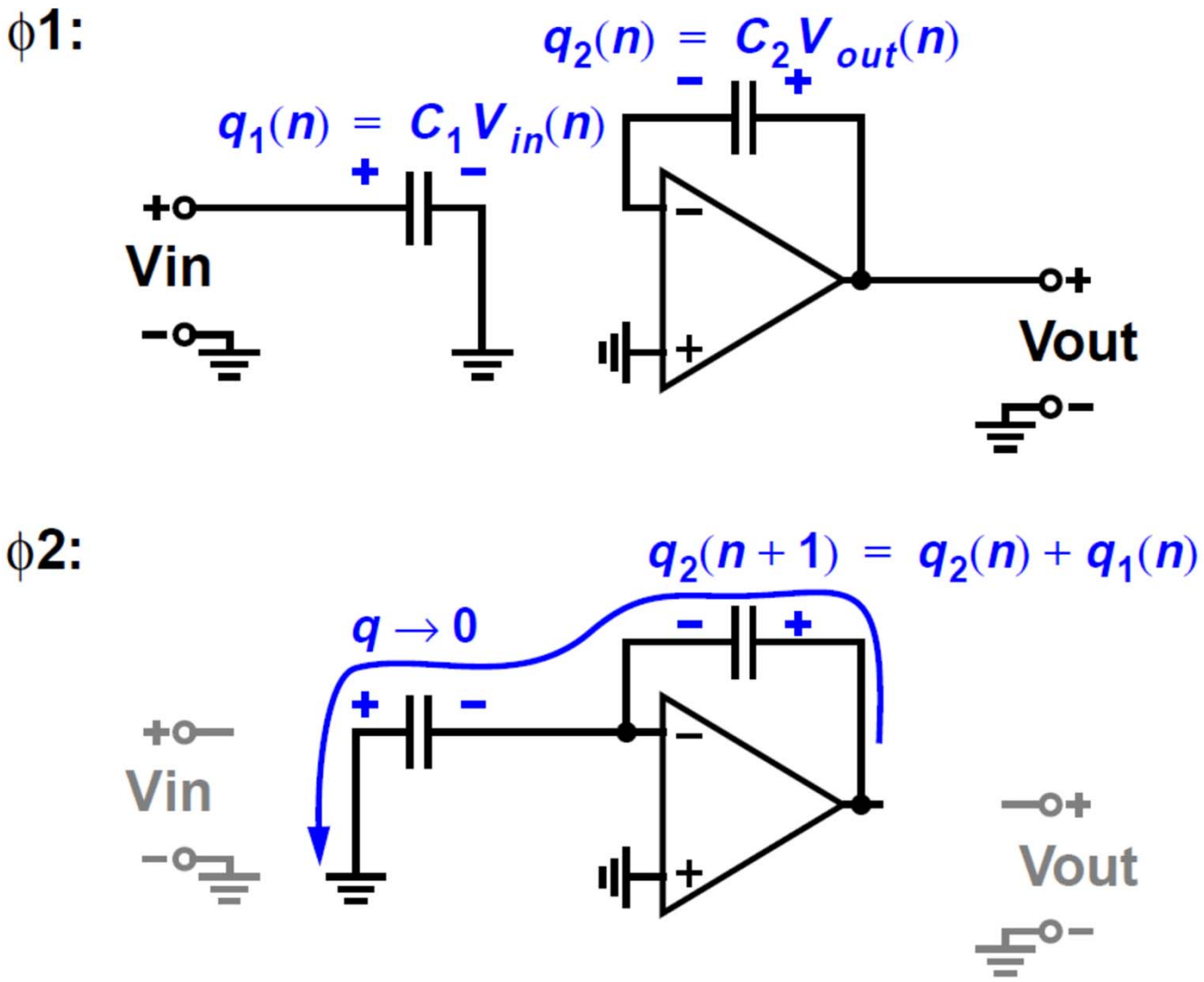
Single-ended circuit:



Timing:



Switched-Capacitor Integrator



Switched-Capacitor Integrator

$$q_2(n+1) = q_2(n) + q_1(n)$$

$$zQ_2(z) = Q_2(z) + Q_1(z)$$

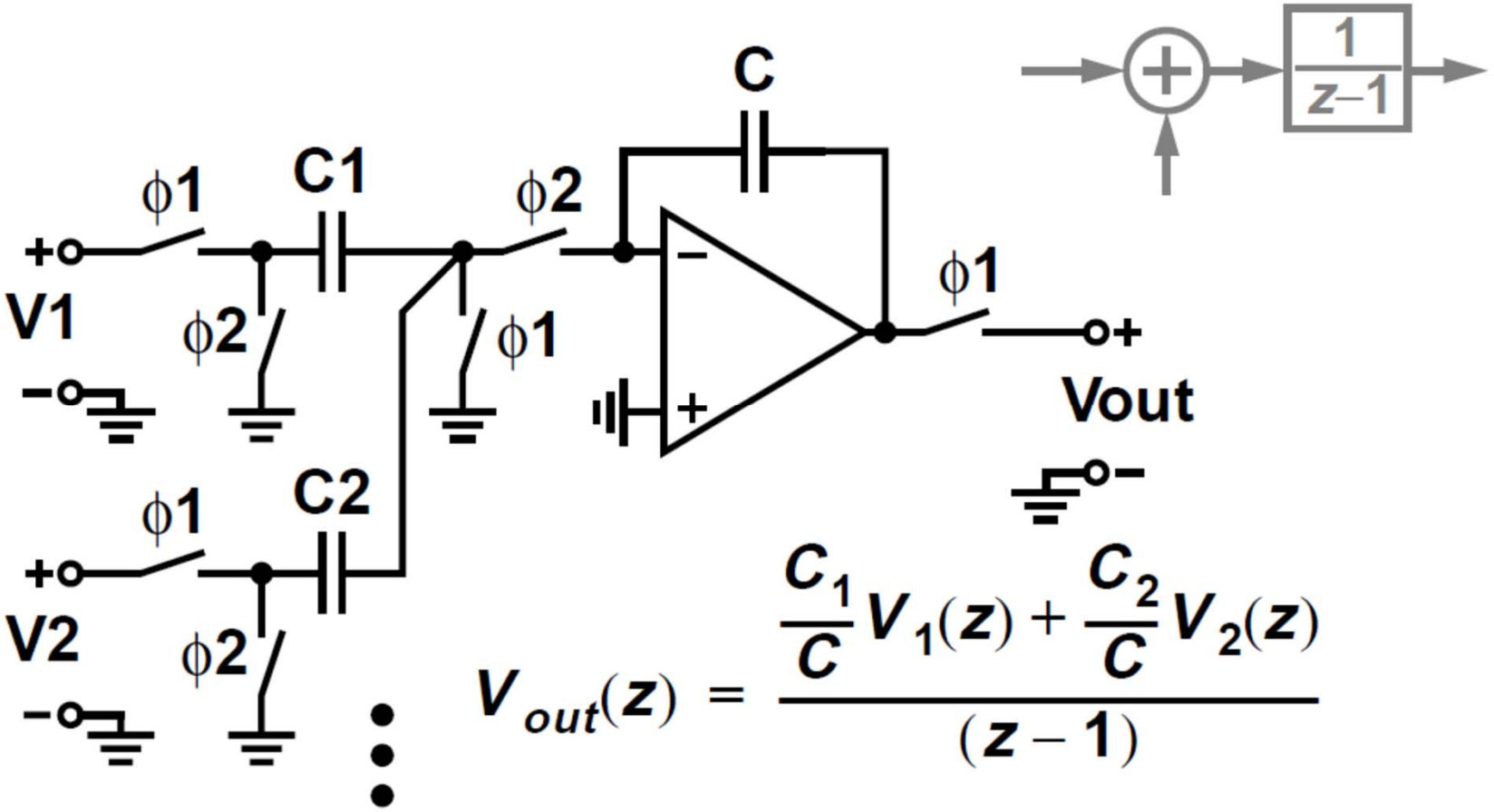
$$Q_2(z) = \frac{Q_1(z)}{z-1}$$

- Since $Q_1 = C_1 V_{in}$ and $Q_2 = C_2 V_{out}$

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1/C_2}{z-1}$$

- Voltage gain is controlled by a ratio of capacitors
  - With careful layout, 0.1% accuracy is possible

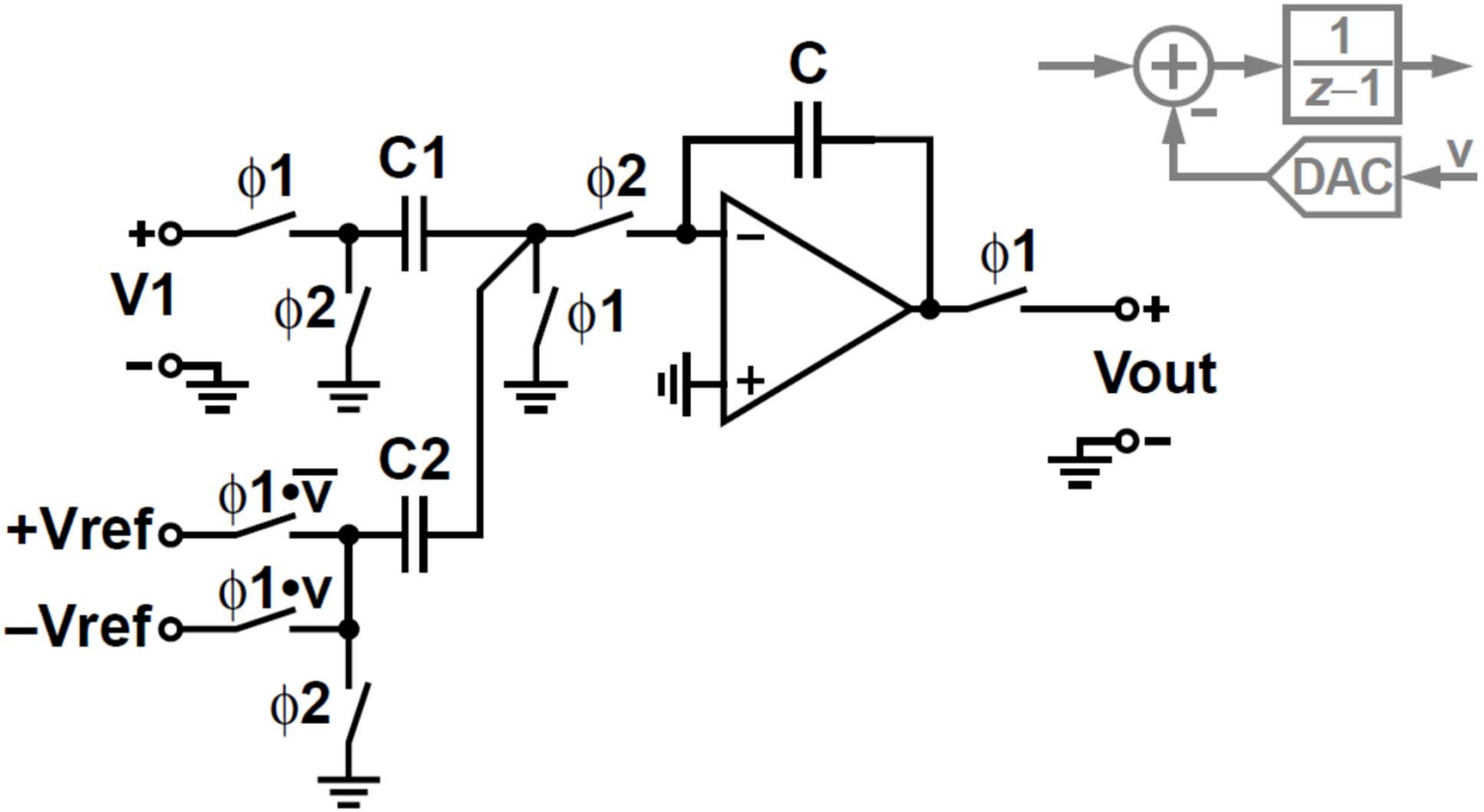
Summation + Integration



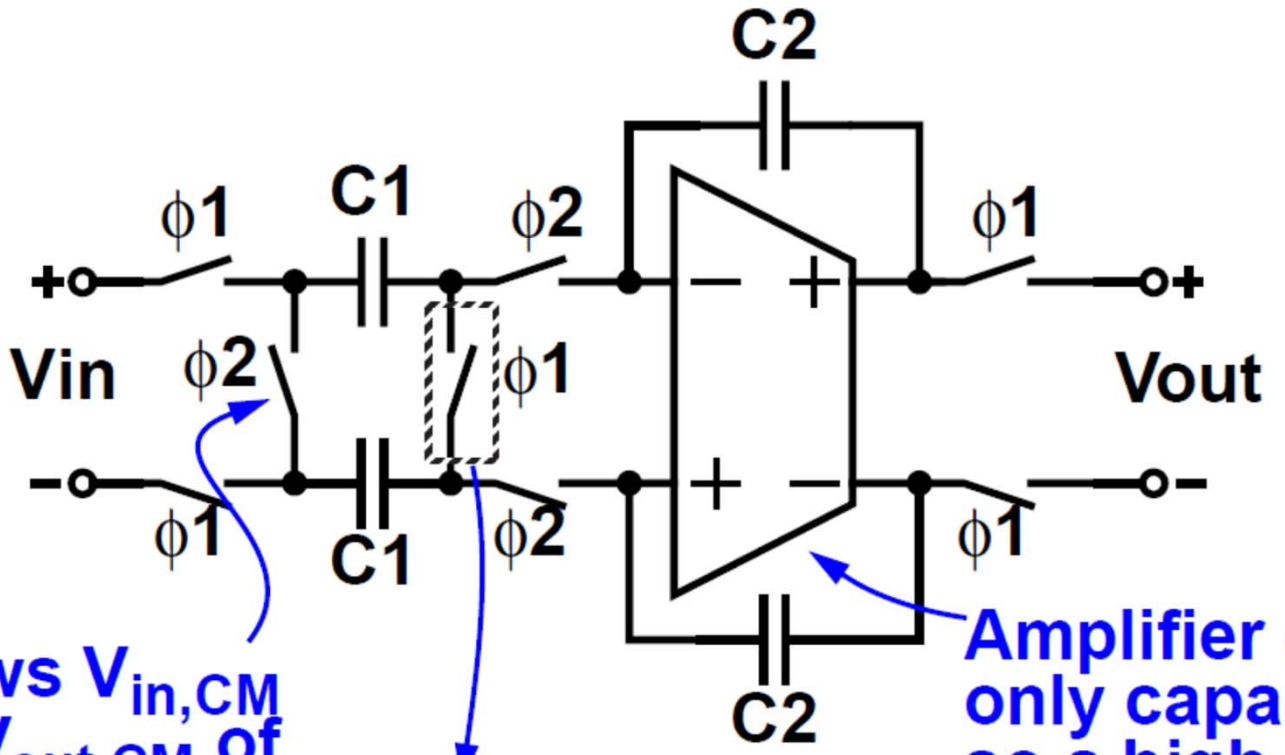
$$V_{out}(z) = \frac{\frac{C_1}{C}V_1(z) + \frac{C_2}{C}V_2(z)}{(z-1)}$$

- **Adding an extra input branch accomplishes addition, with weighting**

1b DAC + Summation + Integration

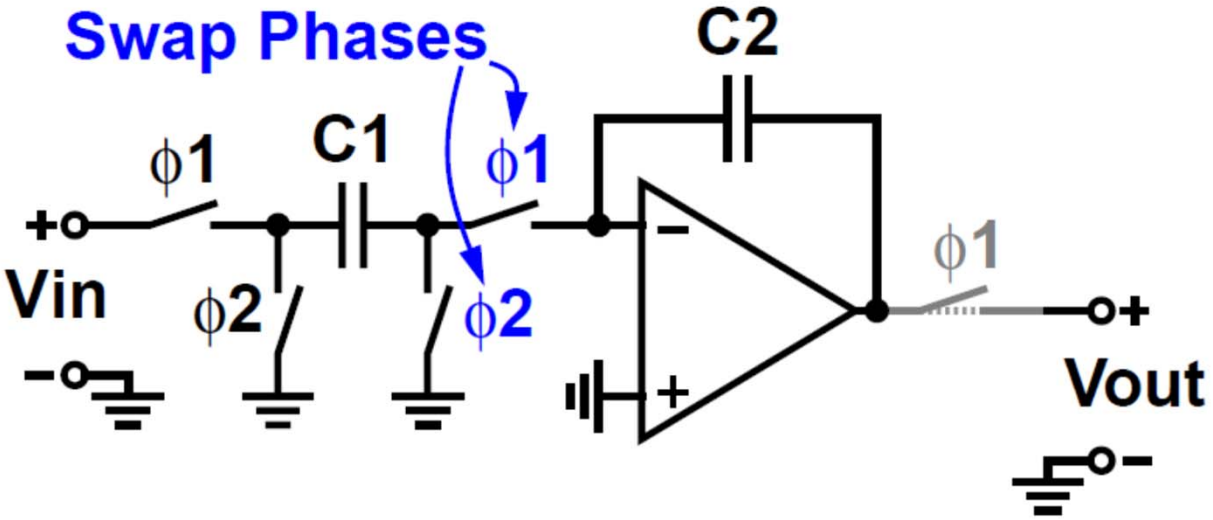


Differential Integrator

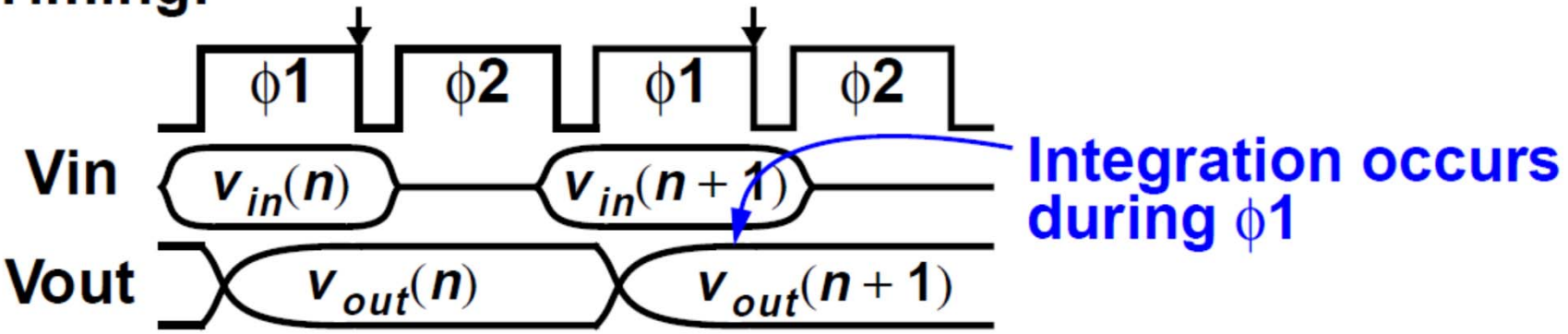


Non-Delaying Integrator

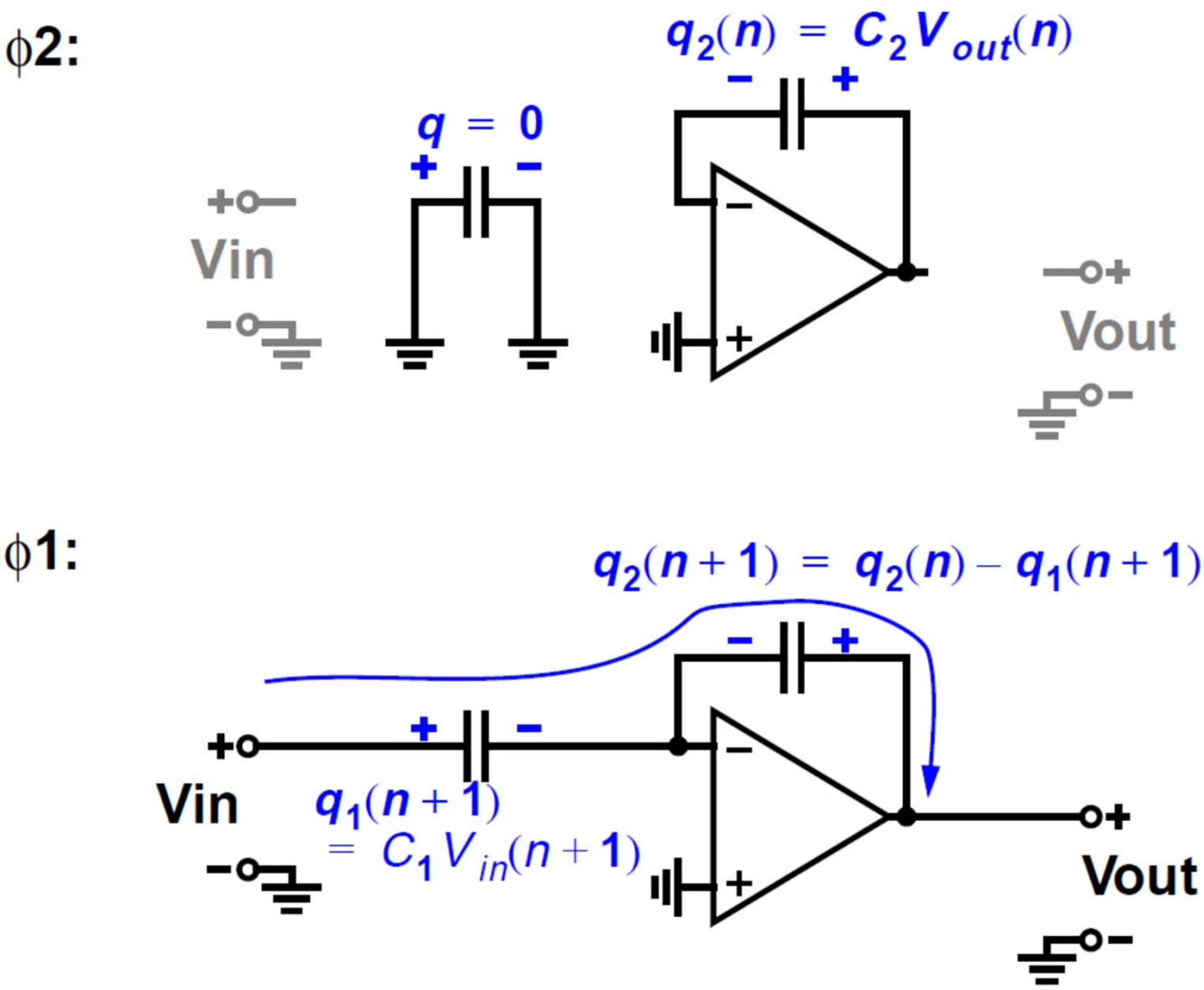
Single-ended circuit:



Timing:



Non-Delaying Integrator



Non-Delaying Integrator

$$q_2(n+1) = q_2(n) - q_1(n+1)$$

$$zQ_2(z) = Q_2(z) - zQ_1(z)$$

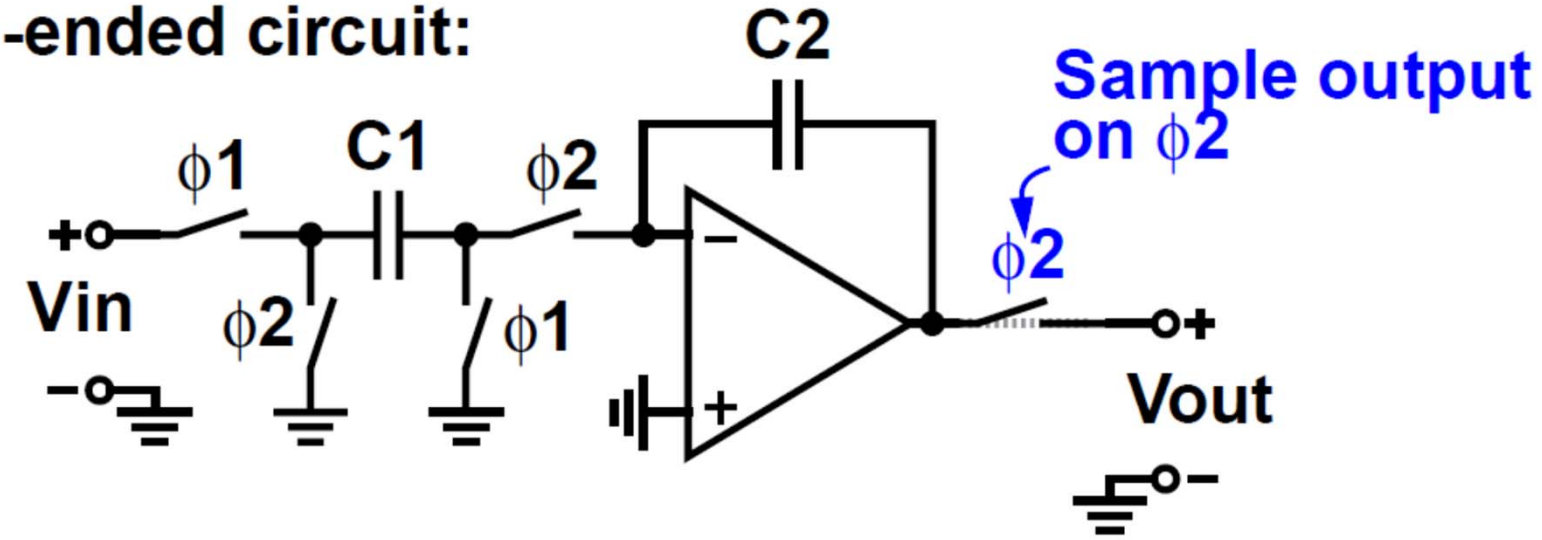
$$Q_2(z) = -\frac{zQ_1(z)}{z-1}$$

- **Delay-free integrator (inverting)**

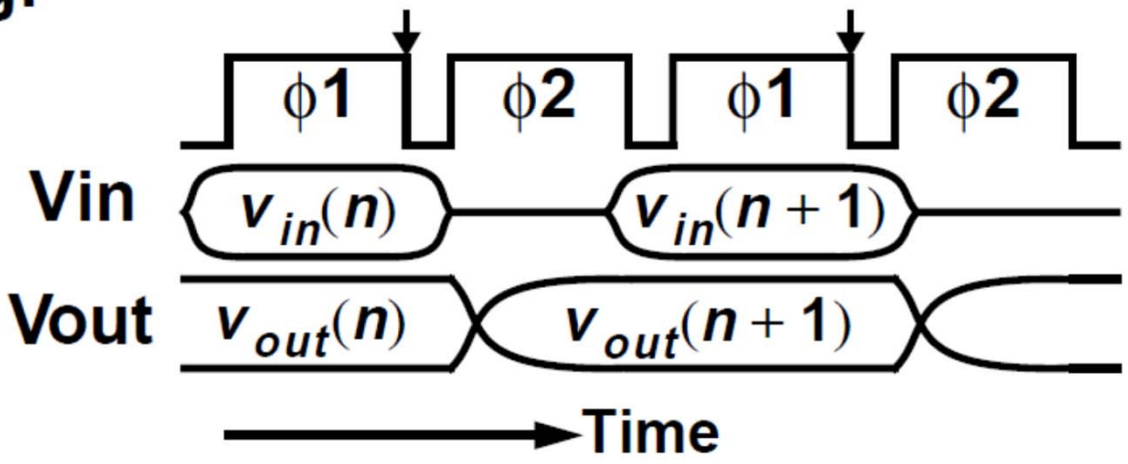
$$\frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2}\frac{z}{z-1}$$

Half-Delay Integrator

Single-ended circuit:



Timing:

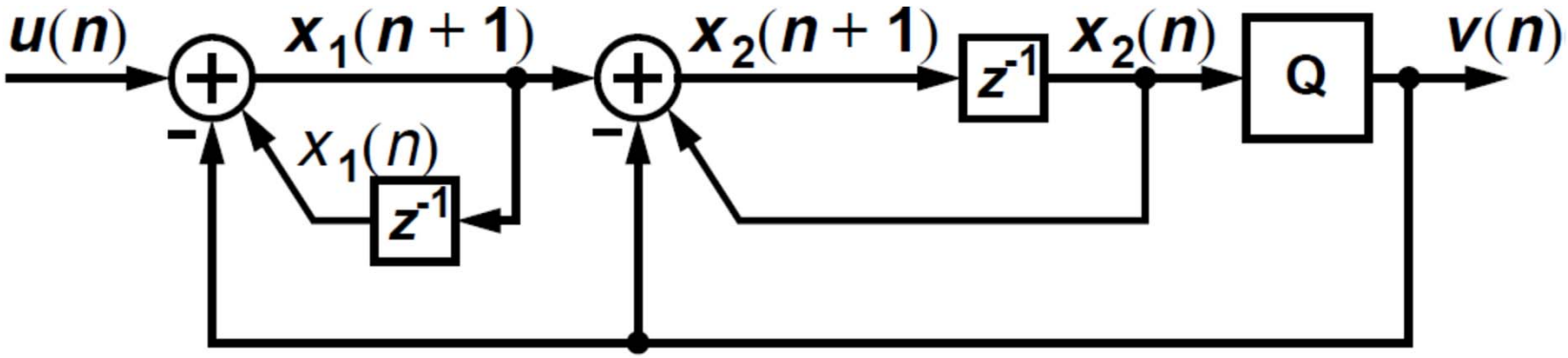


Half-Delay Integrator

- Output is sampled on a different phase than the input
- Some use the notation $H(z) = \frac{z^{1/2}}{z-1}$ to denote the shift in sampling time
- An alternative method is to declare that the border between time *n* and *n+1* occurs at the end of a specific phase, say ϕ_2
- A circuit which samples on ϕ_1 and updates on ϕ_2 is non-delaying (ie, $H(z) = z/(z-1)$) whereas a circuit which samples on ϕ_2 and updates on ϕ_1 is delaying (ie, $H(z) = 1/(z-1)$)

Timing in a ΔΣ ADC

- **The safest way to deal with timing is to construct a timing diagram and verify that the circuit implements the desired difference equations**
- **E.g. MOD2:**



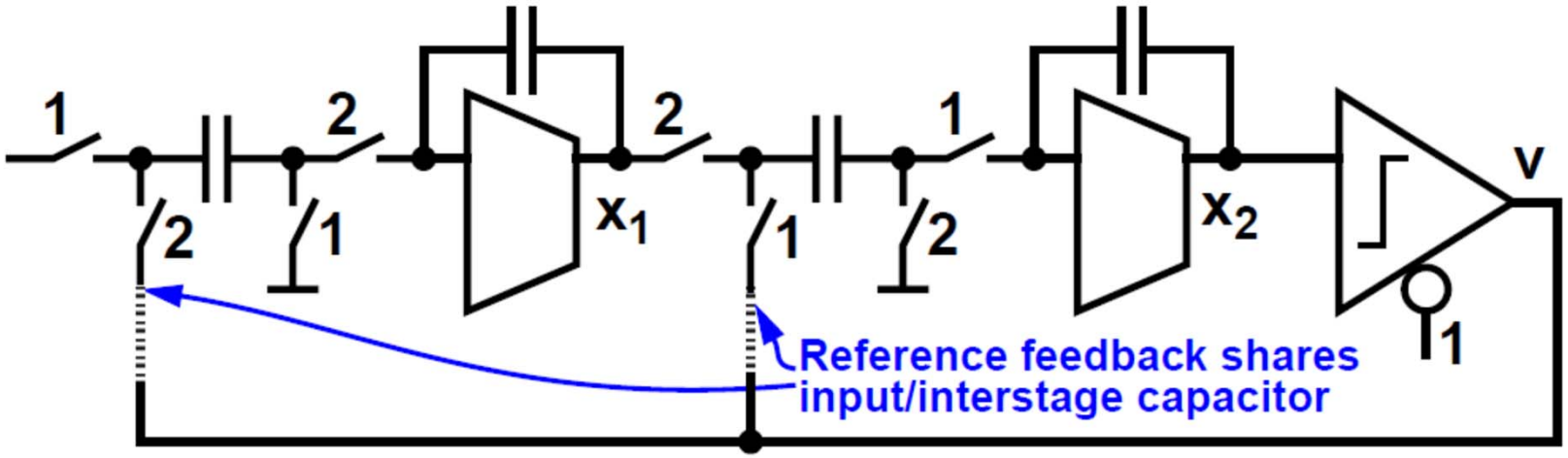
Difference Equations:

$$v(n) = Q(x_2(n)) \quad (0)$$

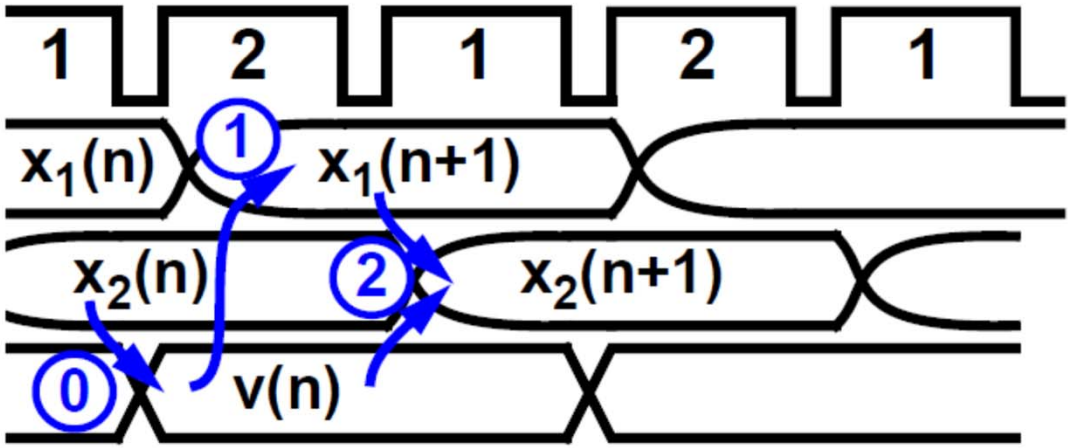
$$x_1(n+1) = x_1(n) - v(n) + u(n) \quad (1)$$

$$x_2(n+1) = x_2(n) - v(n) + x_1(n+1) \quad (2)$$

Switched-Capacitor Realization



Timing



Timing looks OK!

Signal Swing

- So far, we have not paid any attention to how much swing the op amps can support, or to the magnitudes of u, V_{ref}, x_1 and x_2
- For simplicity, assume:

  The full-scale range of u is +/- 1 V

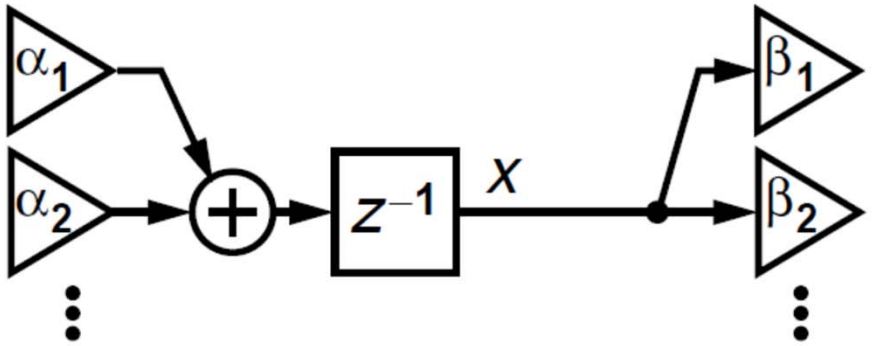
  The op-amp swing is also +/- 1 V

  V_{ref} = 1 V
- We still need to know the ranges of x_1 and x_2 in order to accomplish *dynamic-range scaling*

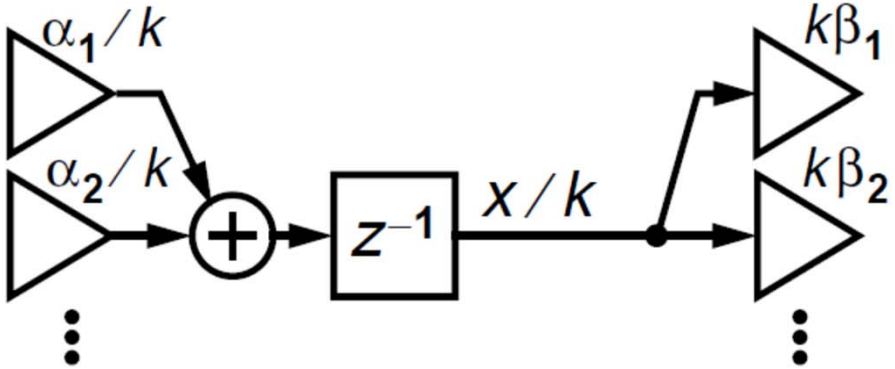
Dynamic-Range Scaling

- **In a linear system with known state bounds, the states can be scaled to occupy any desired range**

e.g. one state of original system:

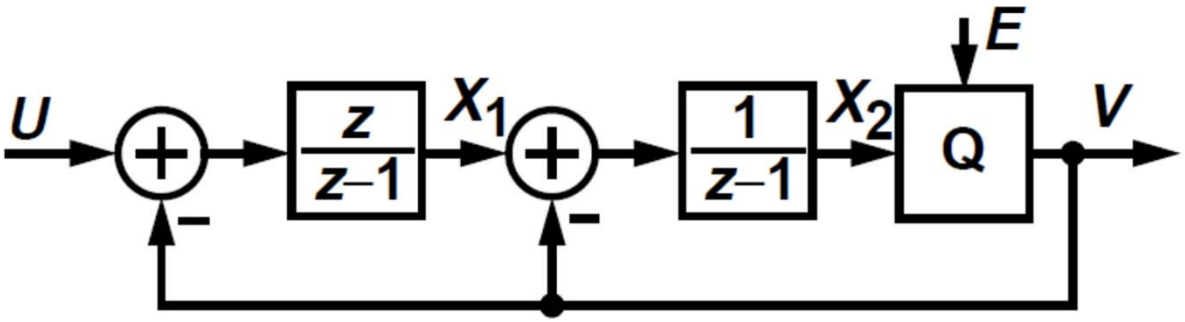


state scaled by 1/*k*:



State Swings in MOD2

- **Linear Theory**



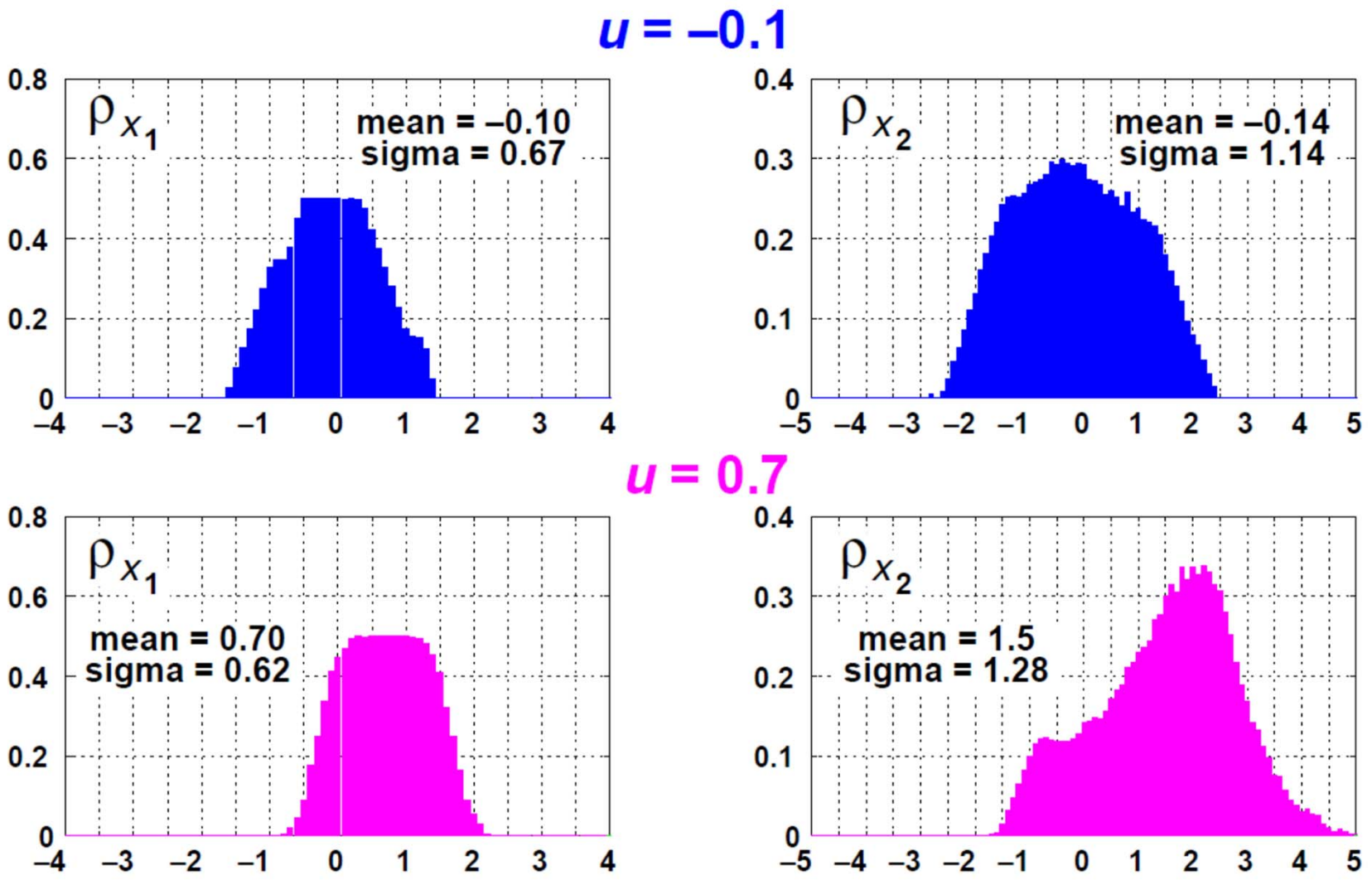
$$V = z^{-1}U + (1 - z^{-1})^2 E$$

$$X_1 = \frac{z}{z-1}(U - V) = U - (1 - z^{-1})E$$

$$X_2 = V - E = z^{-1}U + (-2z^{-1} + z^{-2})E$$

- **If u is constant and e is white with power $\sigma_e^2 = 1/3$, then $\overline{x_1} = u$, $\sigma_{x_1}^2 = 2\sigma_e^2 = 2/3$, $\overline{x_2} = u$ and $\sigma_{x_2}^2 = 5\sigma_e^2 = 5/3$**

Simulated Histograms



Observations

- **The match between simulations and our linear theory is fair for x_1, but poor for x_2**

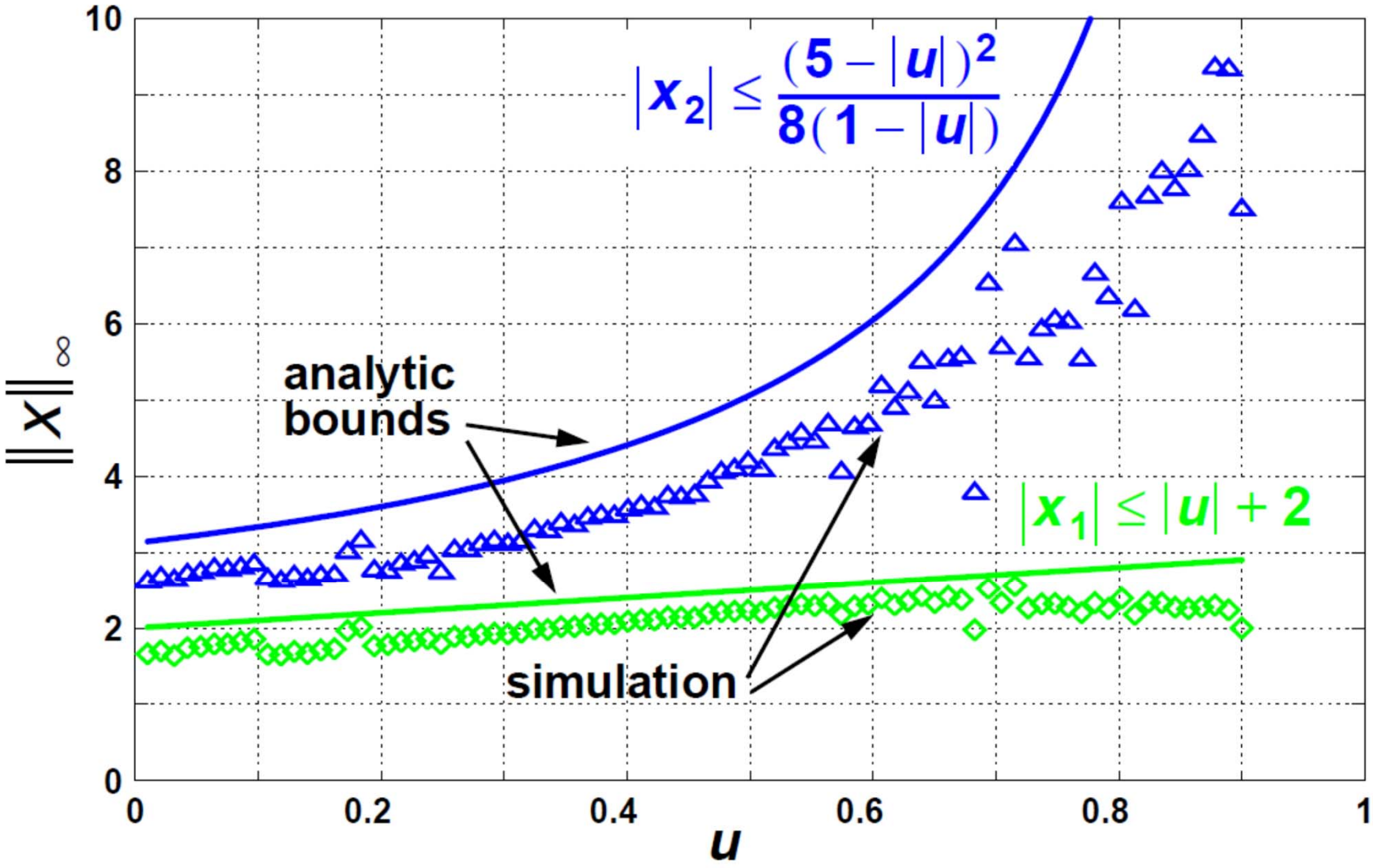
  x_1's mean and standard deviation match theory, although x_1's distribution does not have the triangular form that would result if e were white and uniformly distributed in [-1, 1]

  x_2's mean is 50-100% high, its standard deviation is ~25% low, and the distribution is weird

- **Our linear theory is not adequate for determining signal swings in MOD2**

  No real surprise since linear theory does not handle overload (ie, where x_1 or x_2 go to infinity when u > 1)

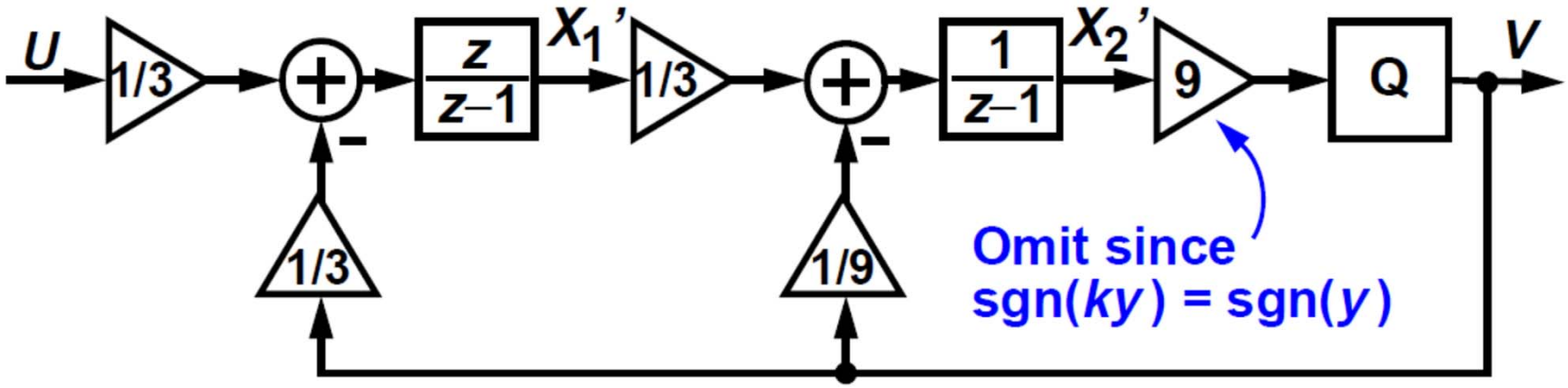
MOD2 Simulated State Bounds



Scaled MOD2

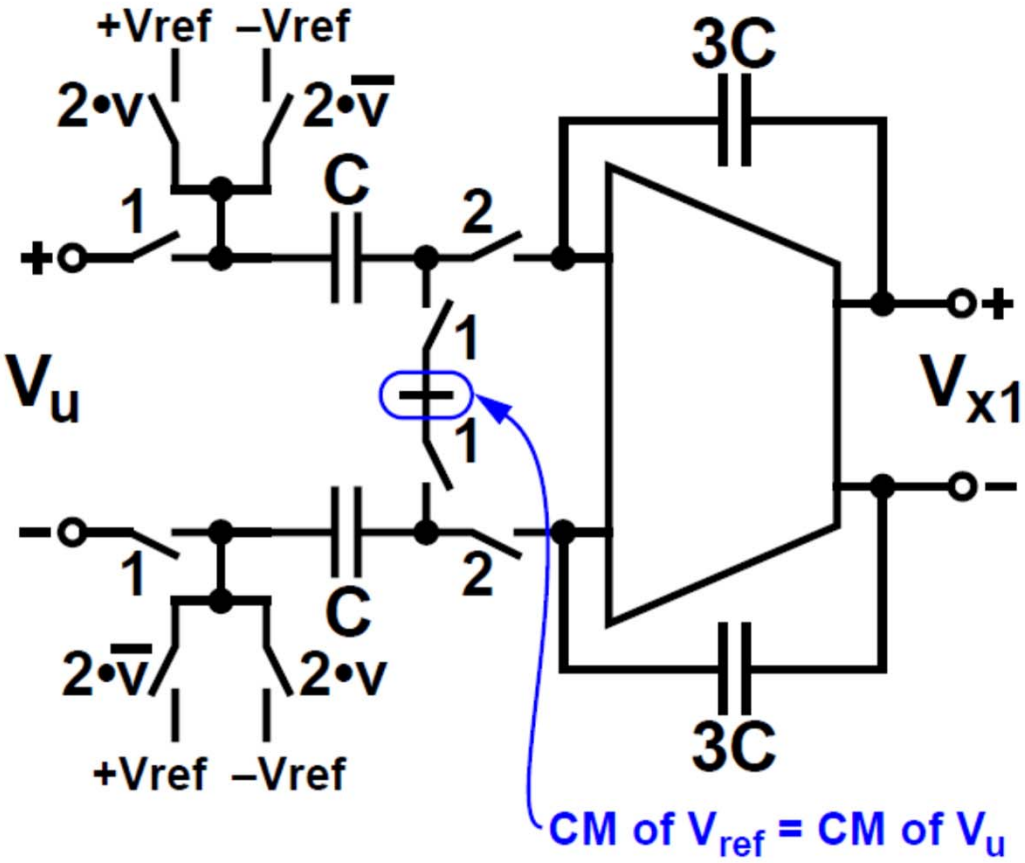
- **Take $\|x_1\|_\infty = 3$ and $\|x_2\|_\infty = 9$**
  - **The first integrator should not saturate**
  - **The second integrator will not saturate for dc inputs up to -3 dBFS and possibly as high as -1 dBFS**

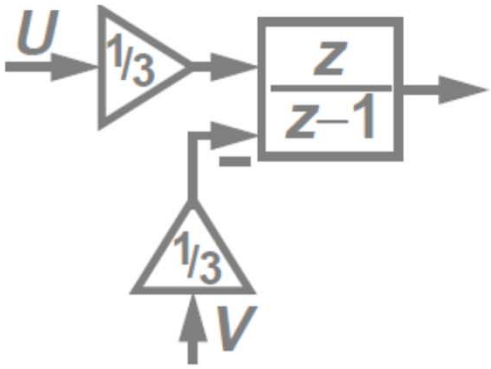
- **Our scaled version of MOD2 is**



First Integrator (INT1)

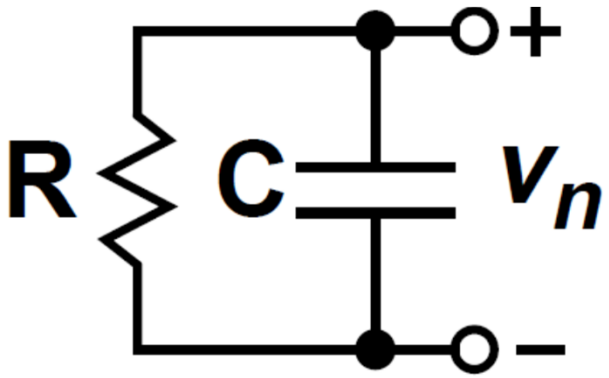
- **Shared Input/Reference Caps**





- **How do we determine C?**

kT/C Noise



- **Regardless of the value of R, the mean-square value of the voltage on C is**

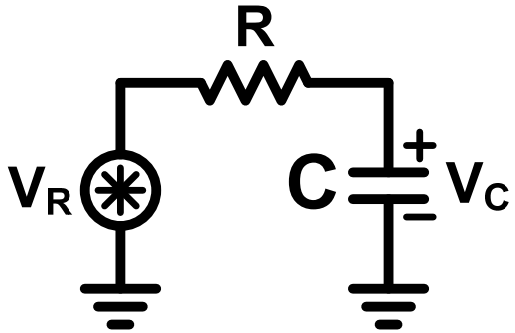
$$\overline{v_n^2} = \frac{kT}{C}$$

where *k* = 1.38 x 10^{-23} J/K is *Boltzmann's constant* and *T* is the temperature in Kelvin

The mean square noise charge is $\overline{q_n^2} = C^2\overline{v_n^2} = kTC$

Derivation of kT/C Noise

- **Noise in RC switch network**



Noise PSD from R: $S_R(f) = 4kTR$

Time constant of R-C filter: $\tau = RC$

Noise voltage across C:

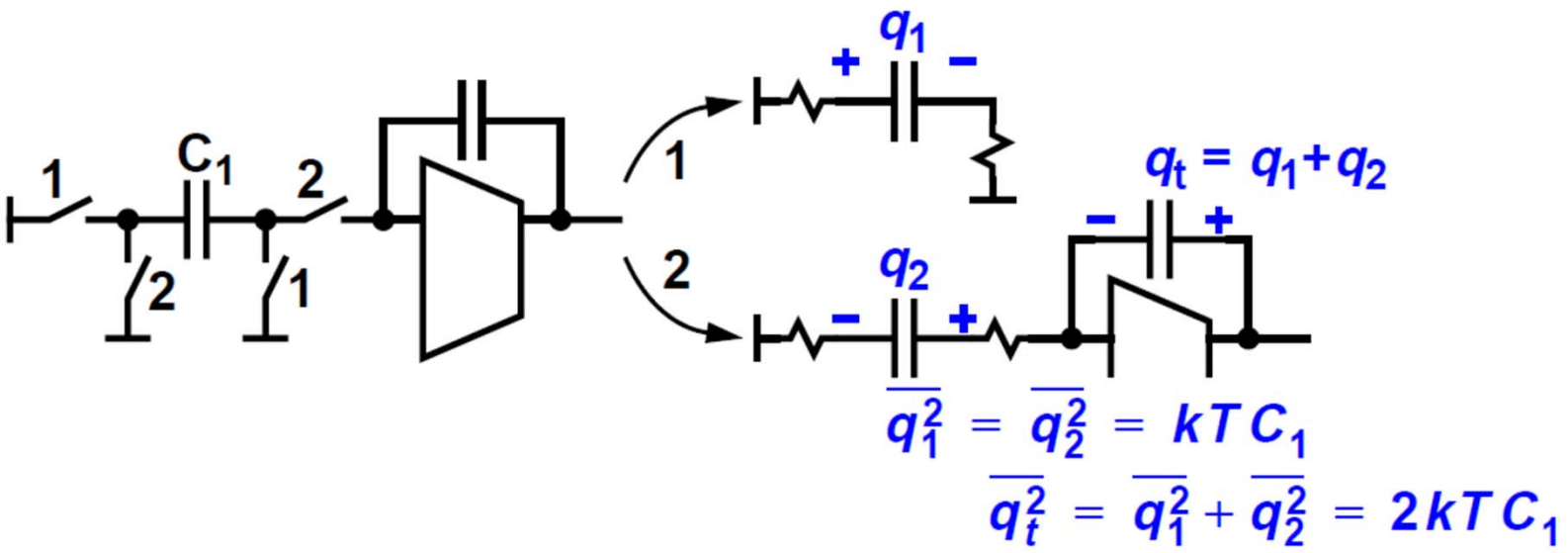
$$\overline{V_C^2} = \int_0^\infty S_R(f) \left| \frac{1}{1+s\tau} \right|^2 df$$

$$= 4kTR \int_0^\infty \left| \frac{1}{1+s\tau} \right|^2 df$$

$$= \frac{4kTR}{4\tau} = \frac{kT}{C}$$

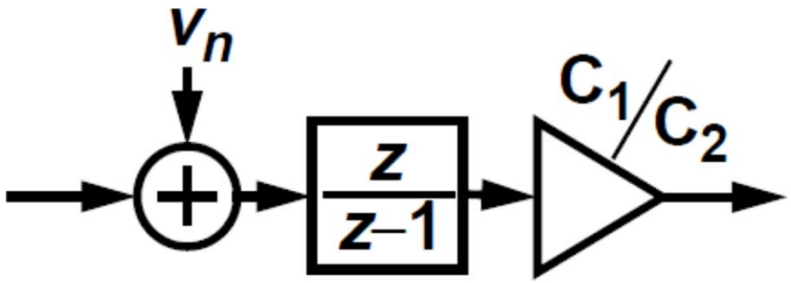
Implications for a SC Integrator

- **Each charge/discharge operation has a random component**
  - **The amplifier plays a role during phase 2, but we'll assume the noise in both phases is kT/C (we will revisit this in 'Noise in SC Circuits' Lecture)**
- **For a given cap these random components are essentially uncorrelated so the noise is white**



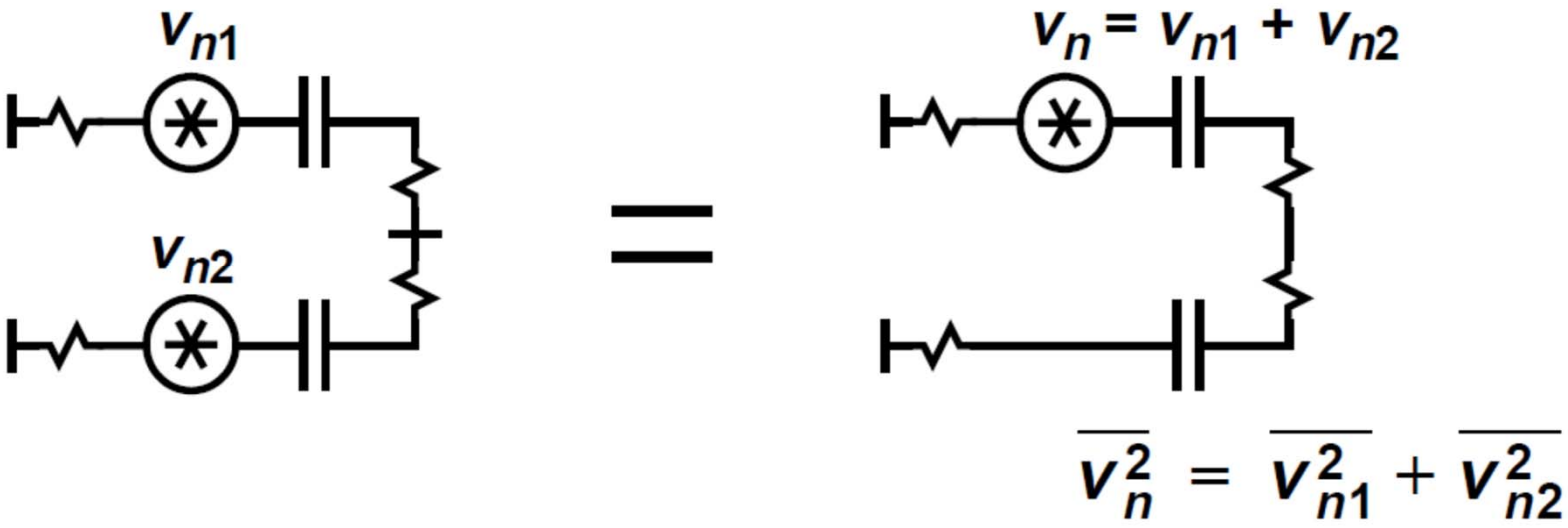
Implications for a SC Integrator

- The noise charge is equivalent to a noise voltage with mean square value $\overline{v_n^2} = 2kT/C_1$ added to the input of the integrator



- This noise power is spread uniformly over all frequencies from 0 to $f_S/2$
- The power in the band from 0 to f_B is v_n^2/OSR

Differential Noise



- Twice as many switched caps
  → twice as much noise power
- The input-referred noise power in our differential integrator is

$$\overline{v_n^2} = 4kT/C_1$$

INT1 Absolute Capacitor Sizes

- **For SNR = 100 dB @ -3 dBFS input**

  The signal power is

$$\overline{v_s^2} = \frac{1}{2} \cdot \frac{(1\,V)^2}{2} = 0.25\,V^2$$

-3 dBFS

$A^2/2$

  Therefore we want $\overline{v_{n,\text{inband}}^2} = 0.25 \times 10^{-10}\,V^2$

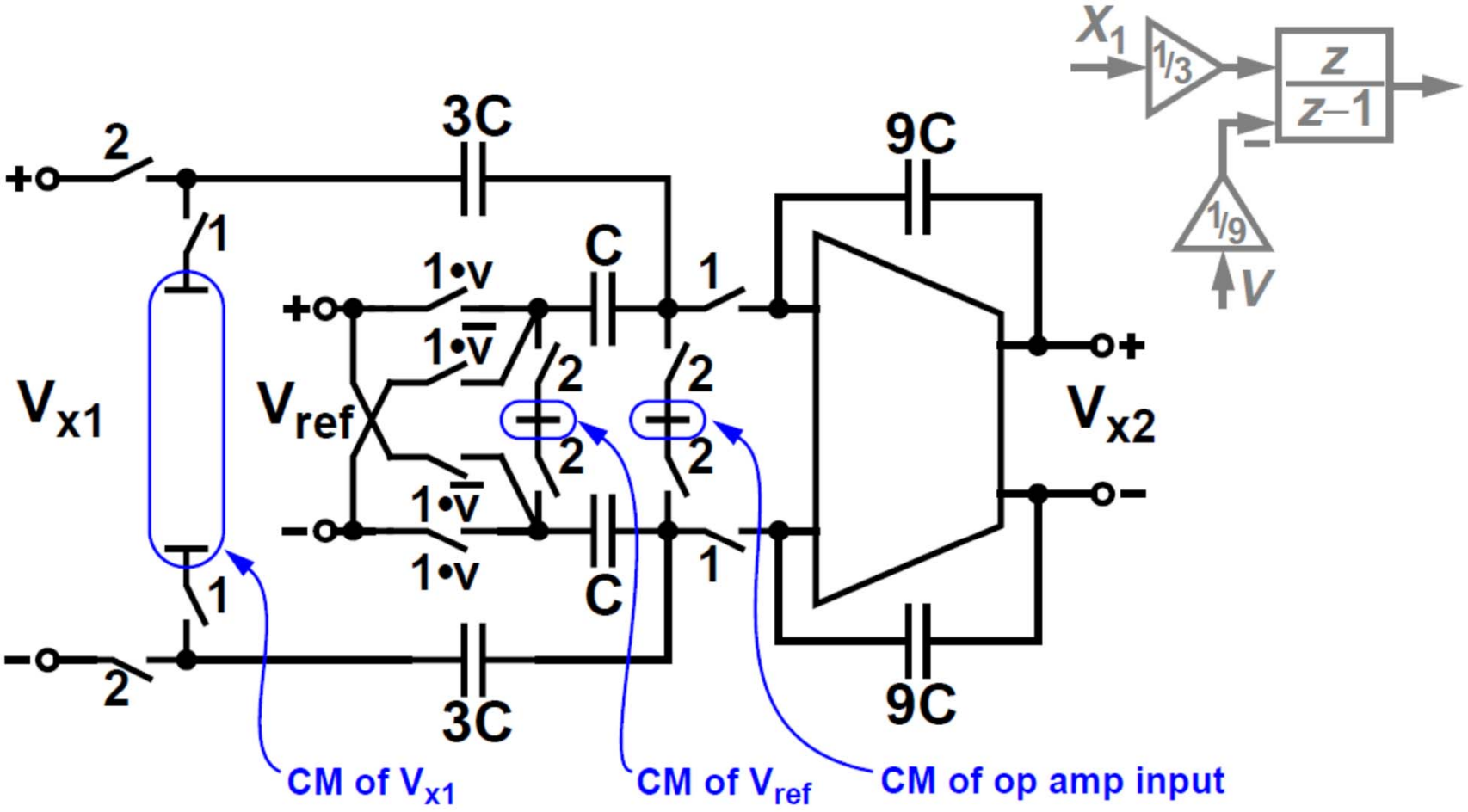
  Since $\overline{v_{n,\text{inband}}^2} = \overline{v_n^2}/OSR$

$$C_1 = \frac{4kT}{\overline{v_n^2}} = 1.33\ \text{pF}$$

- **If we want 10 dB more SNR, we need 10x caps**

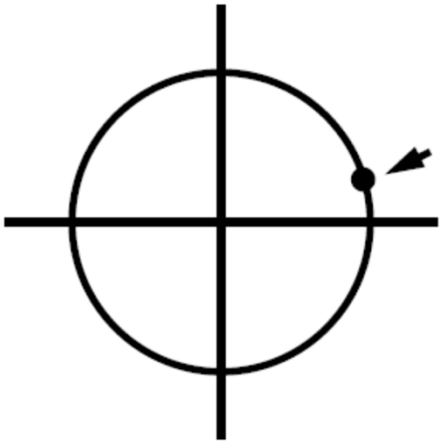
Second Integrator (INT2)

- **Separate Input and Feedback Caps**



INT2 Absolute Capacitor Sizes

- **In-band noise of second integrator is greatly attenuated**



$$\omega_B = \frac{\pi}{OSR}$$

$$\text{INT1 gain @ pb edge: } A = \frac{1/3}{\omega_B} = \frac{OSR}{3\pi}$$

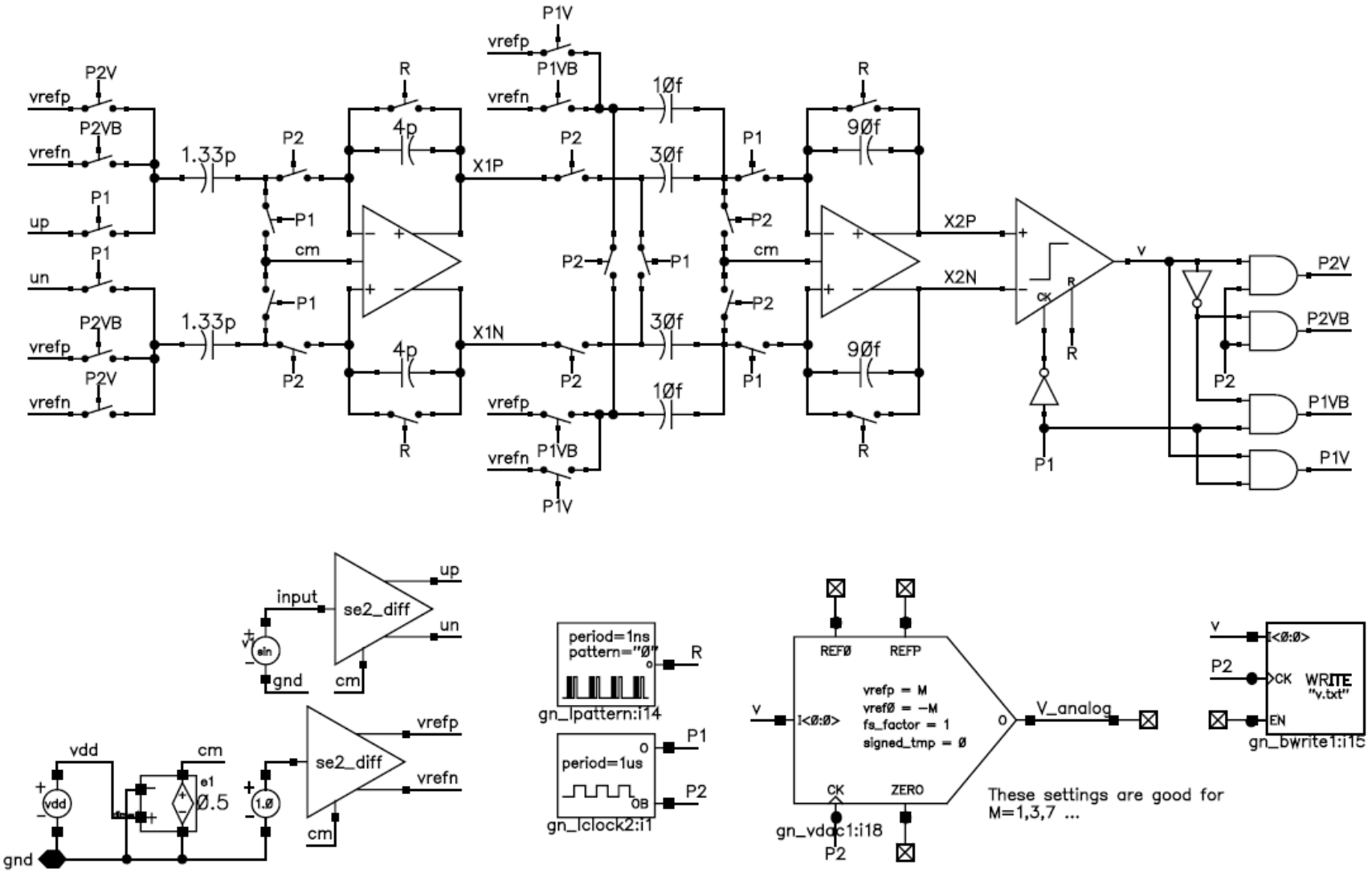
$$\text{INT2 noise attenuation: } > OSR \cdot A^2 \approx 10^6$$

→**Capacitor sizes not dictated by thermal noise**

- **Charge injection errors and desired ratio accuracy set absolute size**

  A reasonable size for a small cap is ~10 fF

Behavioral Schematic



Verification

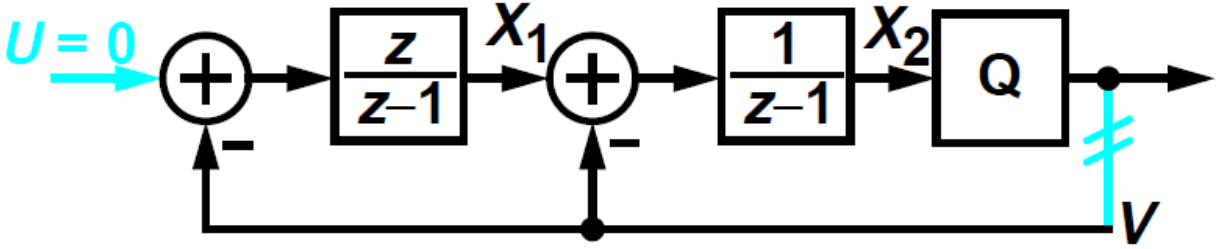
- **Open-loop verification**
  1) **Loop filter**
  2) **Comparator**

  Since MOD2 is a 1-bit system, all that can go wrong is the polarity and the timing

  Usually the timing is checked by (1) so this verification check is not needed
- **Closed-loop verification**
  3) **Swing of internal states**
  4) **Spectrum: SQNR, STF gain**
  5) **Sensitivity, start-up, overload recovery, …**

Loop-Filter Check

- Open the feedback loop, set $u = 0$ and drive an impulse through the feedback path



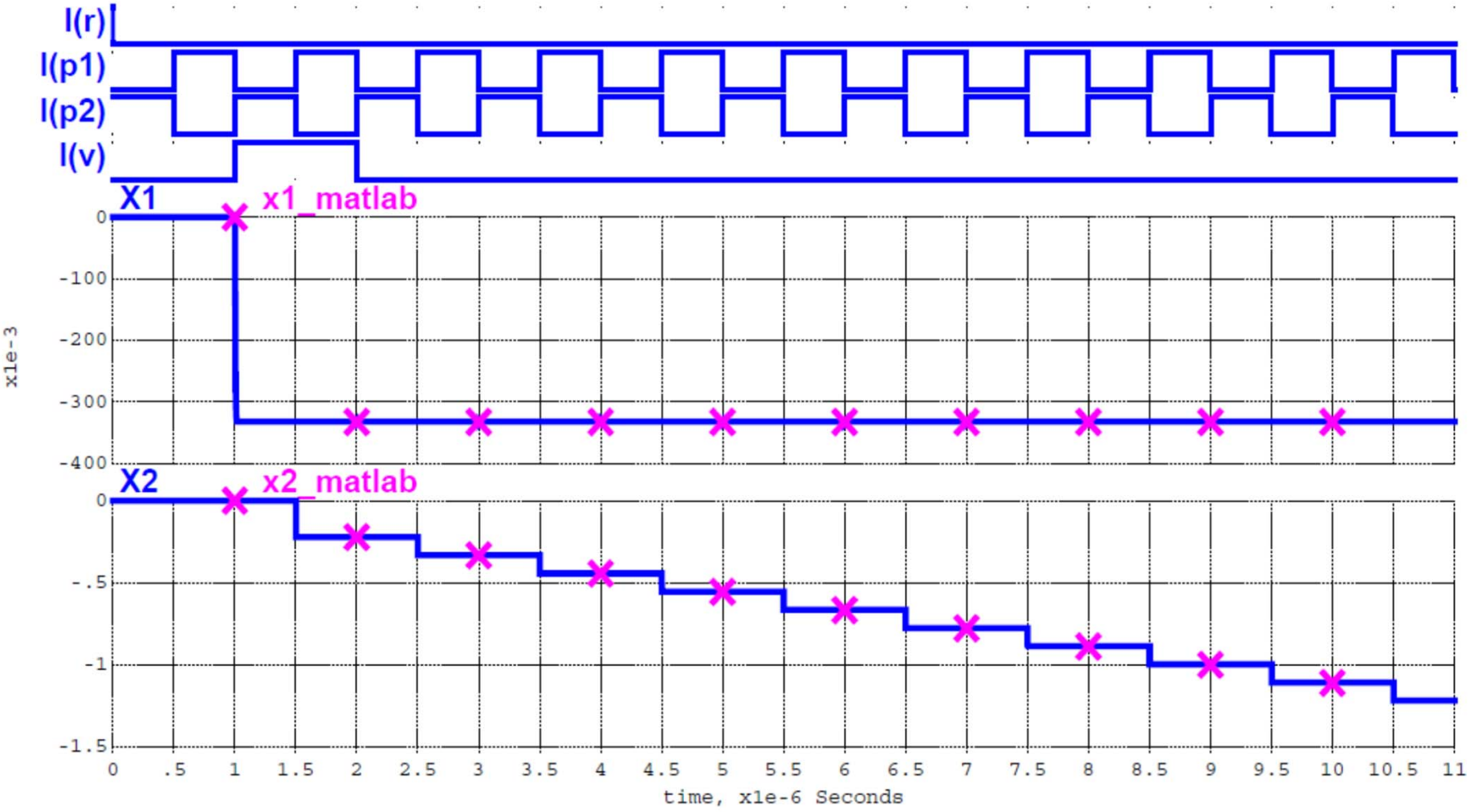
$$X_2 = \frac{-1}{z-1}\left(1 + \frac{z}{z-1}\right)V$$

$$\therefore v(n) = \{1, 0, 0, \ldots\} \Rightarrow x_2(n) = \{-2, -3, -4, \ldots\}$$

- If x_2 is as predicted then the loop filter is correct

  At least for the feedback signal, which implies that the NTF will be as designed

Loop-Filter Check



Impulse Response

- An impulse is {1,0,0,…}, but a binary DAC can only output +/- 1 and cannot produce a 0

Q. How can we determine the impulse response of the loop filter through simulation?

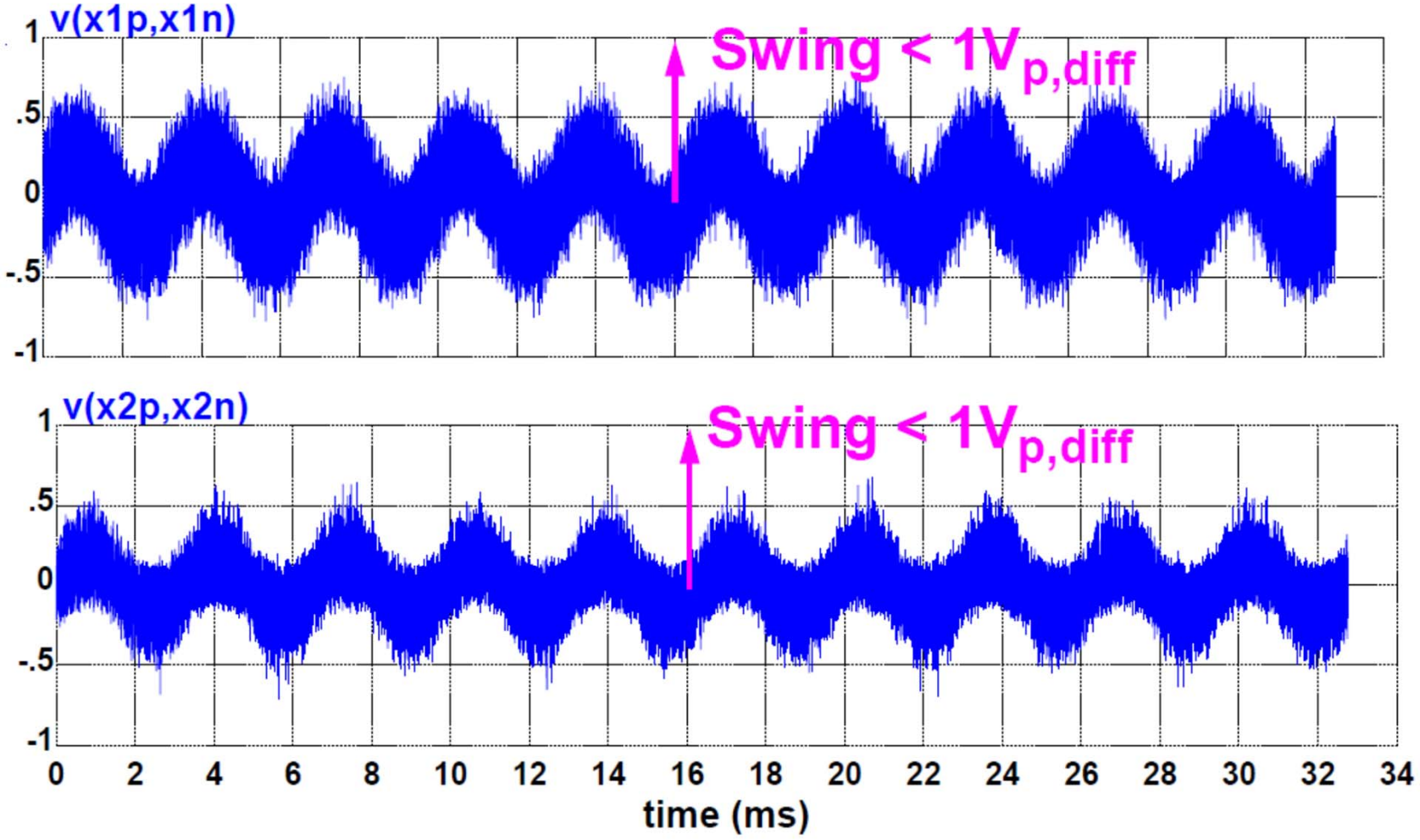
A. Do two simulations: one with v = {-1,-1,-1,…} and one with v = {+1,-1,-1,…}, take the difference, divide by 2

With superposition the difference is v = {2,0,0,…} and the result is divided by 2

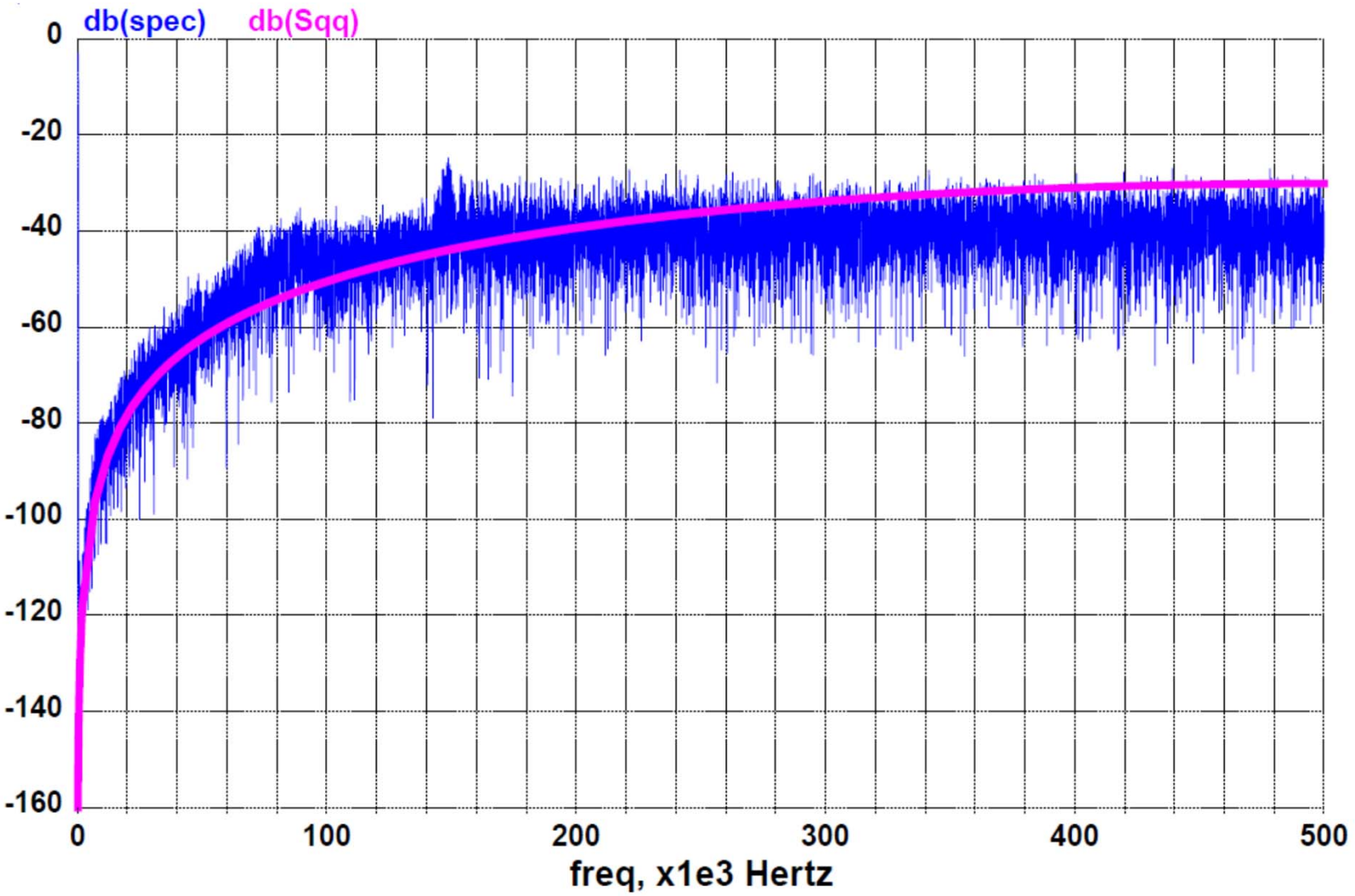
To keep the integrator states from growing too quickly, you could also use v = {-1,-1,+1,-1,…} and then v = {+1,-1,+1,-1,…}

Simulated State Swings

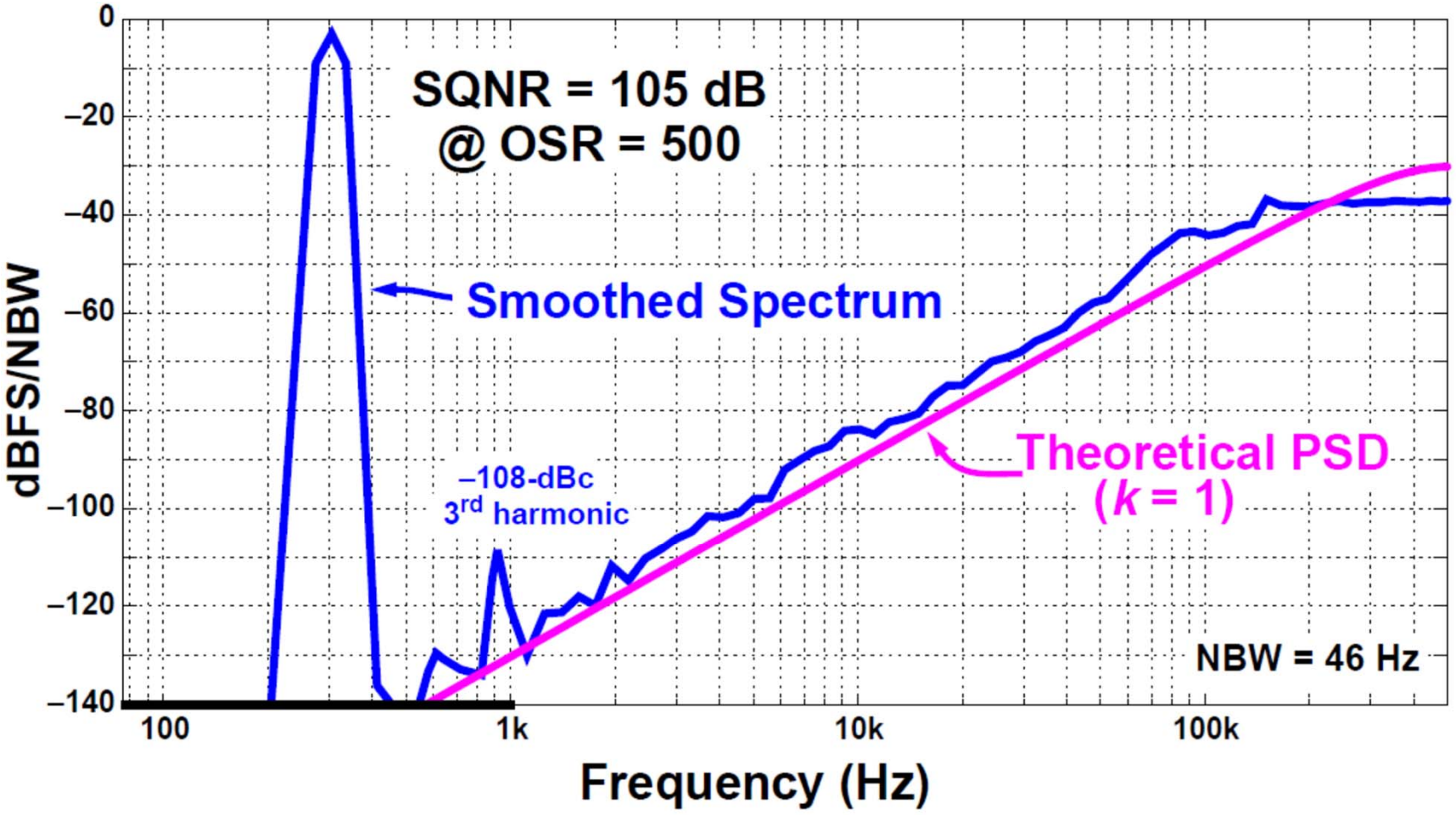
- -3 dBFS, ~300 Hz sine wave



Unclear Spectrum



Better Spectrum



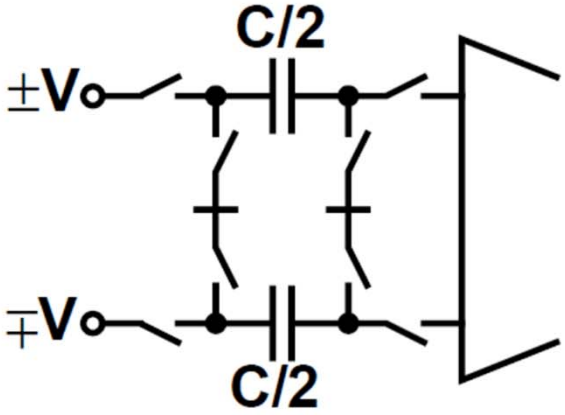
- **SQNR dominated by -108 dBFS 3rd harmonic**

Implementation Summary

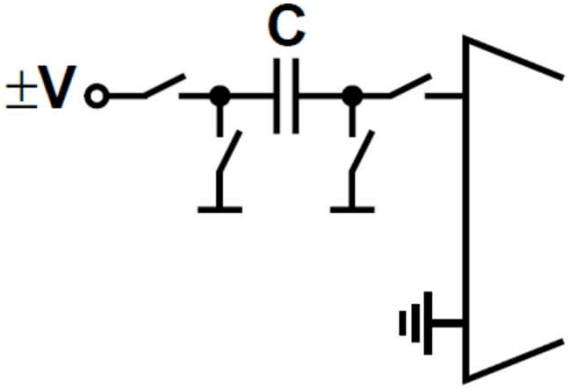
1) Choose a viable SC topology and manually verify timing
2) Dynamic Range scaling
   - You now have a set of capacitor ratios
   - Verify operation: loop filter, timing, swing, spectrum
3) Determine absolute capacitor sizes
   - Verify noise
4) Determine op-amp specs and construct a transistor-level schematic
   - Verify everything
5) Layout, fab, debug, document…

Differential vs Single-Ended

- **Differential is more complicated and has more caps and more noise → single-ended is better?**



$$SNR = \frac{(2V)^2/2}{4kT/(C/2)} = \frac{CV^2}{4kT}$$



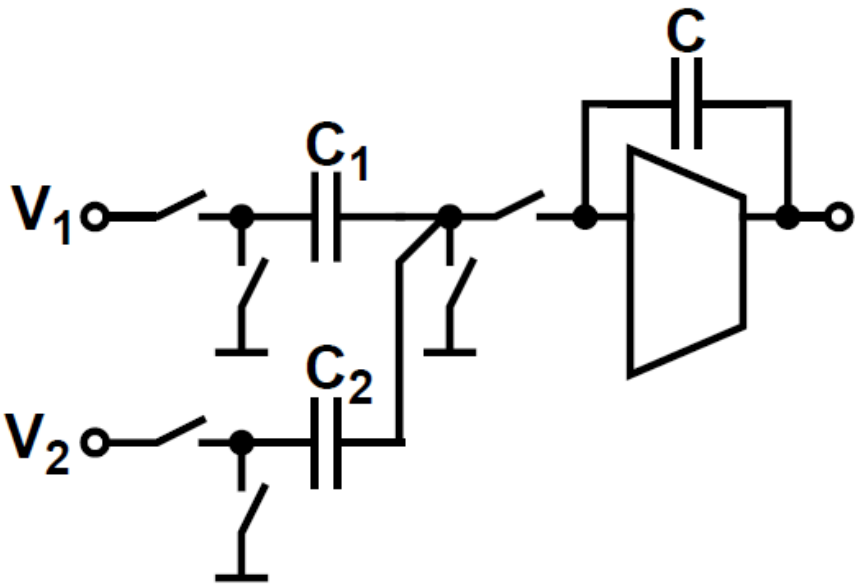
$$SNR = \frac{V^2/2}{2kT/C} = \frac{CV^2}{4kT}$$

- **Same capacitor area → same SNR**

  Differential is generally preferred due to rejection of even-order distortion and common-mode noise/interference.

Shared vs Separate Input Caps

- **Separate caps → more noise**



V_1 input: $\overline{v_{n1}^2} = 2kT/C_1$

V_2 input: $\overline{v_{n2}^2} = 2kT/C_2$

V_2 gain / V_1 gain: C_2/C_1

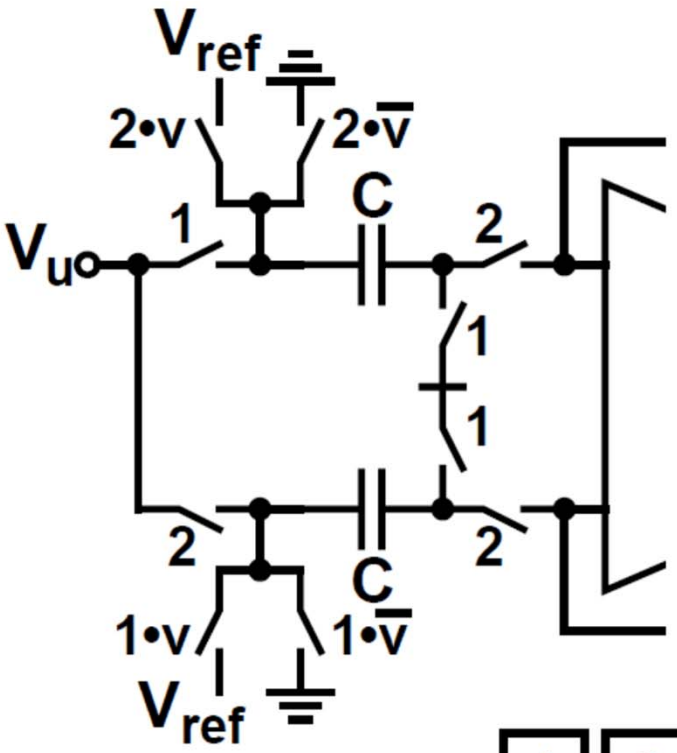
v_{n2} referred to V_1: $v_{n2}C_2/C_1$

Total noise referred to V_1: $(2kT/C_1)(1 + C_2/C_1)$

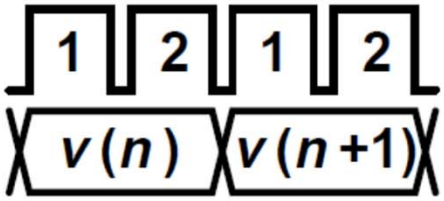
- **Using separate caps allows input CM and ref CM to be different and is often preferred**
  - **Also improves linearity as reference feeds into separate node and won't introduce signal dependent error**

Single-Ended Input

- **Shared Caps**



Full-scale range of V_u is $[0, V_{ref}]$.



What You Learned Today

- MOD2 implementation
- Switched-capacitor integrator
  - Switched-cap summer & DAC too
- Dynamic-range scaling
- kT/C noise
- Verification strategy