Lecture 6
Example Design 2

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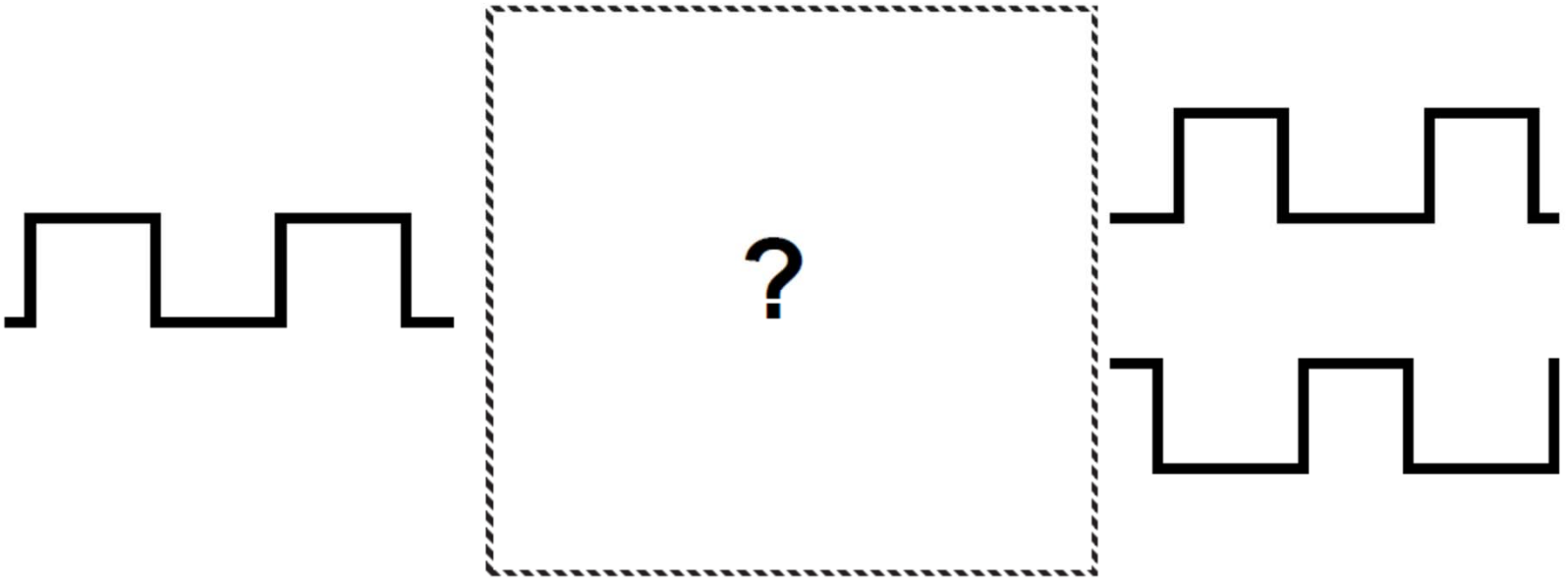
Lecture Plan

Date	Lecture (Wednesday 2-4pm)		Reference	Homework
2020-01-07	1	MOD1 & MOD2	PST 2, 3, A	1: Matlab MOD1&2
2020-01-14	2	MOD*N* + ΔΣ Toolbox	PST 4, B	2: ΔΣ Toolbox
2020-01-21	3	SC Circuits	R 12, CCJM 14	
2020-01-28	4	Comparator & Flash ADC	CCJM 10	3: Comparator
2020-02-04	5	Example Design 1	PST 7, CCJM 14	
2020-02-11	6	Example Design 2	CCJM 18	4: SC MOD2
2020-02-18	Reading Week / ISSCC			
2020-02-25	7	Amplifier Design 1		Project
2020-03-03	8	Amplifier Design 2		
2020-03-10	9	Noise in SC Circuits		
2020-03-17	10	Nyquist-Rate ADCs	CCJM 15, 17	
2020-03-24	11	Mismatch & MM-Shaping	PST 6	
2020-03-31	12	Continuous-Time ΔΣ	PST 8	
2020-04-07	Exam			
2020-04-21	Project Presentation (Project Report Due at start of class)			

Circuit of the Day: Non-Overlap Clock Gen

- **Our switched-capacitor circuits require two non-overlapping clocks. How do we generate them?**

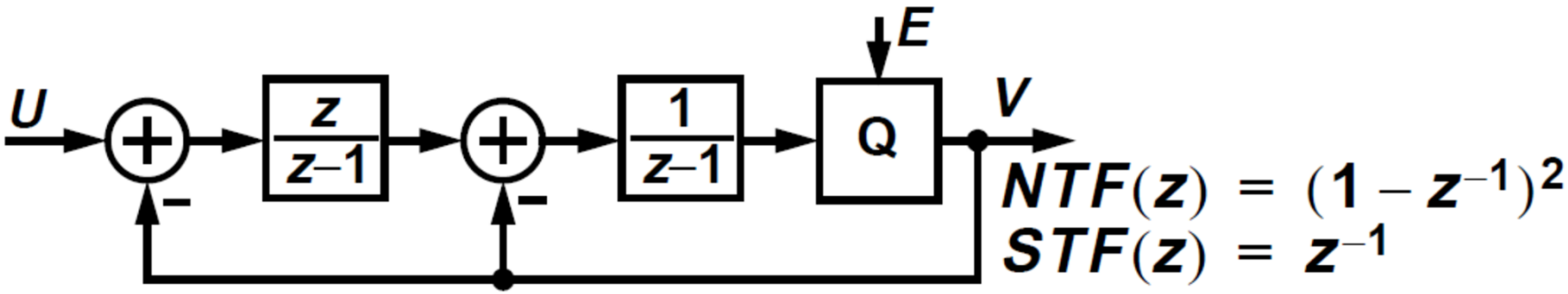


What you will learn…

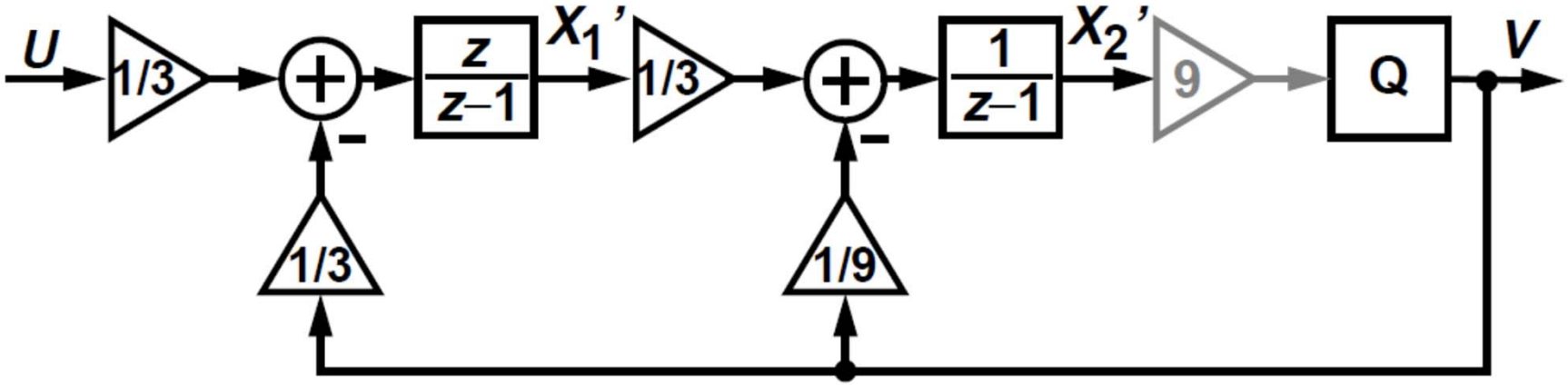
- **Transistor-level implementation of MOD2**
  - **Op-amp, SC CMFB, comparator, clock generator**
- **MOD2 variants**
- **Variable quantizer gain**

Review: MOD2

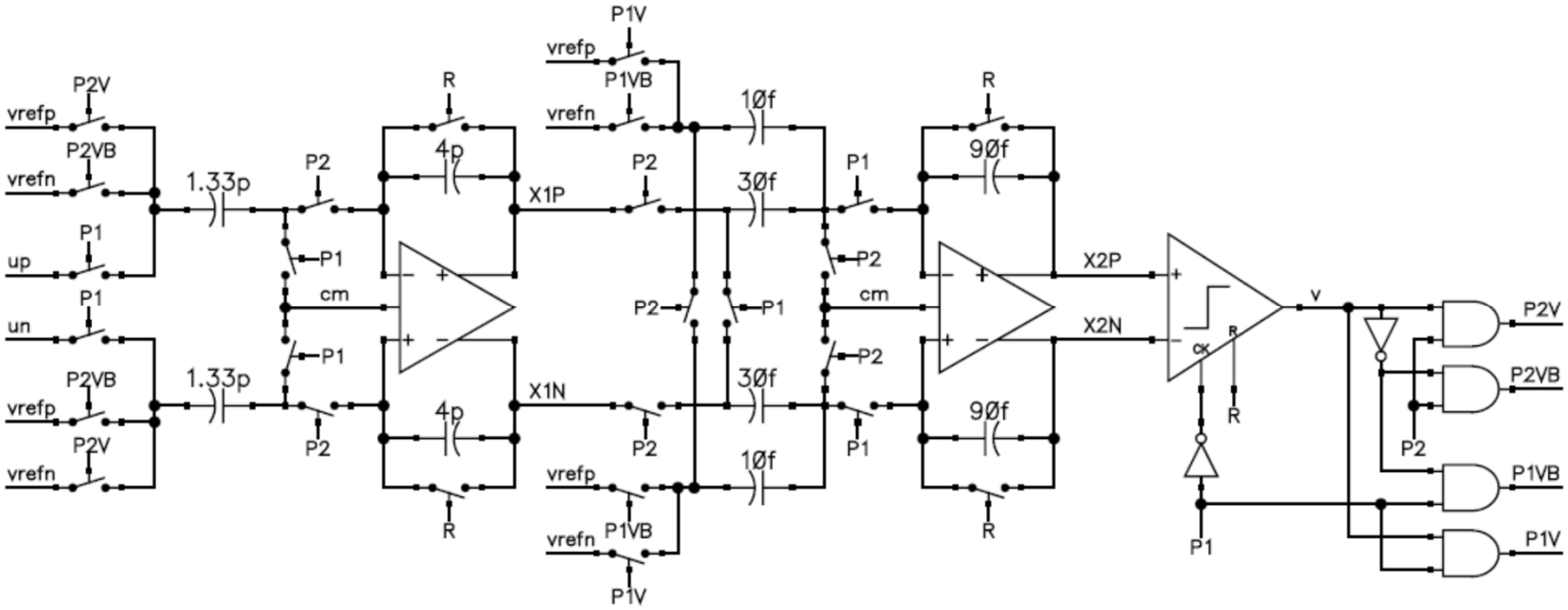
- **Standard Block Diagram**



- **Scaled Block Diagram**



Review: Schematic

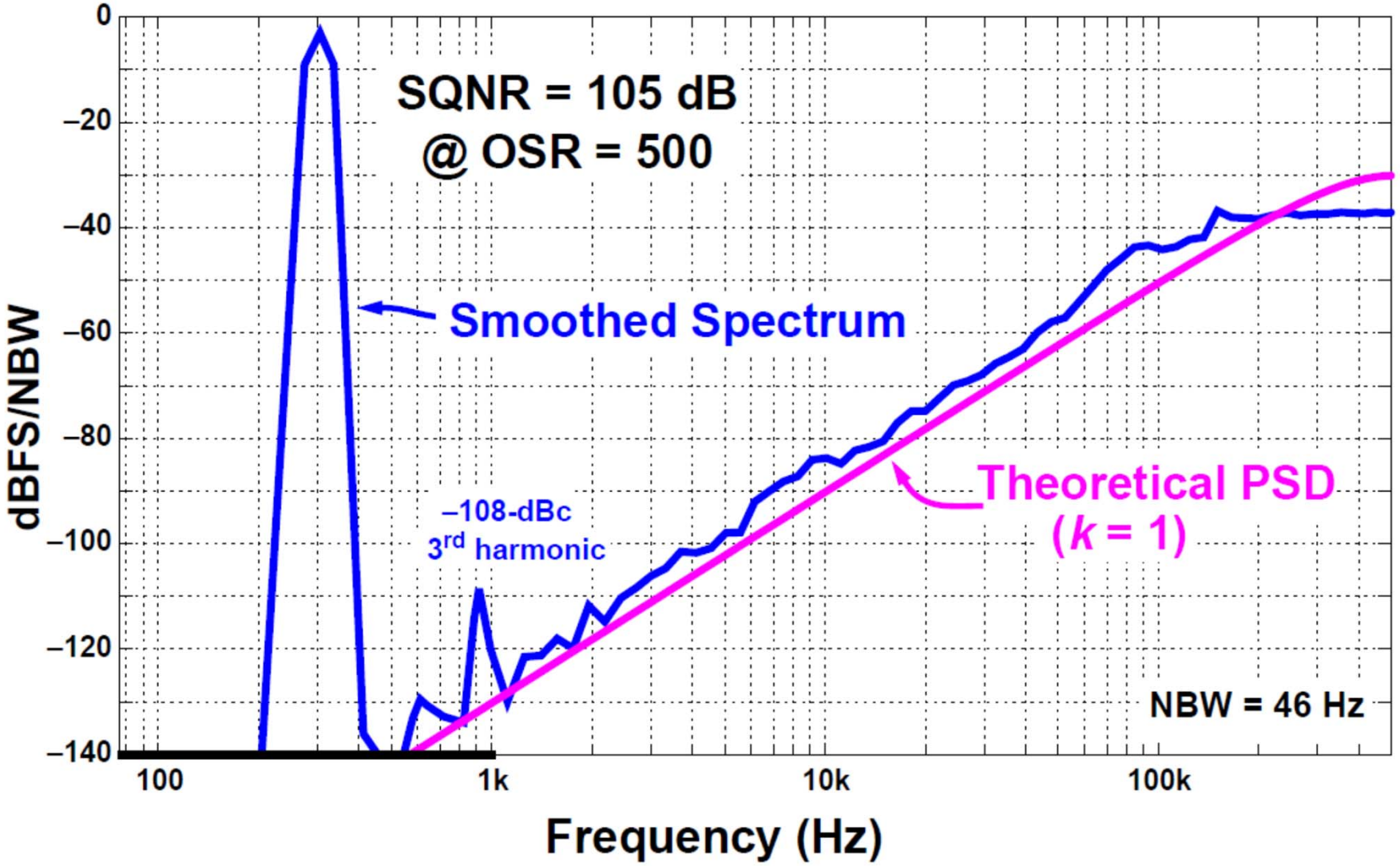


- **1st-stage capacitor sizes set for SNR = 100 dB @ OSR = 500 and -3 dBFS input**

  V_{ref} = +/- 1V and the full-scale input range is +/- 1V

- **2nd-stage capacitor sizes set by minimum allowable capacitance**

Review: Simulated Spectrum



Review: Implementation Summary

✔ 1) **Choose a viable SC topology and manually verify timing**

✔ 2) **Do dynamic-range scaling**

- **You now have a set of capacitor ratios**
- **Verify operation: loop filter, timing, swing, spectrum**

✔ 3) **Determine absolute capacitor sizes**

- **Verify noise**

→ 4) **Determine op-amp specs and construct a transistor-level schematic**

- **Verify everything**

5) **Layout, fab, debug, document …**

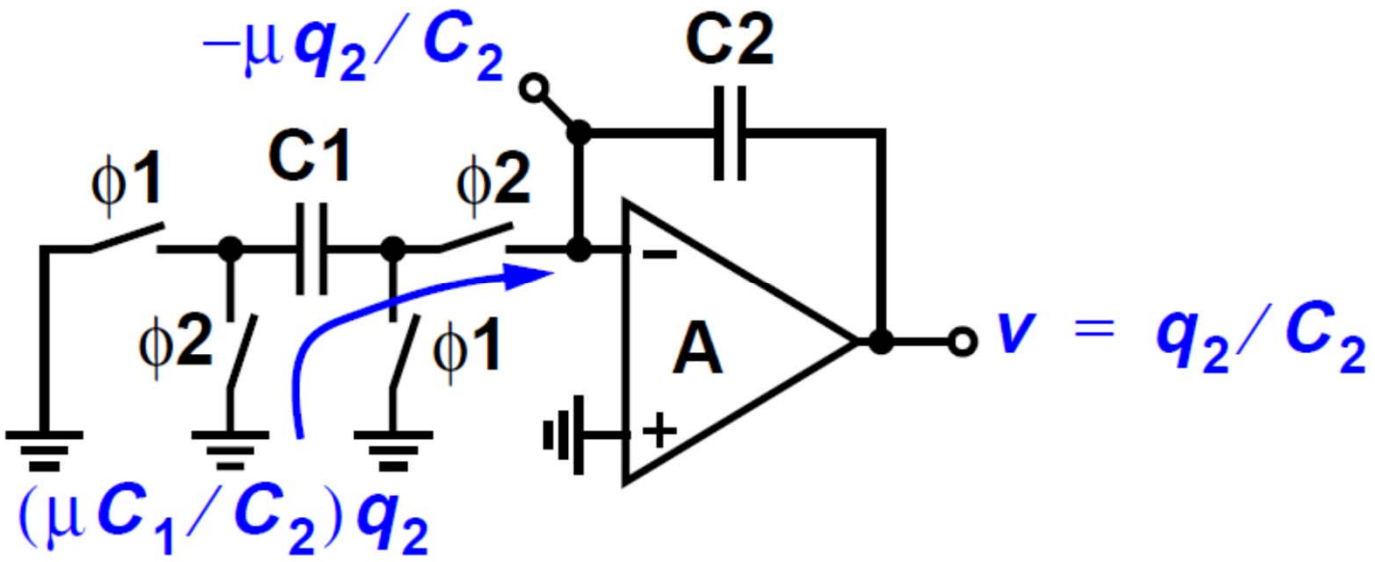
Effect of Finite Op Amp Gain

- **Linear Theory**

  Suppose the amplifier has finite DC gain *A*

  Define $\mu = 1/A$

  To determine the effect on the integrator pole, look at the SC integrator with zero input



Effect of Finite Op Amp Gain

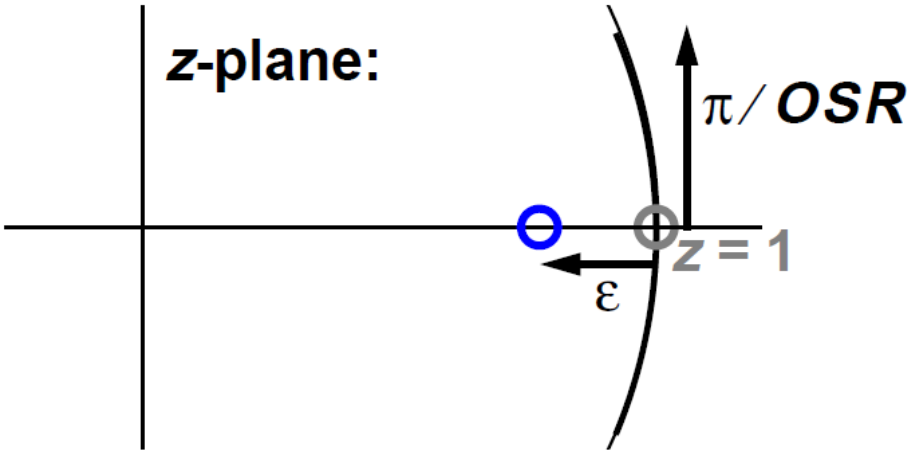
- A fraction of q_2 leaks away each clock cycle

$$q_2(n+1) = (1-\varepsilon)q_2(n) \text{ where } \varepsilon = \mu C_1/C_2$$

- The integrator is lossy with a pole at $z = 1 - \varepsilon$

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1/C_2}{z-(1-\varepsilon)}$$

- Error ε becomes significant once it approaches $\varepsilon \approx \pi/OSR$



Op Amp Gain Requirement

- According to linear theory, finite op amp gain should not degrade the noise significantly as long as

$$A > (C_1/C_2)(OSR/\pi)$$

- For our implementation of MOD2, where $C_1/C_2 = 1/3$ and $OSR = 500$, this leads to

$$A > 50 = 34\text{dB}$$

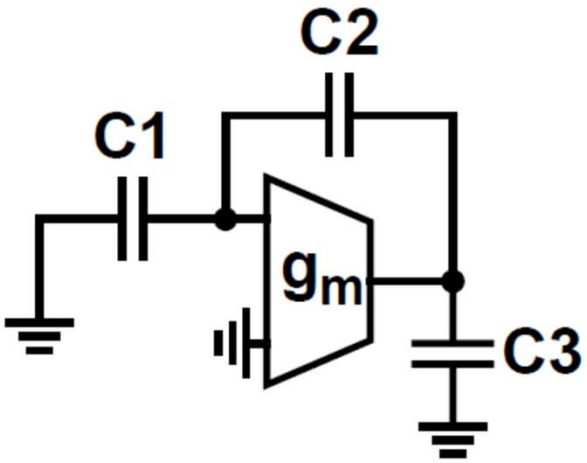
- As OSR decreases, gain requirement goes down

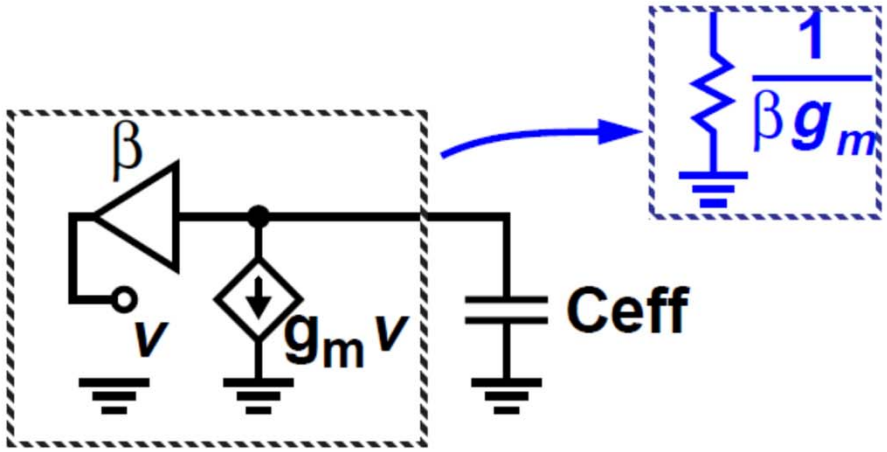
  This does not account for non-linearities that decrease with higher DC gain

Op Amp Transconductance

- **Settling Time**

  Model the op amp as a simple g_m





$$\beta = C_2/(C_1 + C_2)$$

$$C_{eff} = C_3 + C_1C_2/(C_1 + C_2)$$

- **This is a single time constant circuit with**

$$\tau = C_{eff}/(\beta g_m)$$

Settling Requirements

- If g_m is linear, incomplete settling has the same effect as a coefficient error and thus g_m can be very low
- In practice, the g_m is not linear and we need to ensure nearly complete settling
- As a worst case scenario, let's require transients to settle to 1 part in 10^5

  This should be more than enough for -100dBc distortion

Settling Requirements

- If linear settling is allocated 1/4 of a clock period

$$e^{-\frac{T/4}{\tau}} = 10^{-5} \rightarrow \tau = \frac{T}{4\ln 10^5} = 20\text{ns}$$

$$g_m = \frac{C_{eff}}{\beta\tau} = \frac{C_{eff}}{\beta} 4 f_s \ln 10^5$$

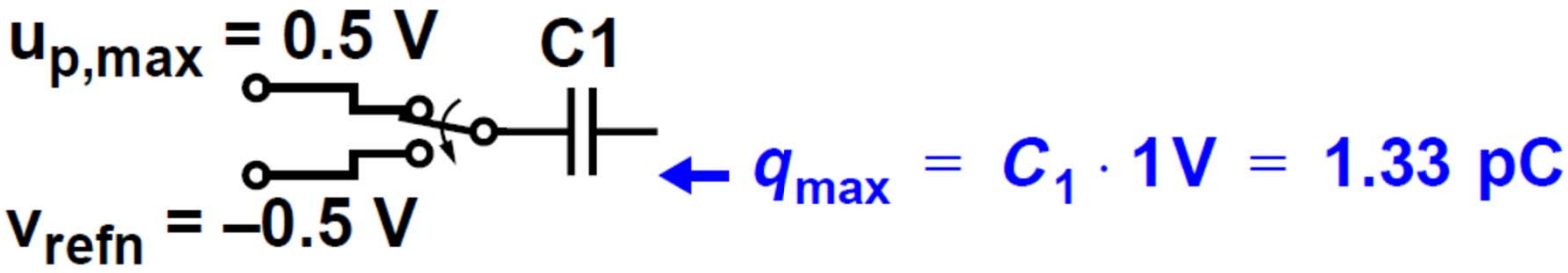
- For INT1 of our MOD2

$$C_{eff} = \left(\frac{4\text{p} \cdot 1.33\text{p}}{4\text{p} + 1.33\text{p}} + 30\text{f} \right) = 1.0\text{pF}$$

- For $\beta = 3/4$, $f_s = 1\text{MHz}$ → $g_m = 61\mu\text{A/V}$

Slewing

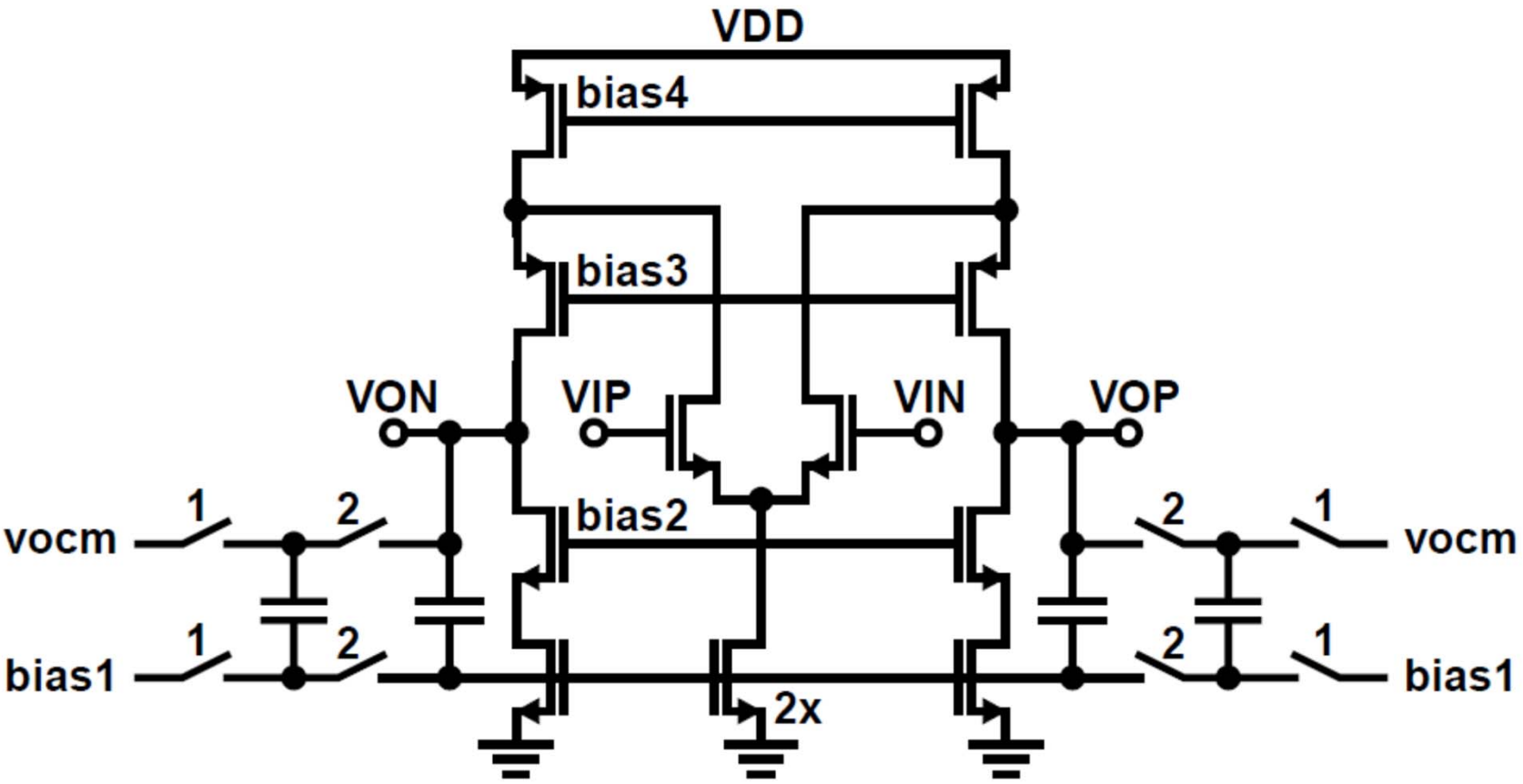
- **The maximum charge transferred through C1 is**



- **If we require the slew current to be enough to transfer q_{max} in 1/4 of a clock period, then**

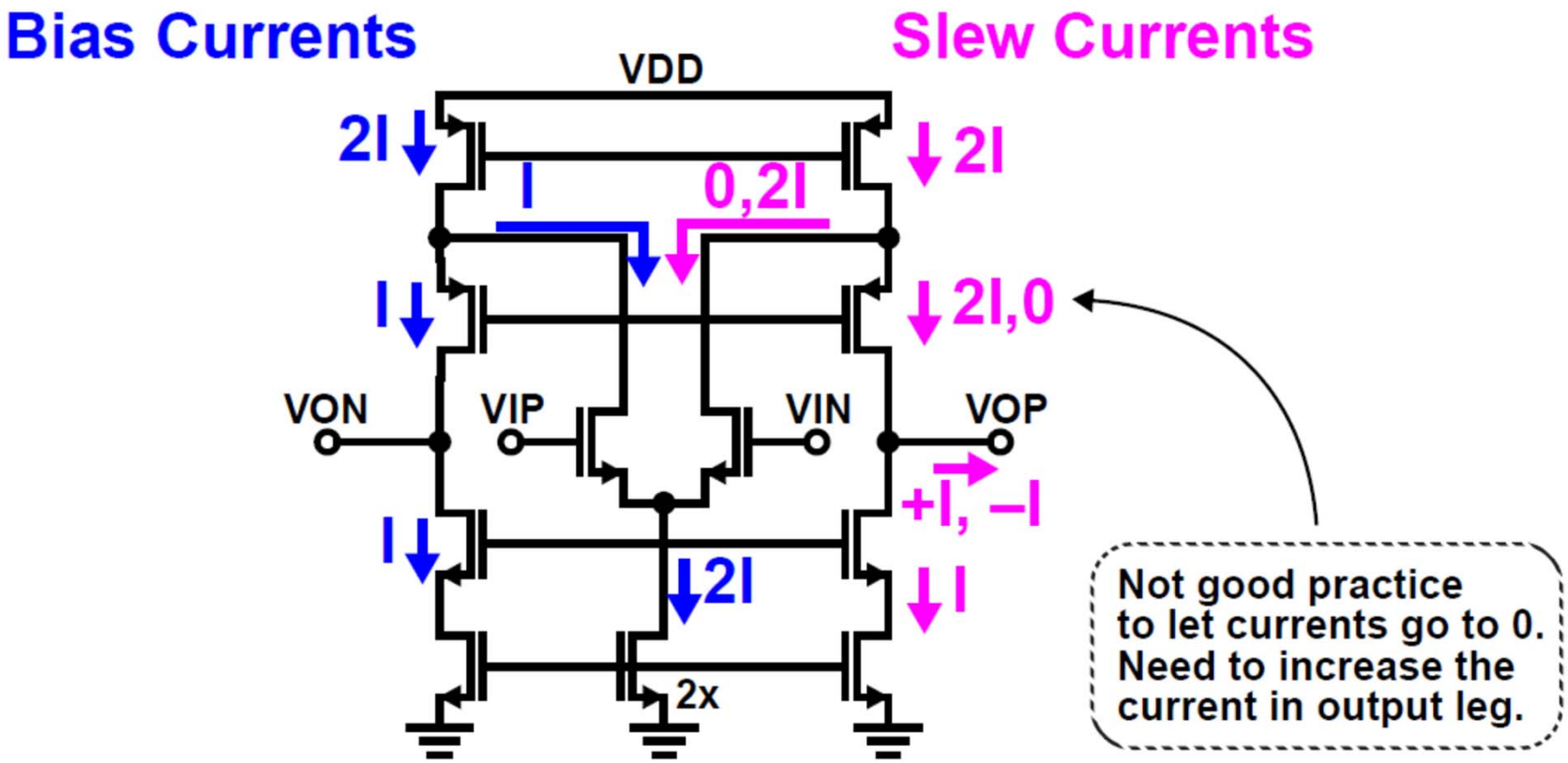
$$I_{slew} = \frac{q_{max}}{T/4} \approx 5\mu A$$

Op-Amp Design



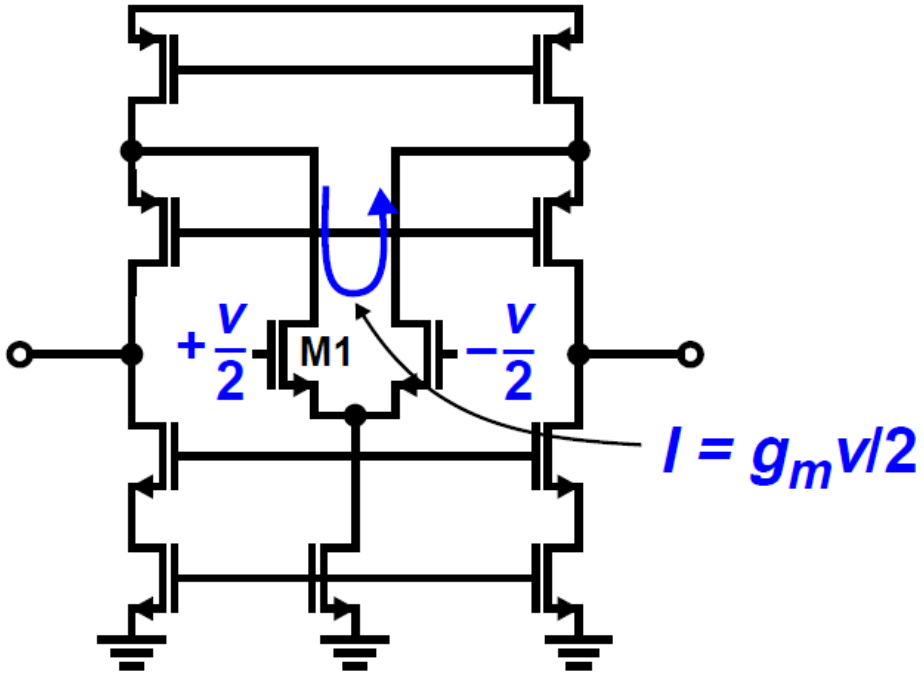
- **Folded-cascode op-amp with switched-capacitor common-mode feedback**

Op-Amp Design: Bias Current



- **Slew constraint dictates I > 5uA**

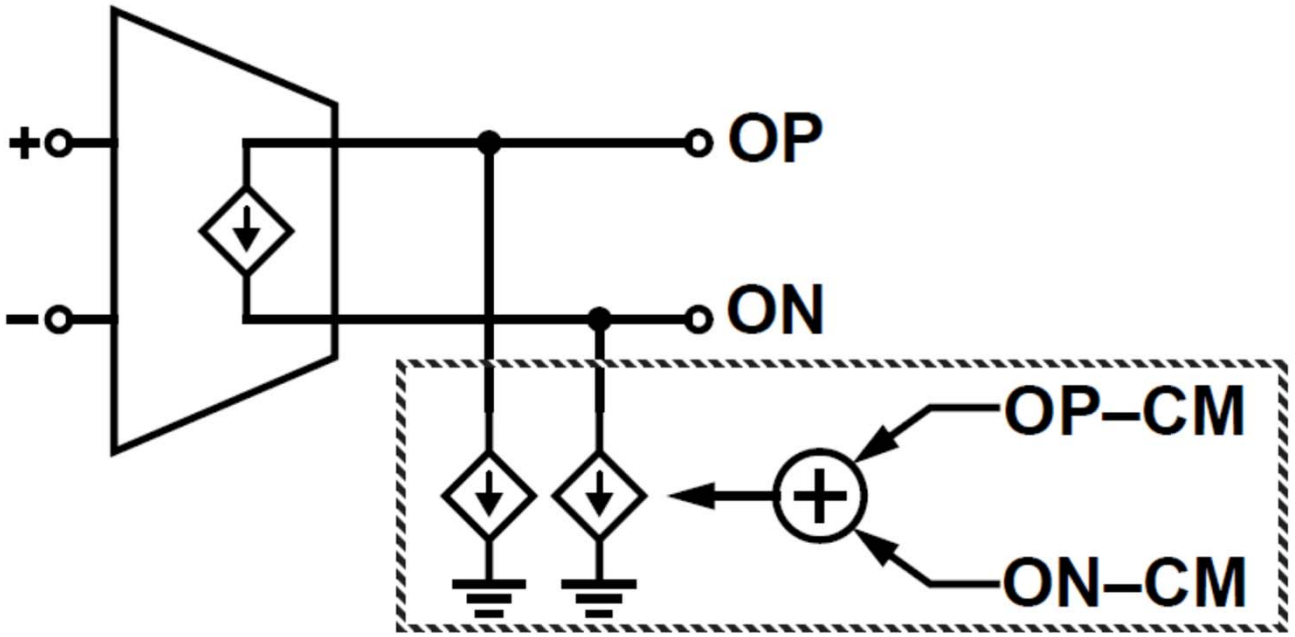
Op-Amp Design: g_m



- **Square-law MOSFET model: $g_m = 2I_D/\Delta V$**
- **$I_D = 5\mu A$, $g_m \geq 60\mu A/V$ → $\Delta V \leq 167mV$**

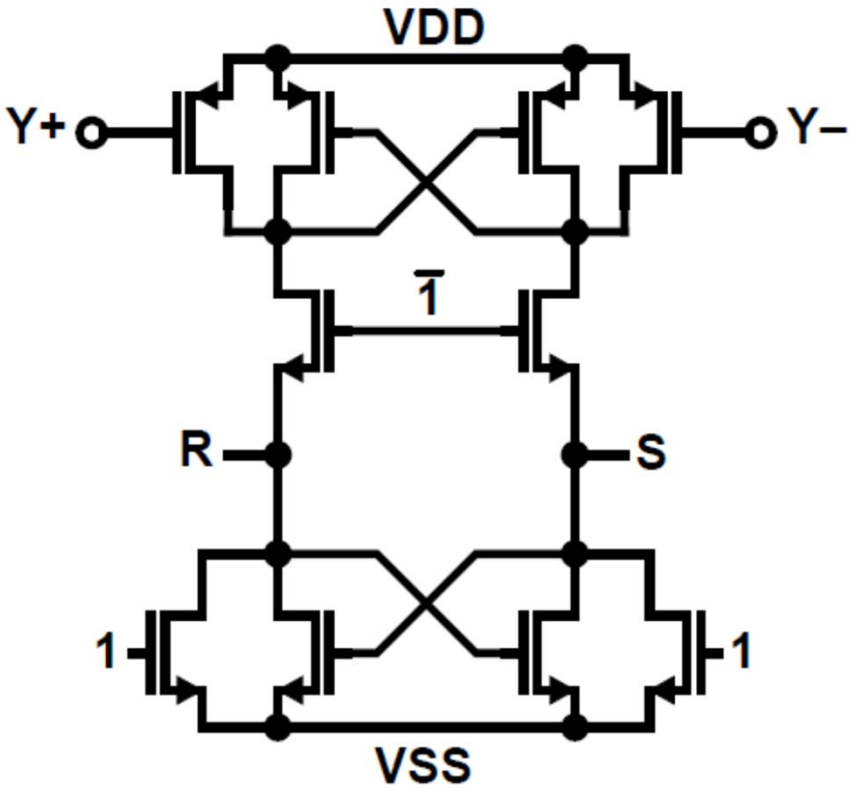
  Usually $\Delta V \approx 100 - 200mV$, so we should be able to get high enough g_m

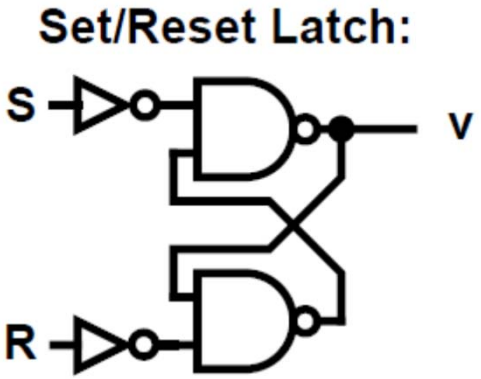
Ideal Common-Mode Feedback



- **Can use this circuit to speed up the simulation**

Latched Comparator

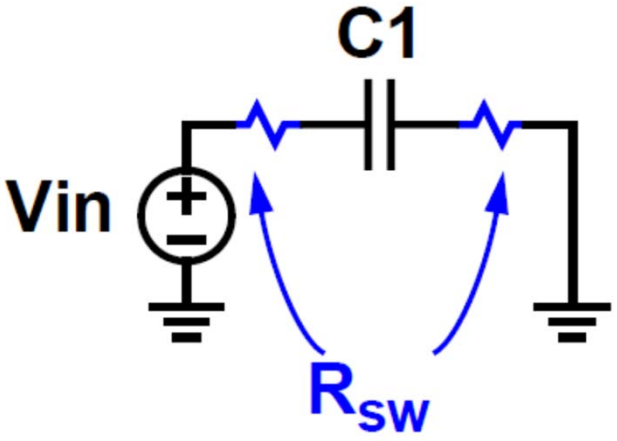




- **Falling phase 1 initiates regenerative action**
  - **S and R connected to a Set/Reset latch**

Switch Resistance

- **Sampling Phase**



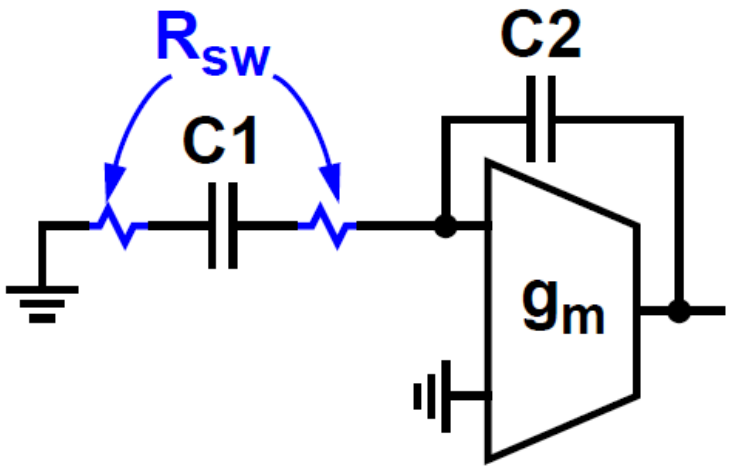
- **If R_{sw} is constant, it has only a filtering (linear) effect which is benign**
- **The on-resistance of MOS switches varies with V_{gs} (and hence V_{in})**

→ Must make MOS switches large enough

Switch Resistance

- **Integration Phase**

Differential Half-Circuit:

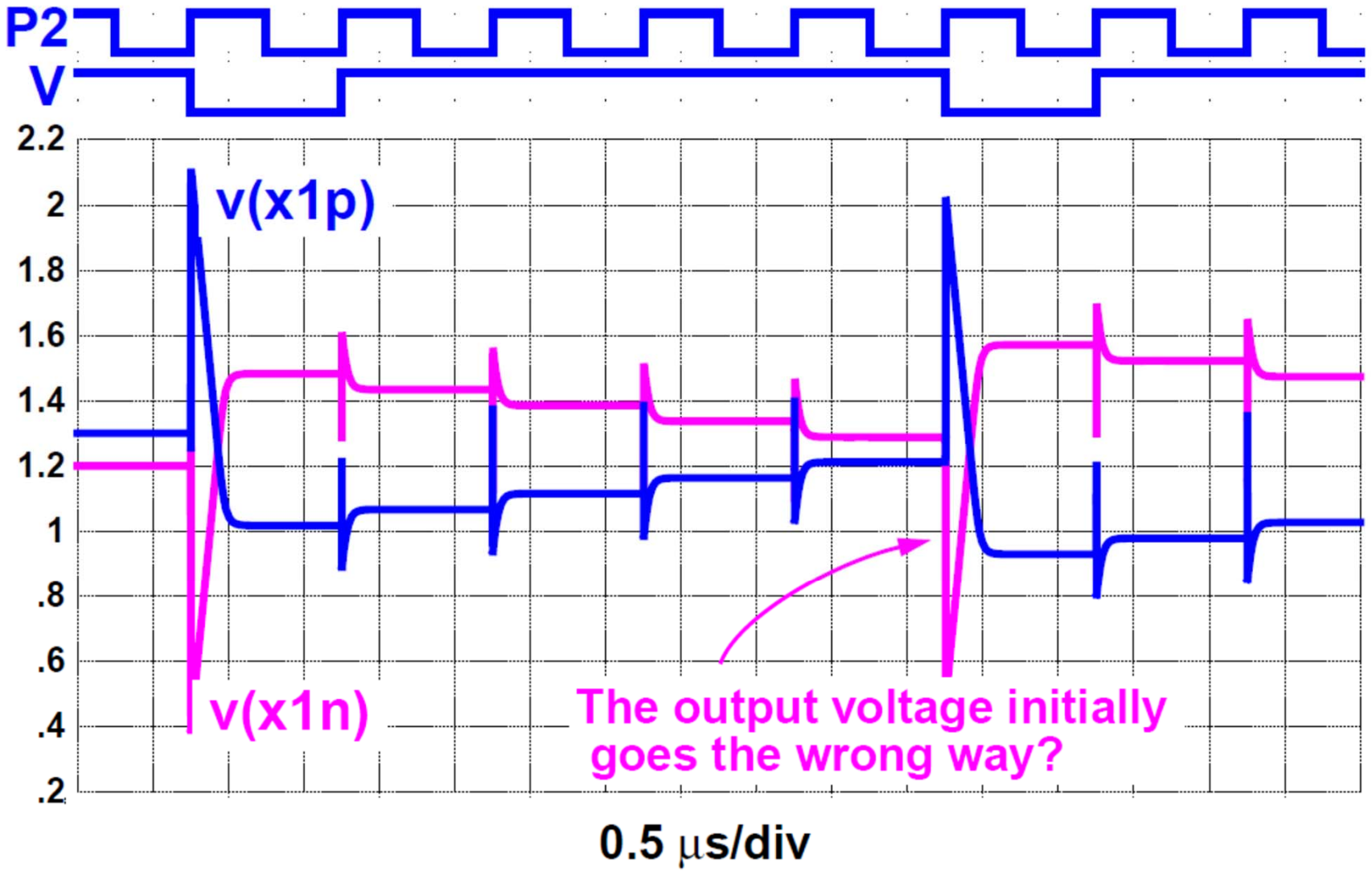


- R_{sw} **increases the settling time by a factor of** $1 + 2g_m R_{sw}$

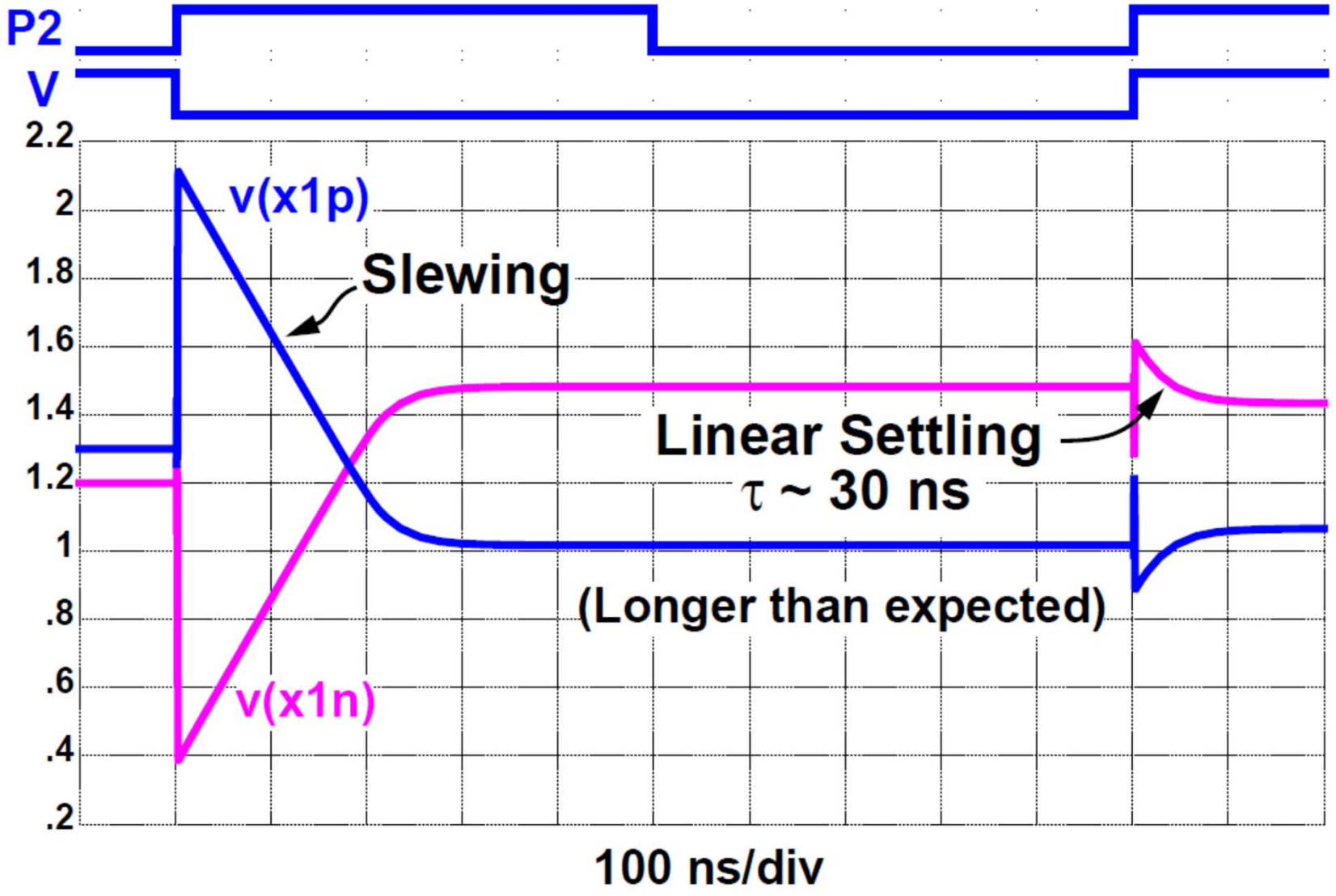
→ **Set** $R_{sw} \leq \frac{1}{20g_m}$ **to make the increase in** τ **small**

- **So in our MOD2, we want** $R_{sw} \leq 0.7\text{k}\Omega$

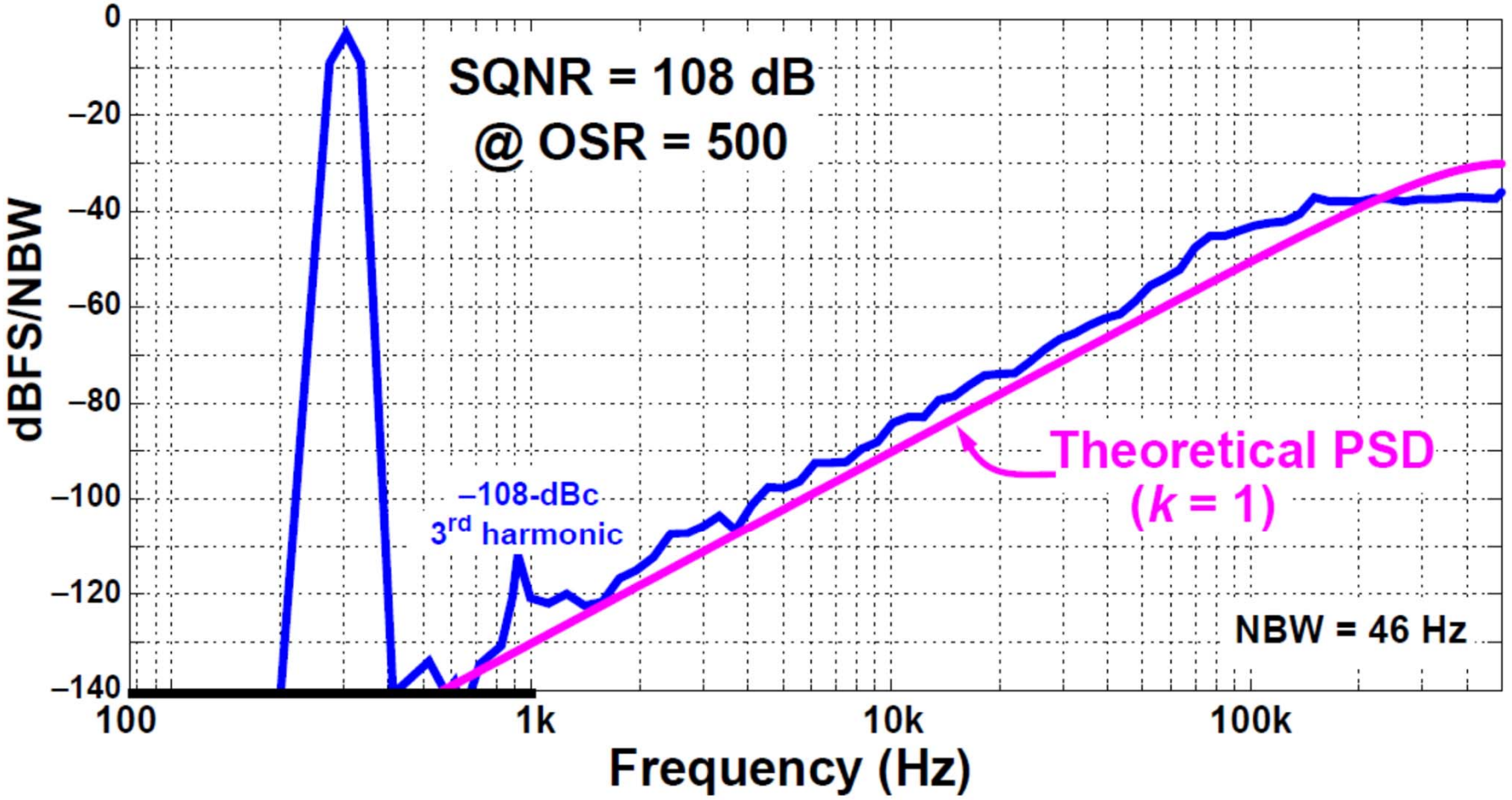
Simulated Waveforms



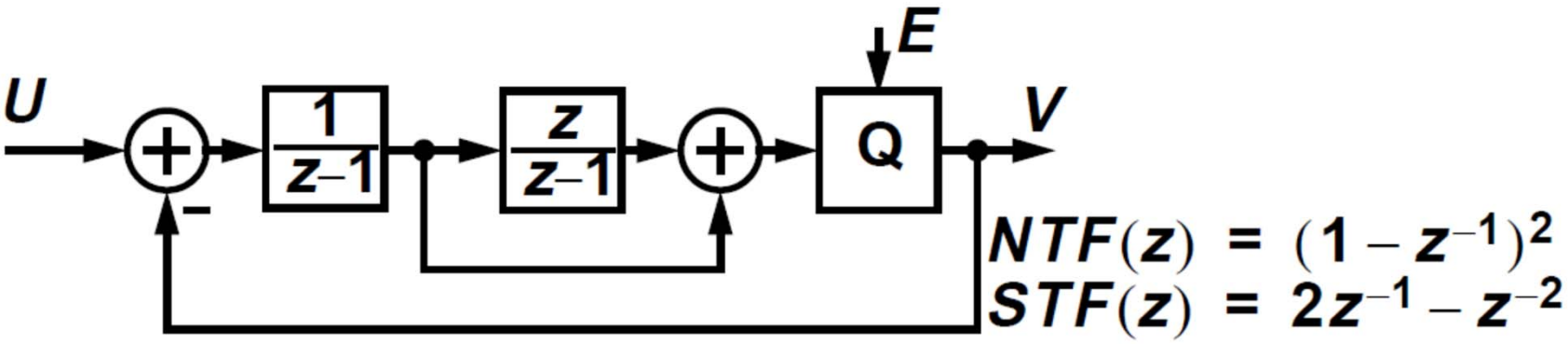
Expanded Waveforms



Simulated Spectrum

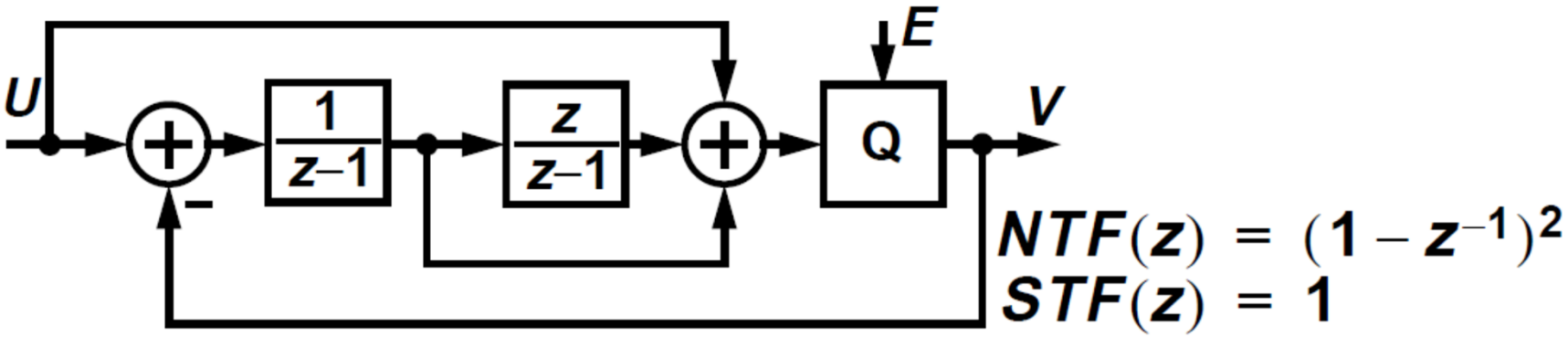


Topological Variant: Feed-Forward



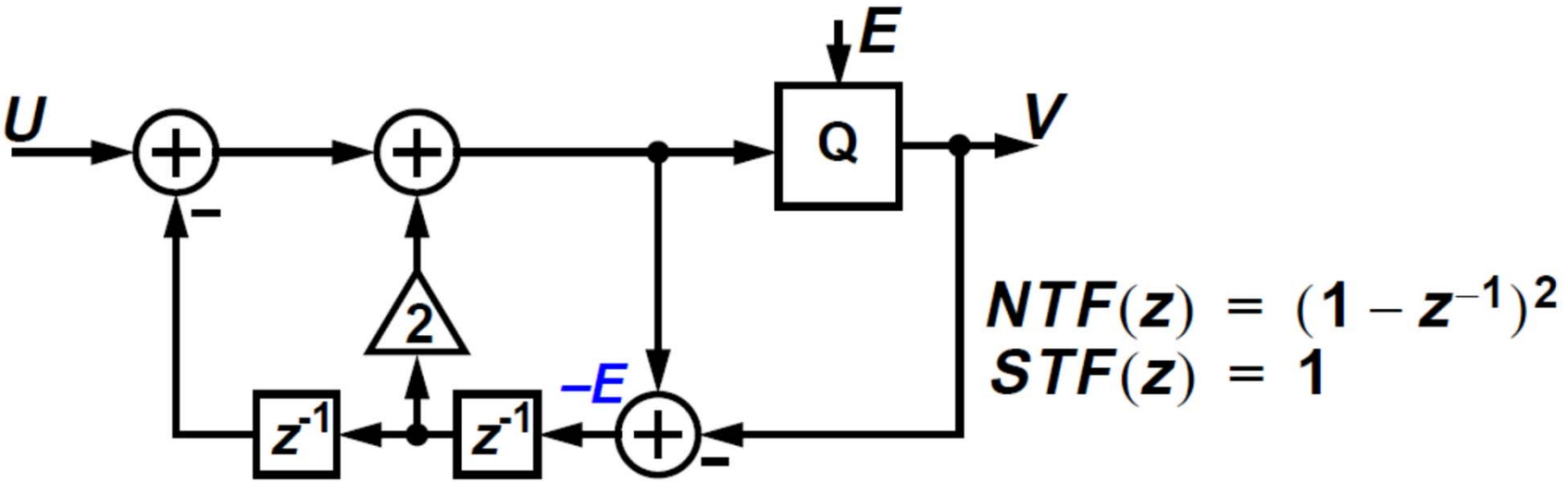
- **Output of first integrator has no DC component**
  - **Dynamic range requirements of this integrator are relaxed**
- **Although $|STF| \approx 1$ near $\omega = 0$, $|STF| = 3$ for $\omega = \pi$**
  - **Instability is more likely**

Topological Variant: Input Feed-Forward



- **No DC component in either integrator's output**
  - **Reduced dynamic range requirements in both integrators, especially for multi-bit modulators**
- **Perfectly flat STF**
  - **No increased risk of instability**
- **Timing is tricky**

Topological Variant: Error Feedback



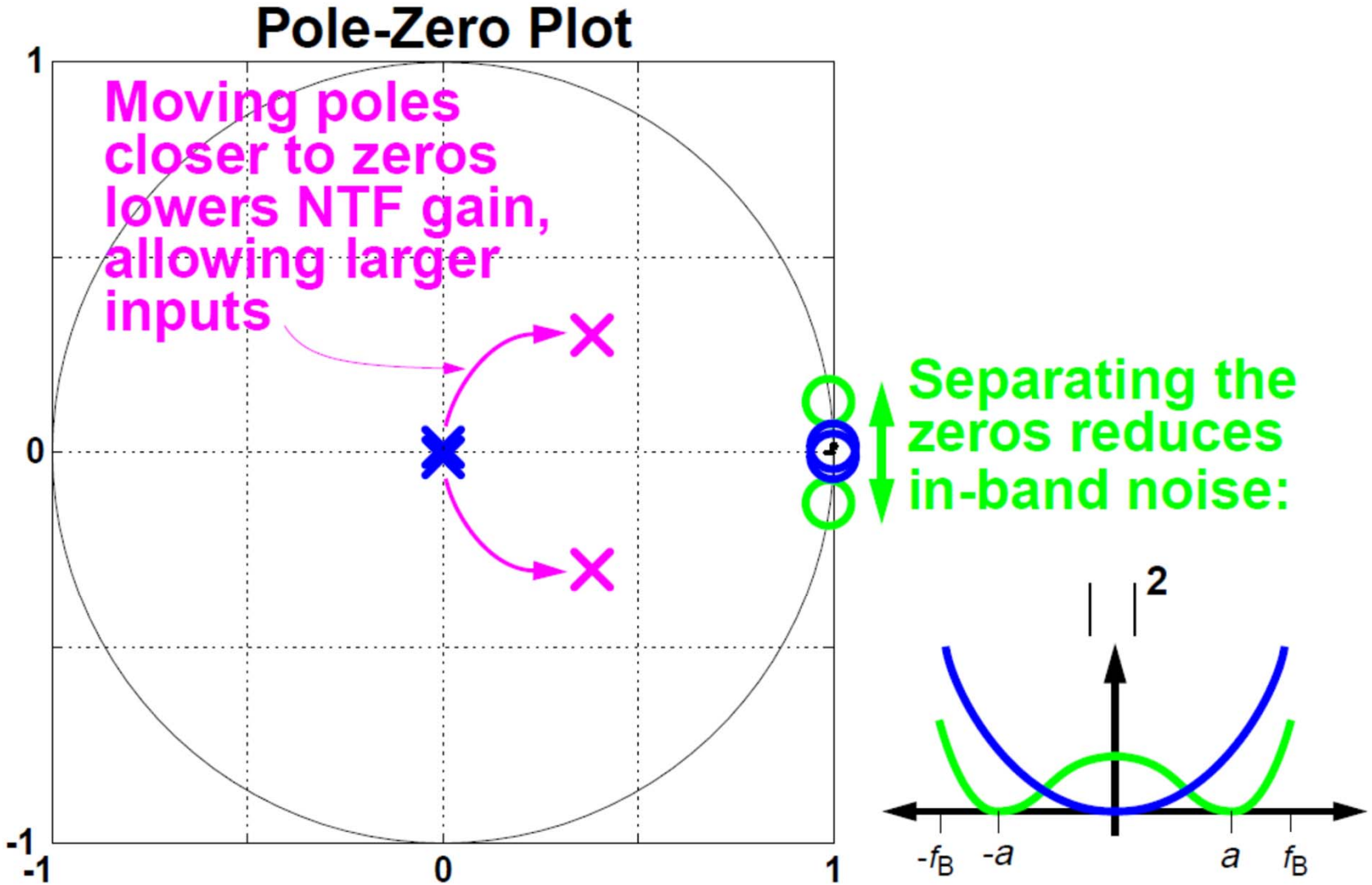
- **Simple**
- **Very sensitive to gain errors**

  Only suitable for digital implementations

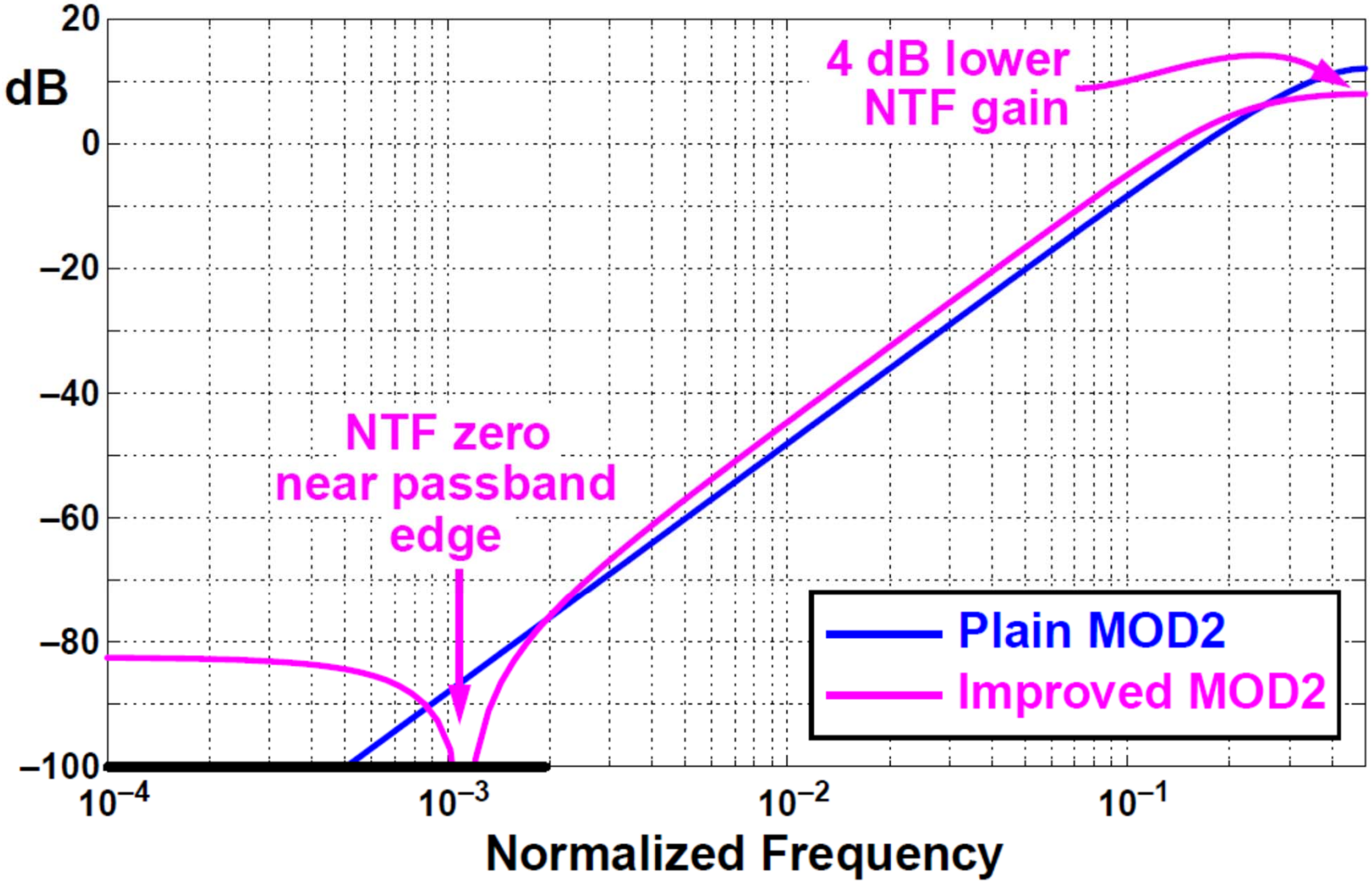
Is MOD2 the only 2nd-order modulator?

- **Except for filtering provided by the STF, any modulator with the same NTF as MOD2 has the same input-output behaviour as MOD2**
  - **SQNR curve is the same**
  - **Tonality of the quantization noise is unchanged**
- **Internal states, sensitivity, thermal noise, etc can differ from realization to realization**
- **A 2nd-order modulator is truly different only if it possesses a different 2nd-order NTF**

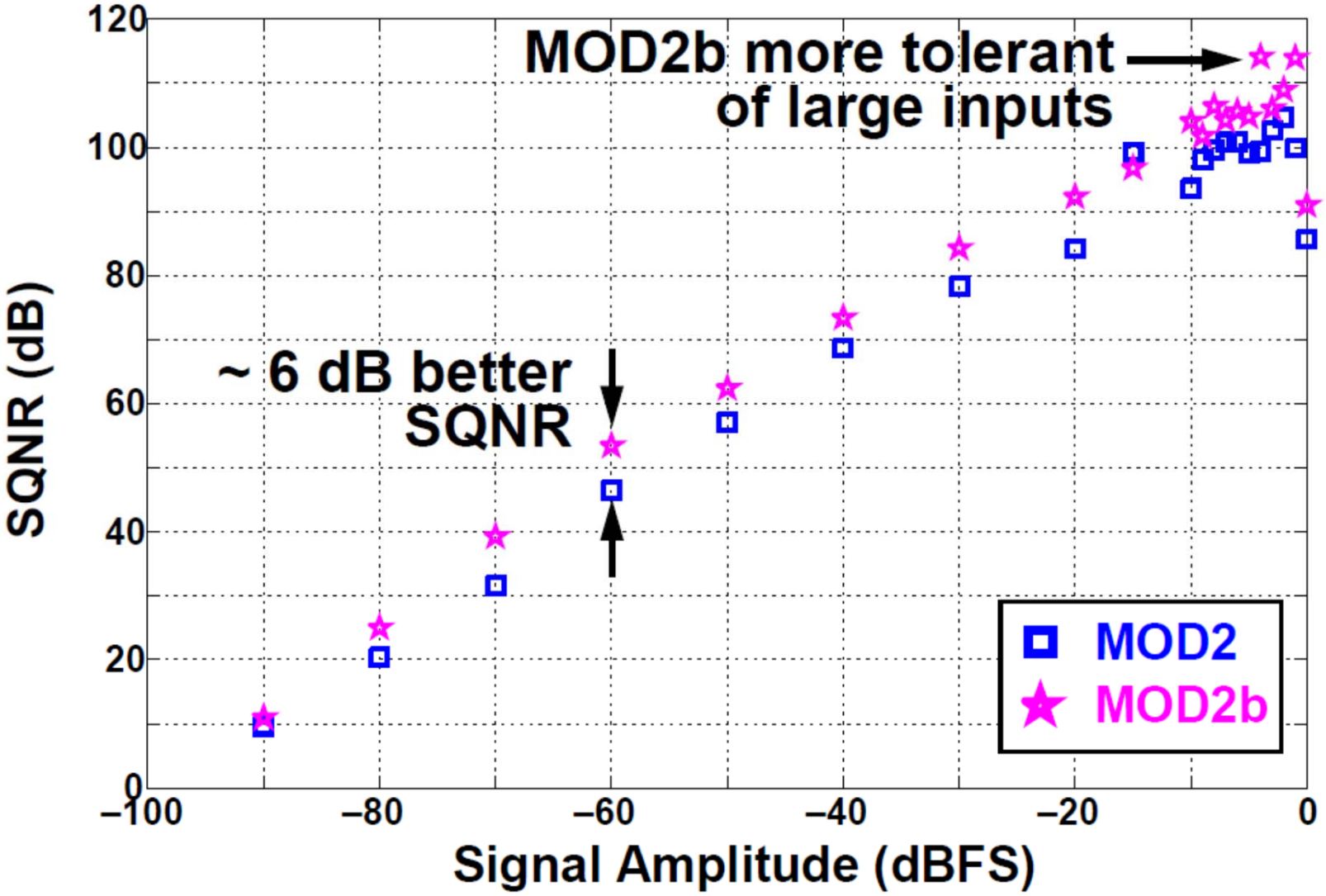
A Better 2nd-Order NTF



NTF Comparison

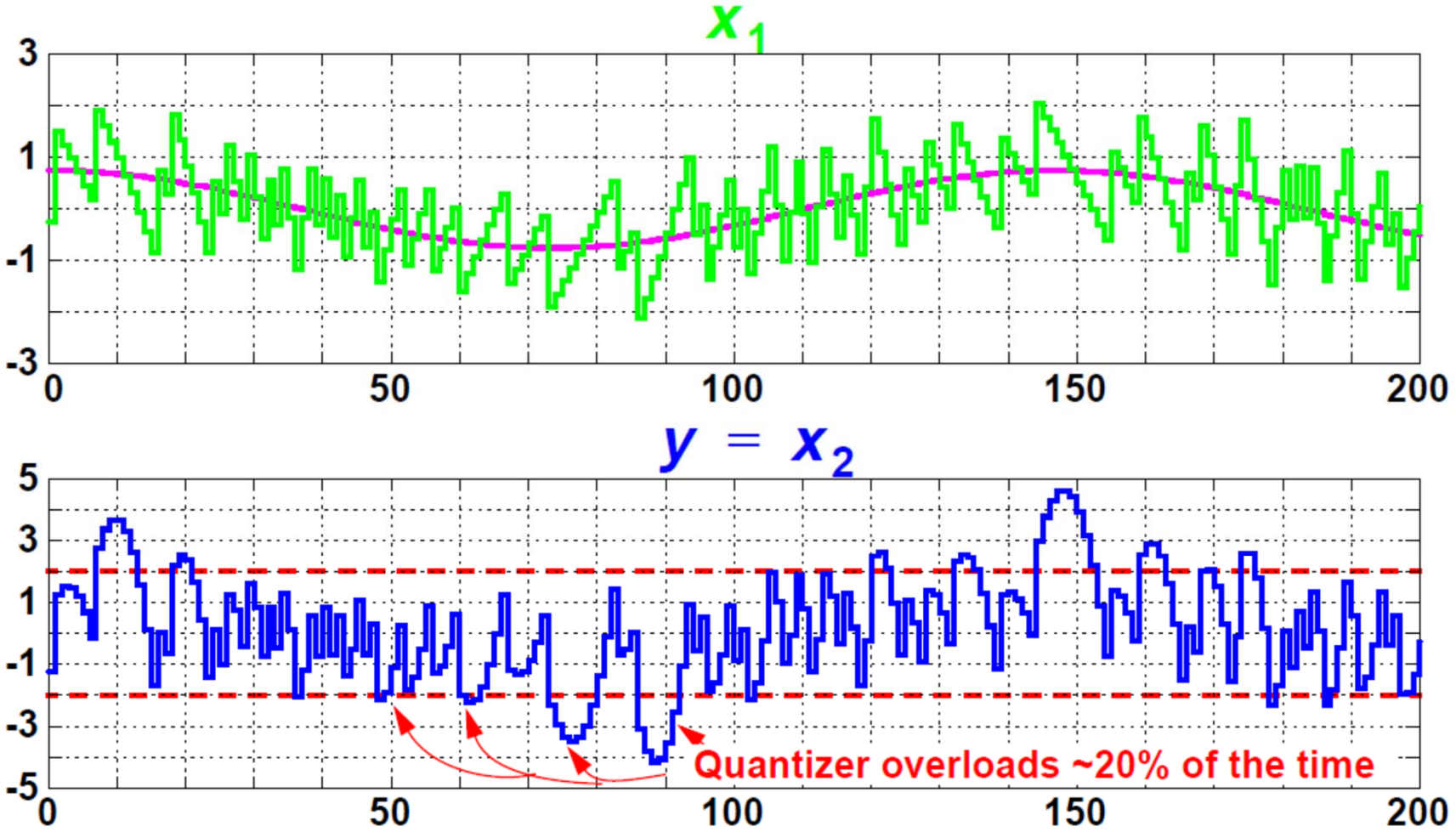


SNR vs Amp Comparison



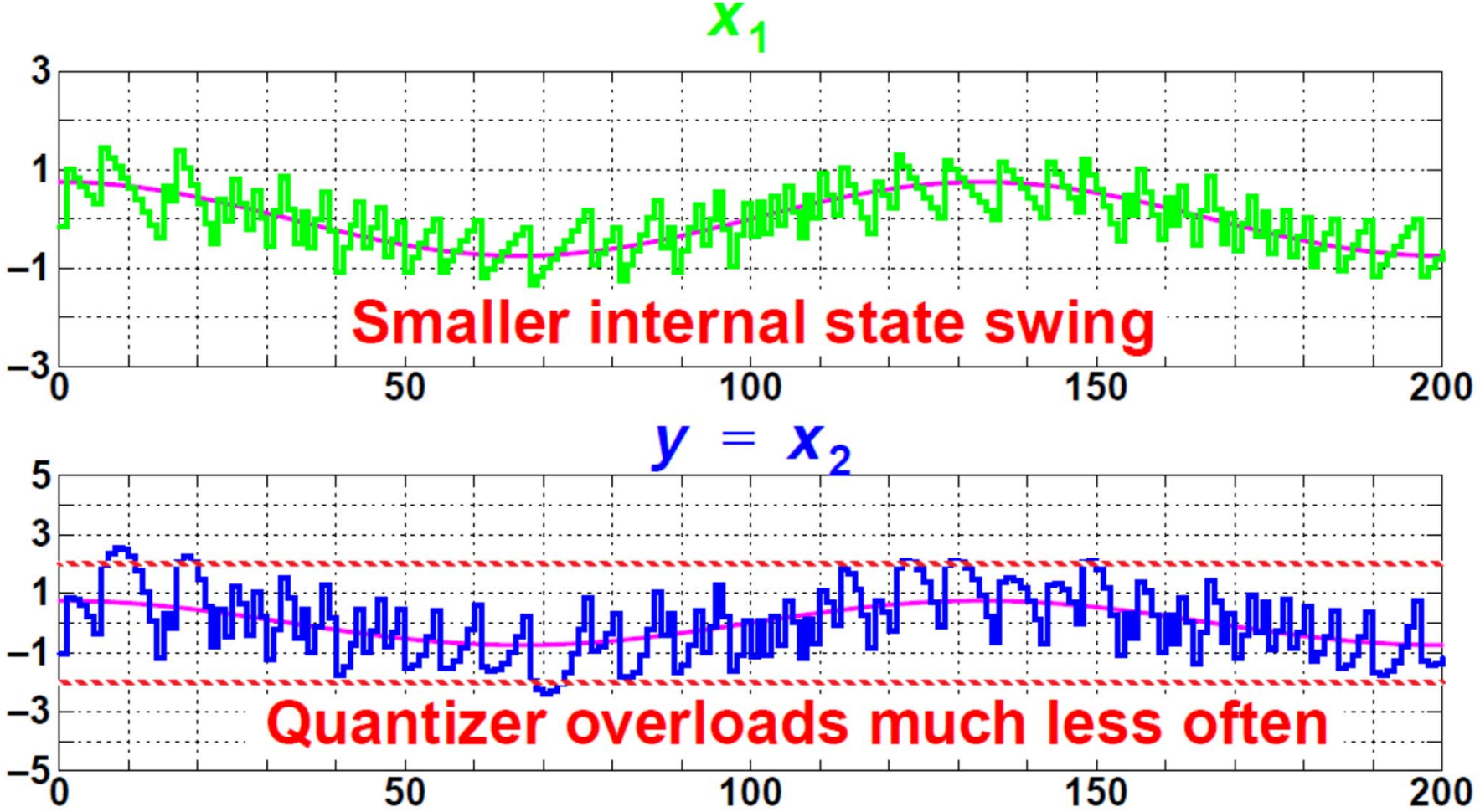
MOD2 Internal Waveforms

- **Input at 75% of Full-Scale**

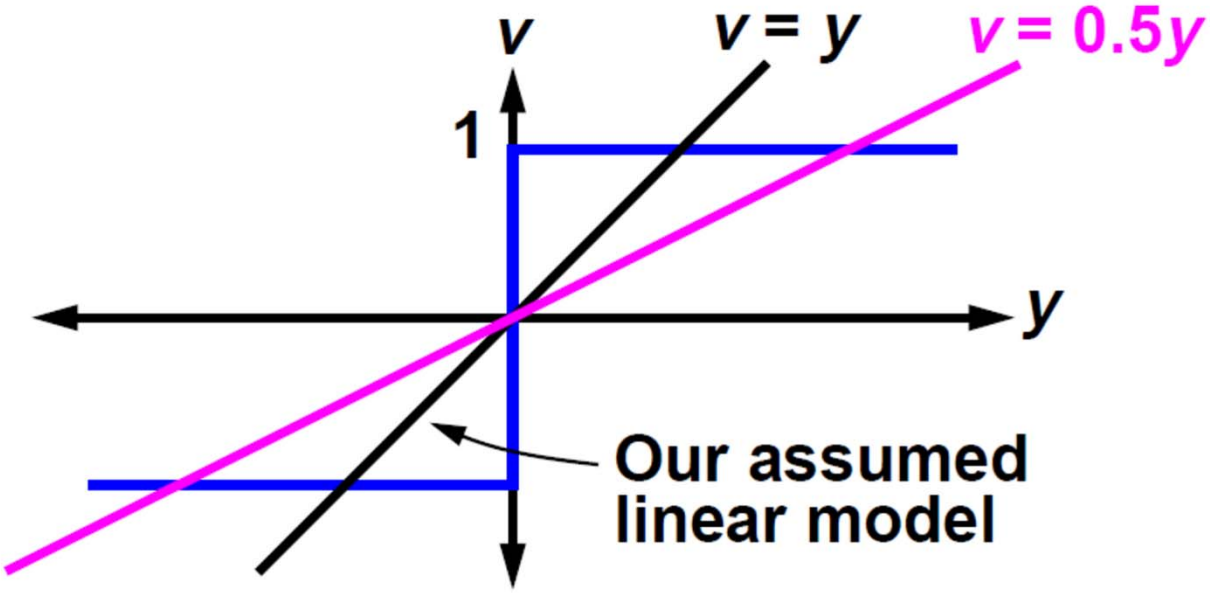


MOD2b Internal Waveforms

- **Input at 75% of Full-Scale**



Gain of a Binary Quantizer



- **The effective gain of a binary quantizer is not known a priori**
- **The gain (k) depends on the statistics of the quantizer's input**

  Halving the signal doubles the gain

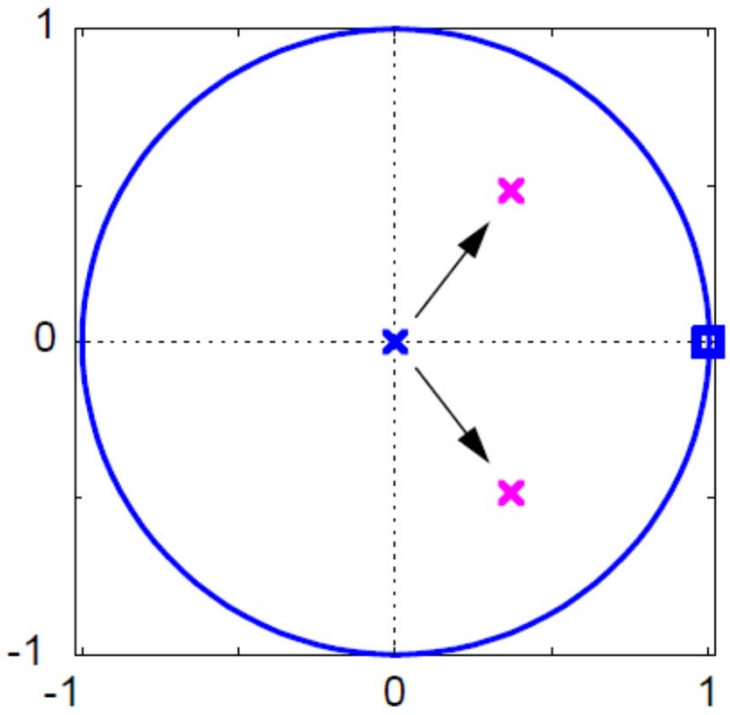
Gain of the Quantizer in MOD2

- **The effective gain of a binary quantizer can be computed from the simulation data using the following equation [PST Eq 2.14]**

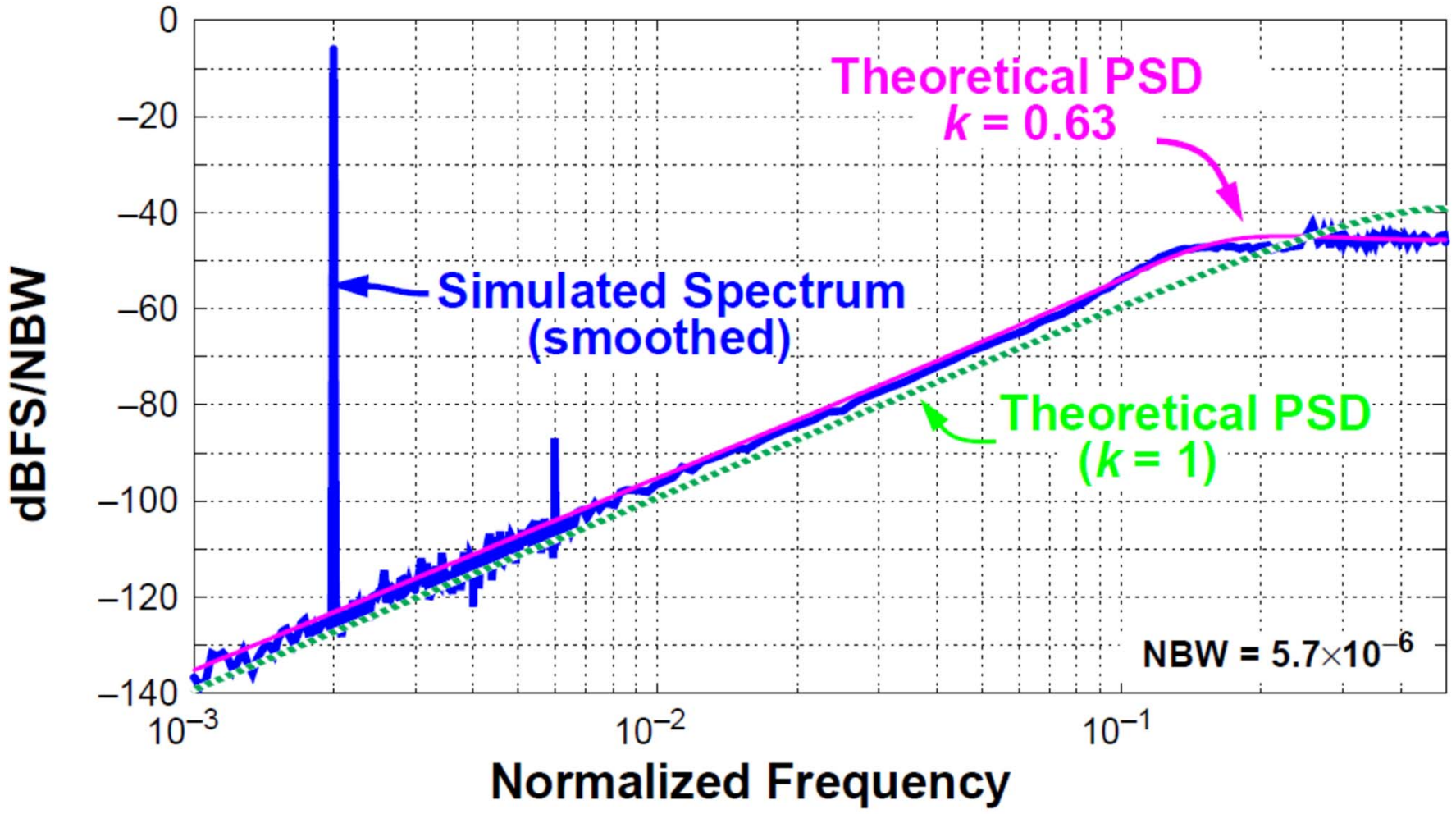
$$k = \frac{E[|y|]}{E[y^2]}$$

- $k \neq 1$ **alters the NTF**

$$NTF_k(z) = \frac{NTF_1(z)}{k + (1-k)NTF_1(z)}$$



Revised PSD Prediction



- **Much more similar to theoretical PSD**

Variable Quantizer Gain

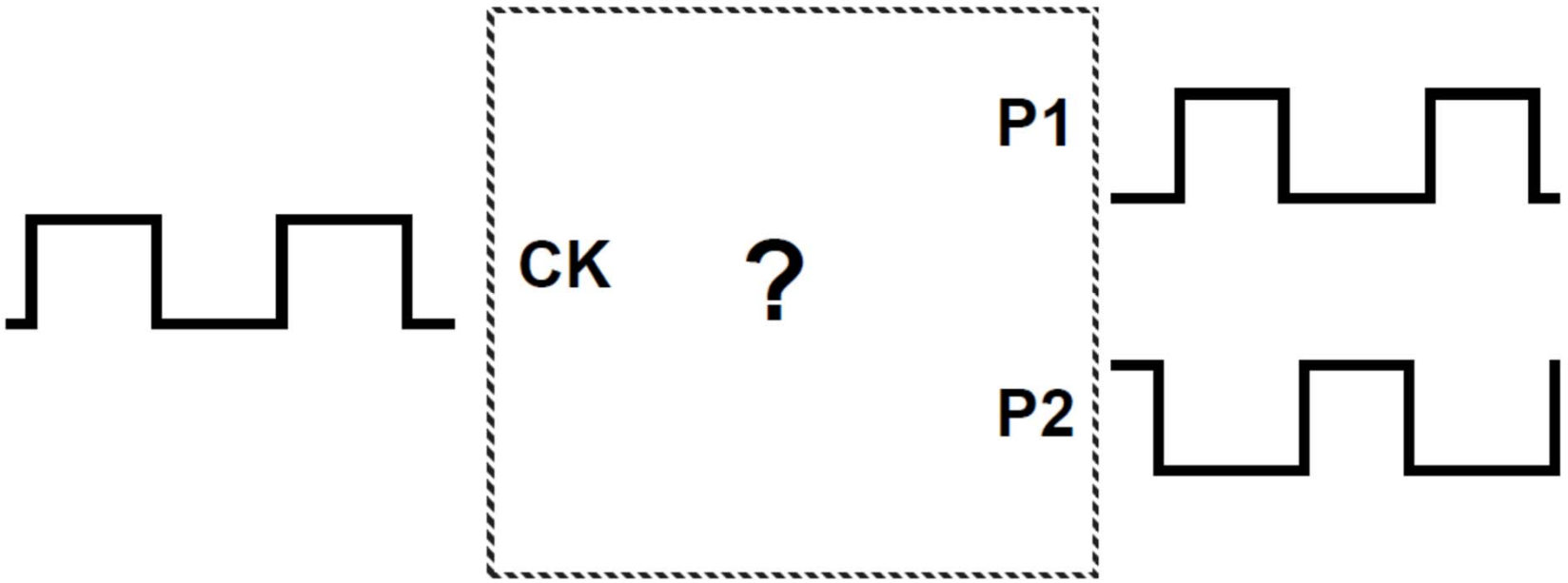
- When the input is small (below -12 dBFS) the effective gain of MOD2's quantizer is $k = 0.75$
- MOD2's 'small-signal NTF' is thus

$$NTF(z) = \frac{(z-1)^2}{z^2 - 0.5z + 0.25}$$

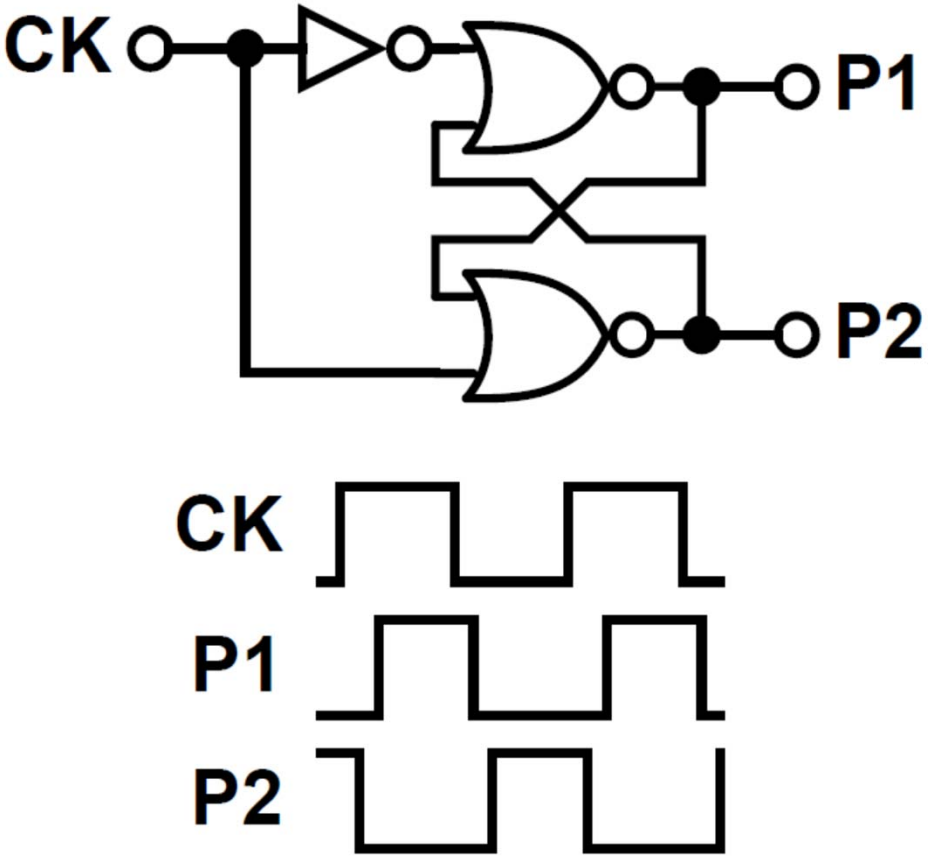
- This NTF has 2.5 dB less quantization noise suppression than the $(1 - z^{-1})^2$ NTF derived from the assumption that $k = 1$
- As the input signal increases, *k* decreases and the suppression of quantization noise degrades

  SQNR increases less quickly than the signal power. Eventually the SQNR saturates and then decreases as the signal power reaches full-scale.

Circuit of the Day: Non-Overlap Clock Gen

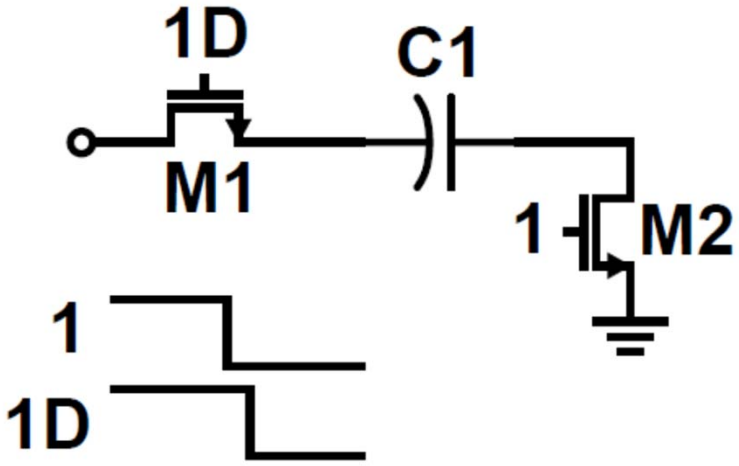


Circuit of the Day: Non-Overlap Clock Gen



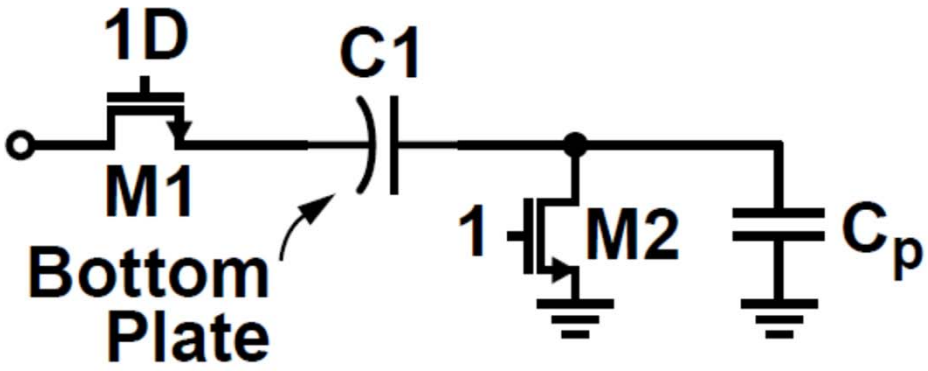
- **Non-overlap time set by NOR's t_{PLH}**

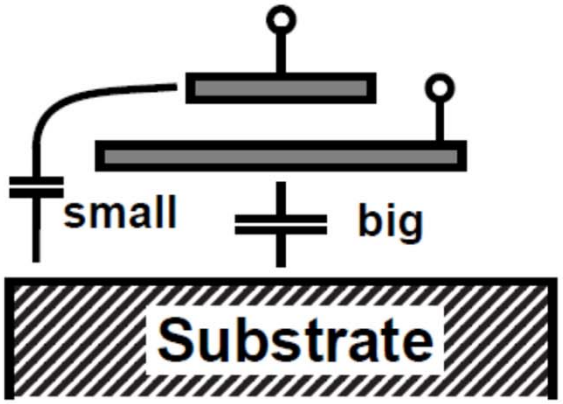
Clocking Details, Early/Late Phases



- **Charge injected via M1 is (non-linearly) signal-dependent while charge injection from M2 is signal-independent**
- **Open M2 (early) then open M1 (late) so that charge injected from C_{gs1} cannot enter C1**

Clocking Details, Bottom-plate sampling





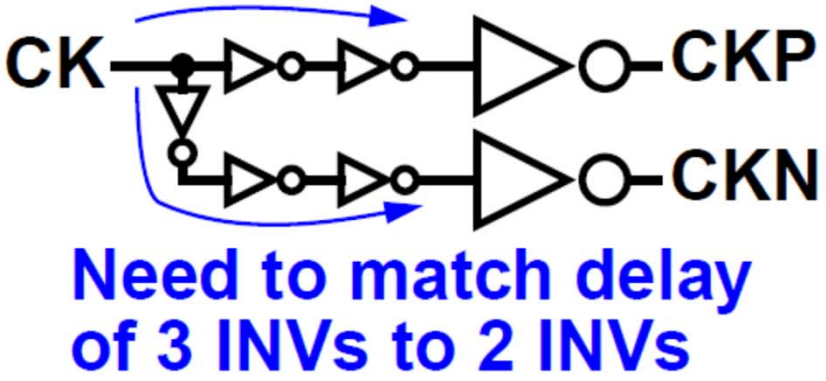
- **Parasitic capacitance on the right terminal of C1 degrades the op-amp feedback factor β**
- **C_p for the top plate is smaller, so use the top plate for the right terminal and the bottom plate for the left**

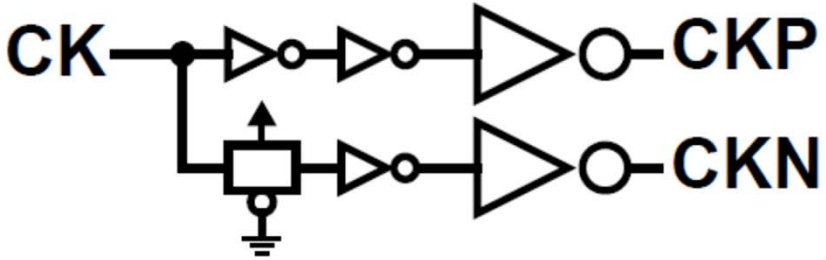
Complementary Clock Alignment

- **We need complementary clocks if transmission gates are used for the switches**

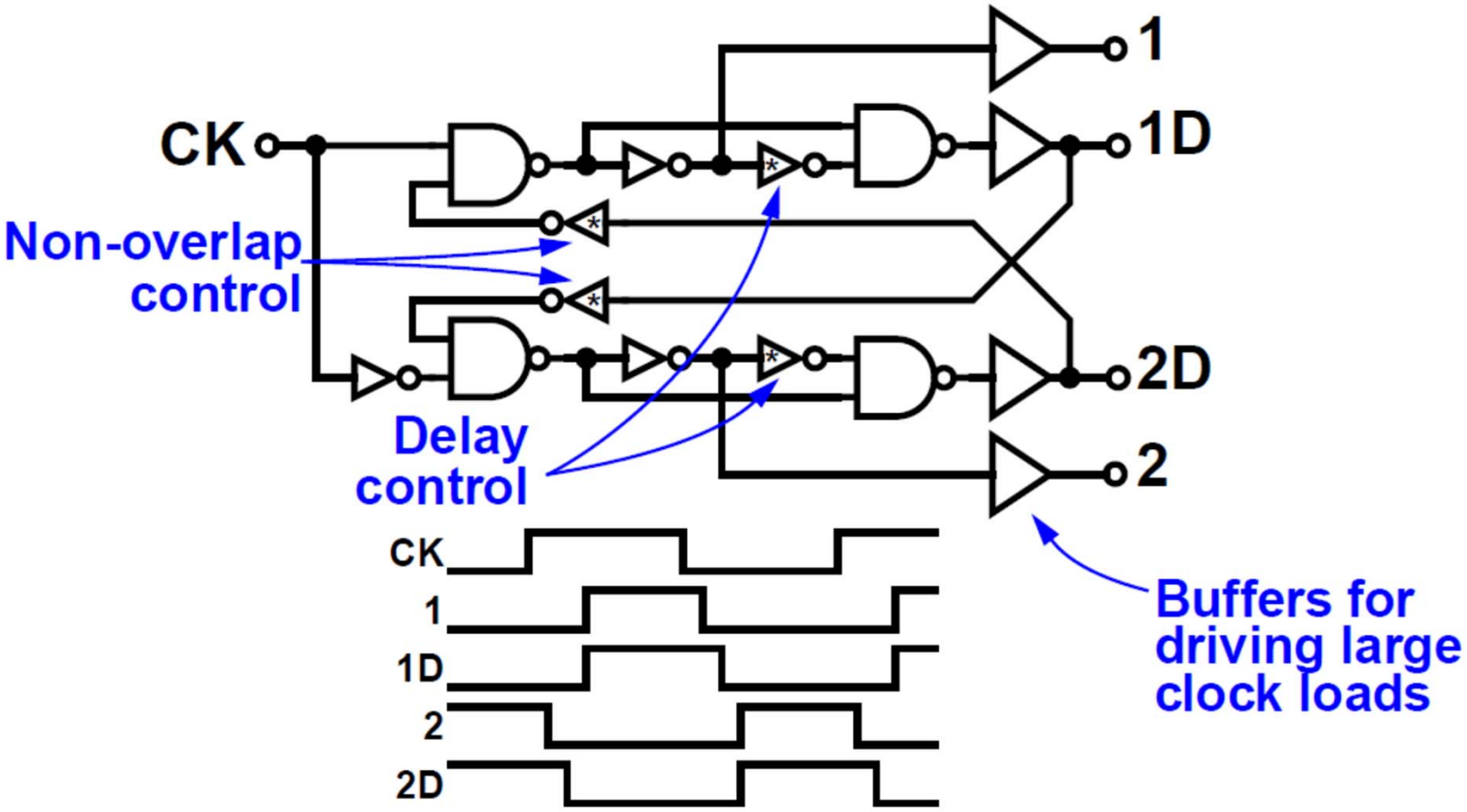
Q. How do we align them?

A. Carefully size the inverters relative to their capacitive loads, or use a transmission gate to mimic an inverter delay:





Professional Clock Generator



- **To maximize the time available for settling, make the early and late phases start at the same time**

Homework #4 (Due Feb 25*)

- **Construct a differential switched-capacitor implementation of MOD2 using ideal elements (switches, capacitors, amplifiers, comparator) and verify it.**
- **Scale the circuit such that the full-scale differential input range is [-1,+1] V and the op amp swing is 0.5 $V_{p,diff}$ at -6 dBFS. You may assume that -0.5 V and +0.5V references are available and that the input is available in differential form.**
- **Choose capacitor values such that the SNR with a -6 dBFS input will be 90 dB when OSR = 128. You may assume that the only source of noise is kT/C noise.**

Homework #4 Deliverables

1. **Block diagram after dynamic-range scaling**
2. **Schematic with all cap values and clock phases clearly labelled**
3. **Open-loop impulse response plot (short transient sim)**
4. **Time-domain plots of input signal and integrator outputs for a -6 dBFS input (transient sim)**
5. **Spectrum of output data for a -6 dBFS input, with SNDR calculated**
6. **kT/C noise calculation (justify your choice of C)**

What You Learned Today

- **Transistor-level implementation of MOD2**
  - **Op-amp, SC CMFB, comparator, clock generator**
- **MOD2 variants**
- **Variable quantizer gain**