Lecture 4
Comparator & Flash ADC Design

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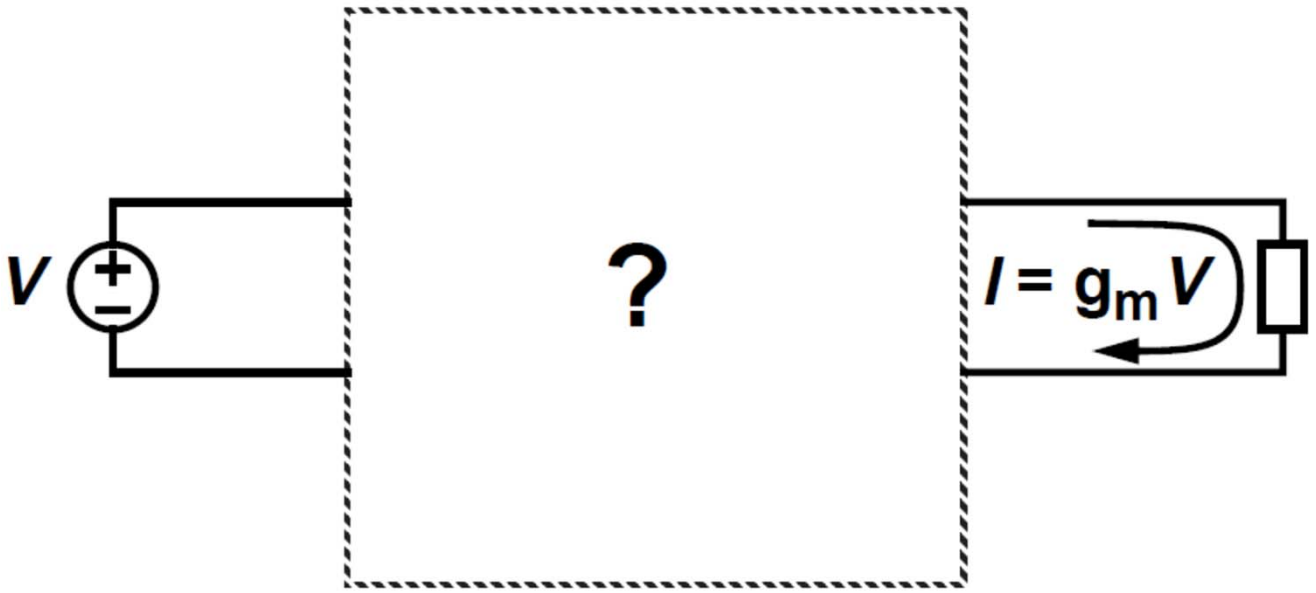
Lecture Plan

Date	Lecture (Wednesday 2-4pm)		Reference	Homework
2020-01-07	1	MOD1 & MOD2	PST 2, 3, A	1: Matlab MOD1&2
2020-01-14	2	MOD*N* + ΔΣ Toolbox	PST 4, B	2: ΔΣ Toolbox
2020-01-21	3	SC Circuits	R 12, CCJM 14	
2020-01-28	4	Comparator & Flash ADC	CCJM 10	3: Comparator
2020-02-04	5	Example Design 1	PST 7, CCJM 14	
2020-02-11	6	Example Design 2	CCJM 18	4: SC MOD2
2020-02-18	Reading Week / ISSCC			
2020-02-25	7	Amplifier Design 1		Project
2020-03-03	8	Amplifier Design 2		
2020-03-10	9	Noise in SC Circuits		
2020-03-17	10	Nyquist-Rate ADCs	CCJM 15, 17	
2020-03-24	11	Mismatch & MM-Shaping	PST 6	
2020-03-31	12	Continuous-Time ΔΣ	PST 8	
2020-04-07	Exam			
2020-04-21	Project Presentation (Project Report Due at start of class)			

Circuit of the Day: Linear Transconductor



- **Useful in many circuits**
  1. **Gm-C filter**
  2. **LNA**
  3. **Mixer**
  4. **Continuous-Time ΔΣ ADC**

What you will learn…

- **Example Comparator Circuit**
- **Regeneration Time Constant τ**
- **Metastability, Probability of Error**
- **Offset, Auto-zeroing**
- **Flash ADC**

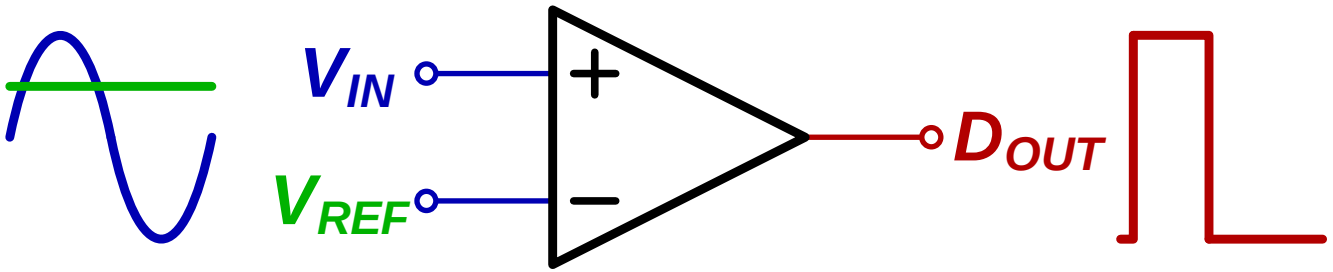
Comparator

- **Basic building block of an A/D converter**

  Acts as a 1-bit A/D converter

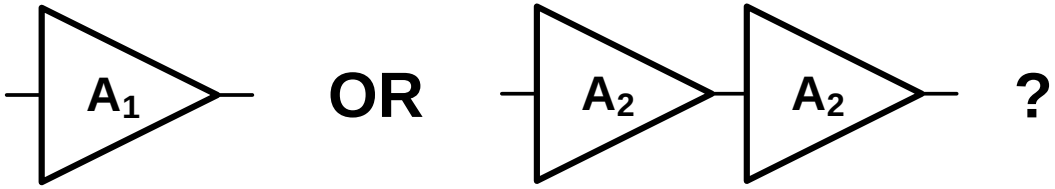
- **Output amplifies difference between V_{IN} & V_{REF}**

  With a large gain, output is ‘digital’ at either the positive or negative supply rail

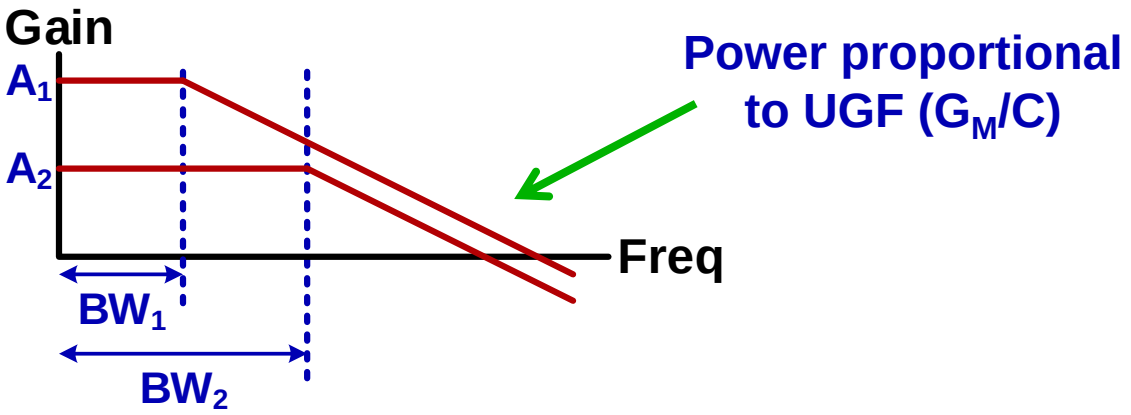


Comparator

- **Not an open-loop amplifier**



Amplifier (A_1) typically high gain, low 3dB frequency
Cascaded low-gain stages (A_2) faster for a given power

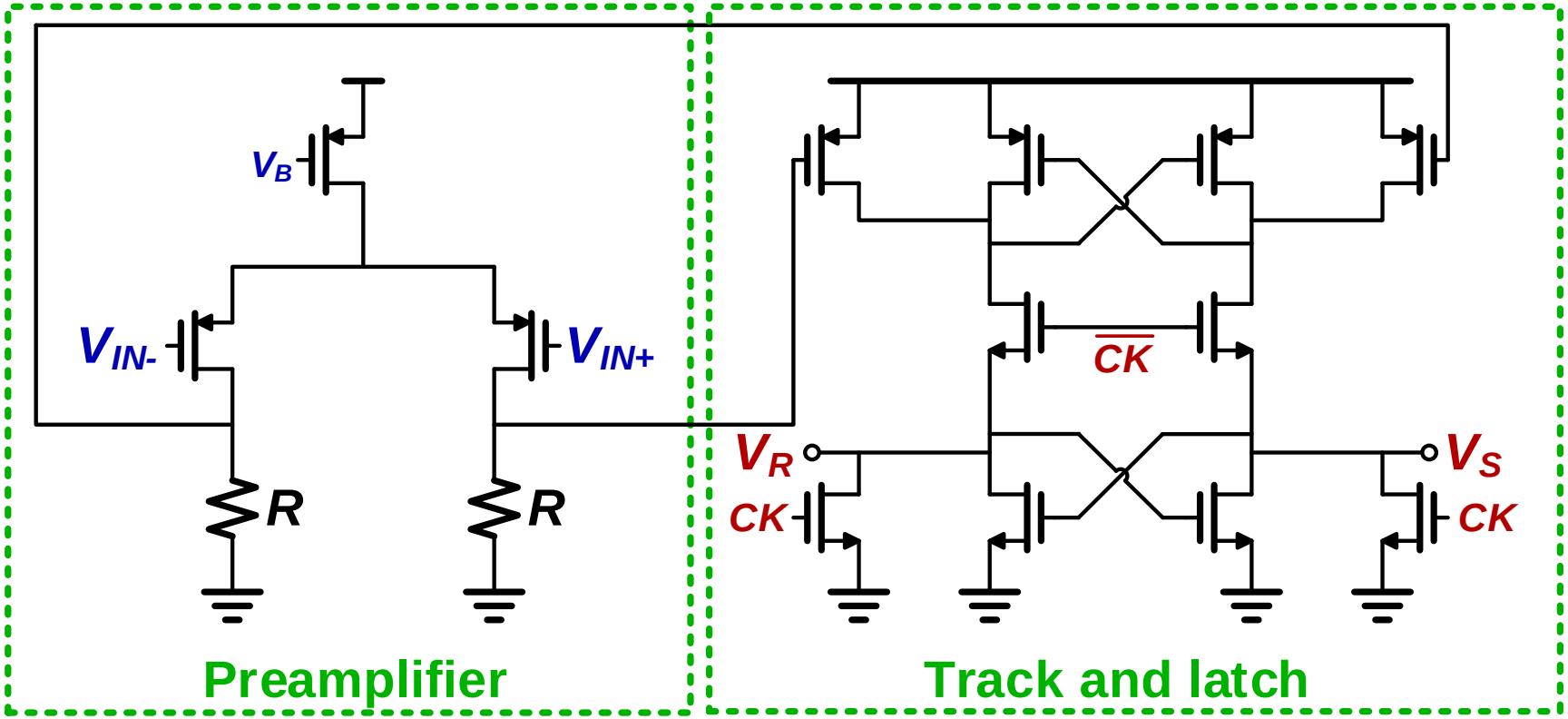


Comparator

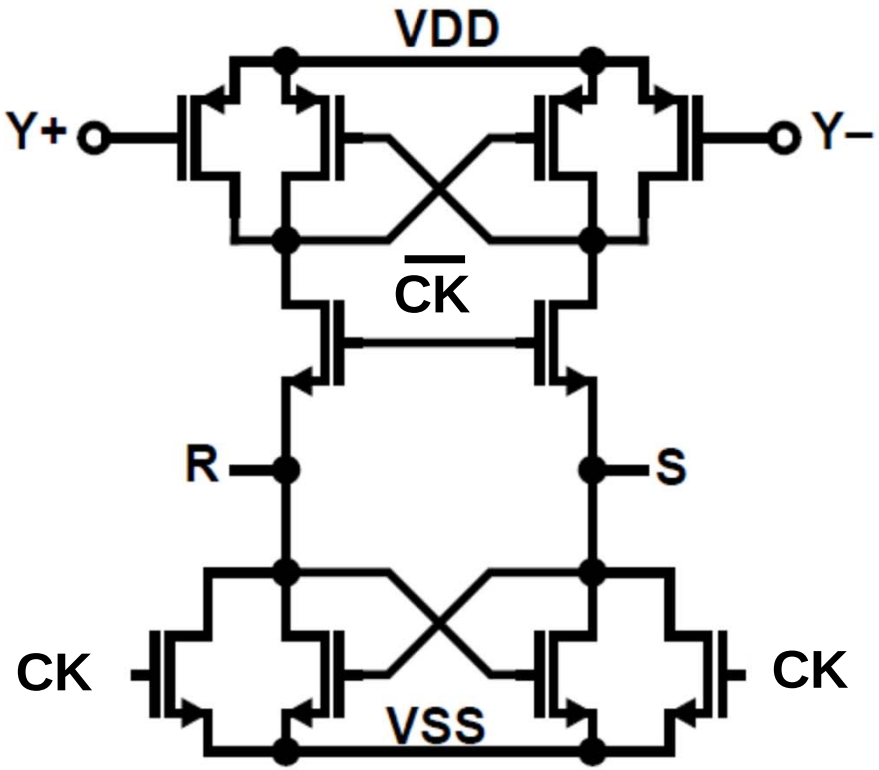
- **Latched comparator**

  Track when CK high, precharge output low

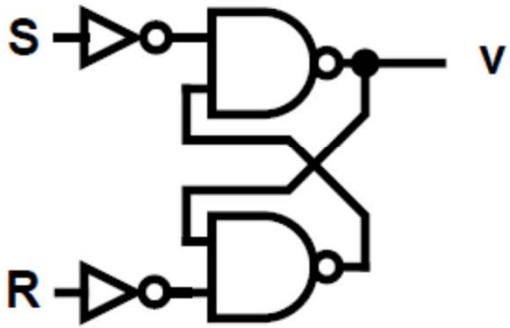
  Latch when CK low



Comparator: Track and Latch



Set/Reset Latch:

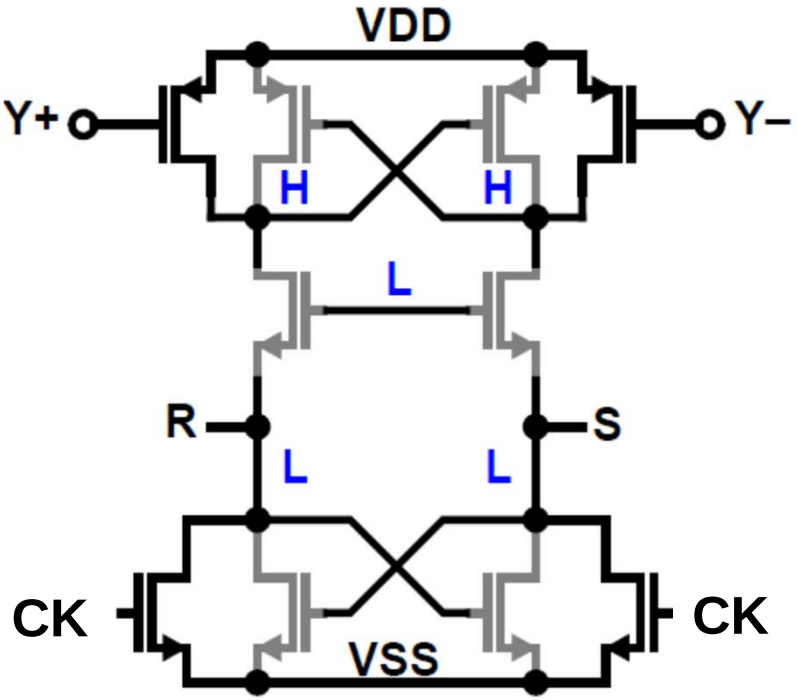


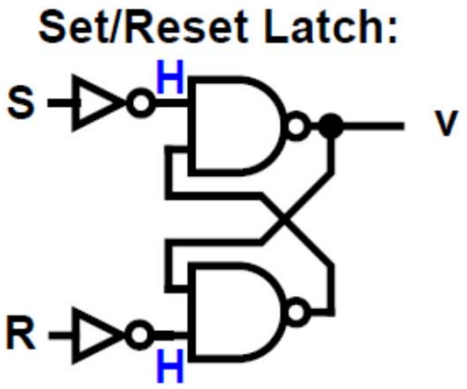
Inverter thresholds are chosen so that the inverters respond only after R/S have resolved.

- **Falling CK phase initiates regenerative action**
  - **S and R connected to a Set/Reset latch**

Comparator: Track and Latch

- **CK is High: ‘Reset’ or ‘Track’ Mode**





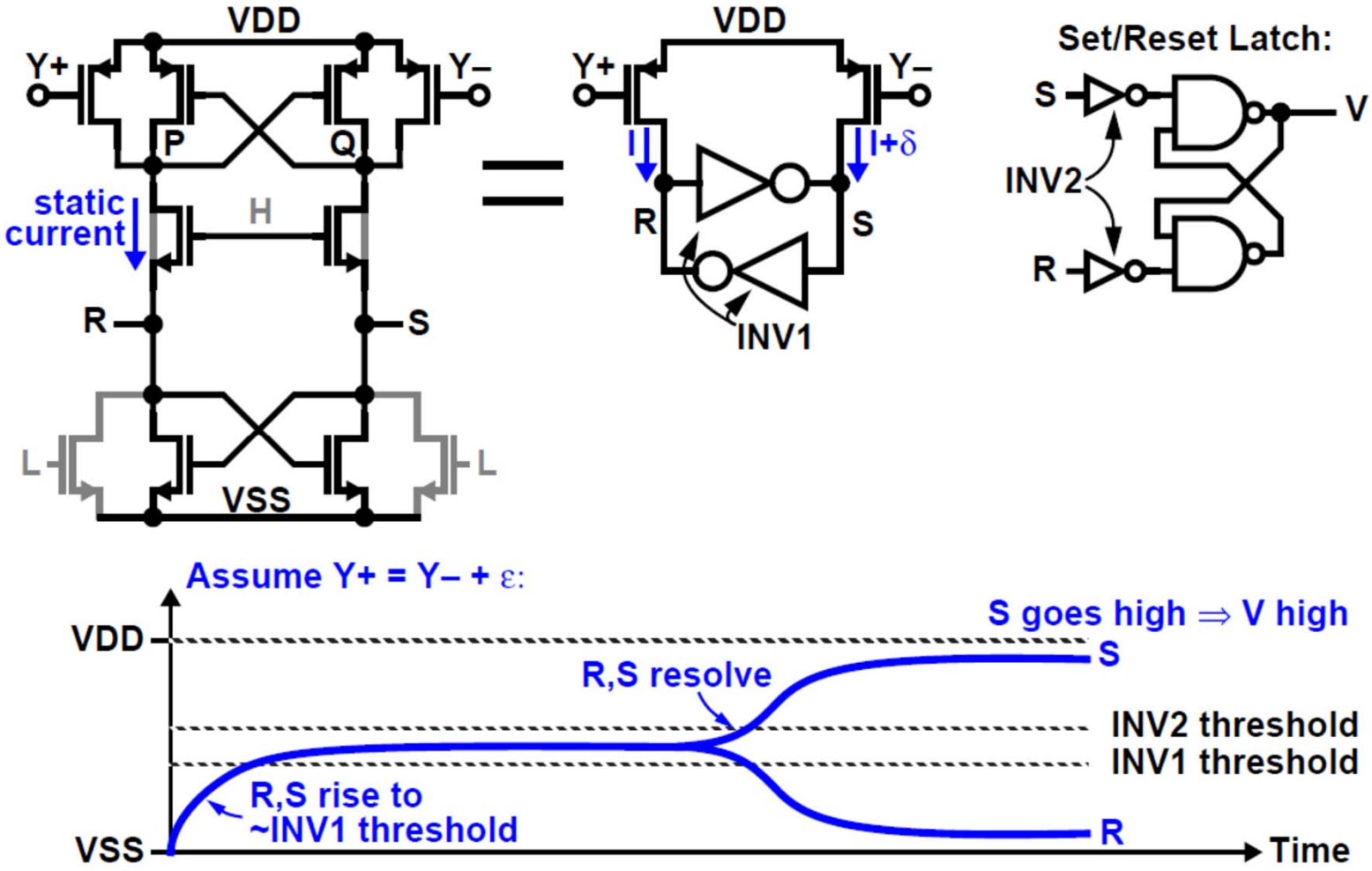
- **Active part of the comparator is reset**

  Grayed-out devices are off

- **R and S are low → the SR latch is in hold mode**

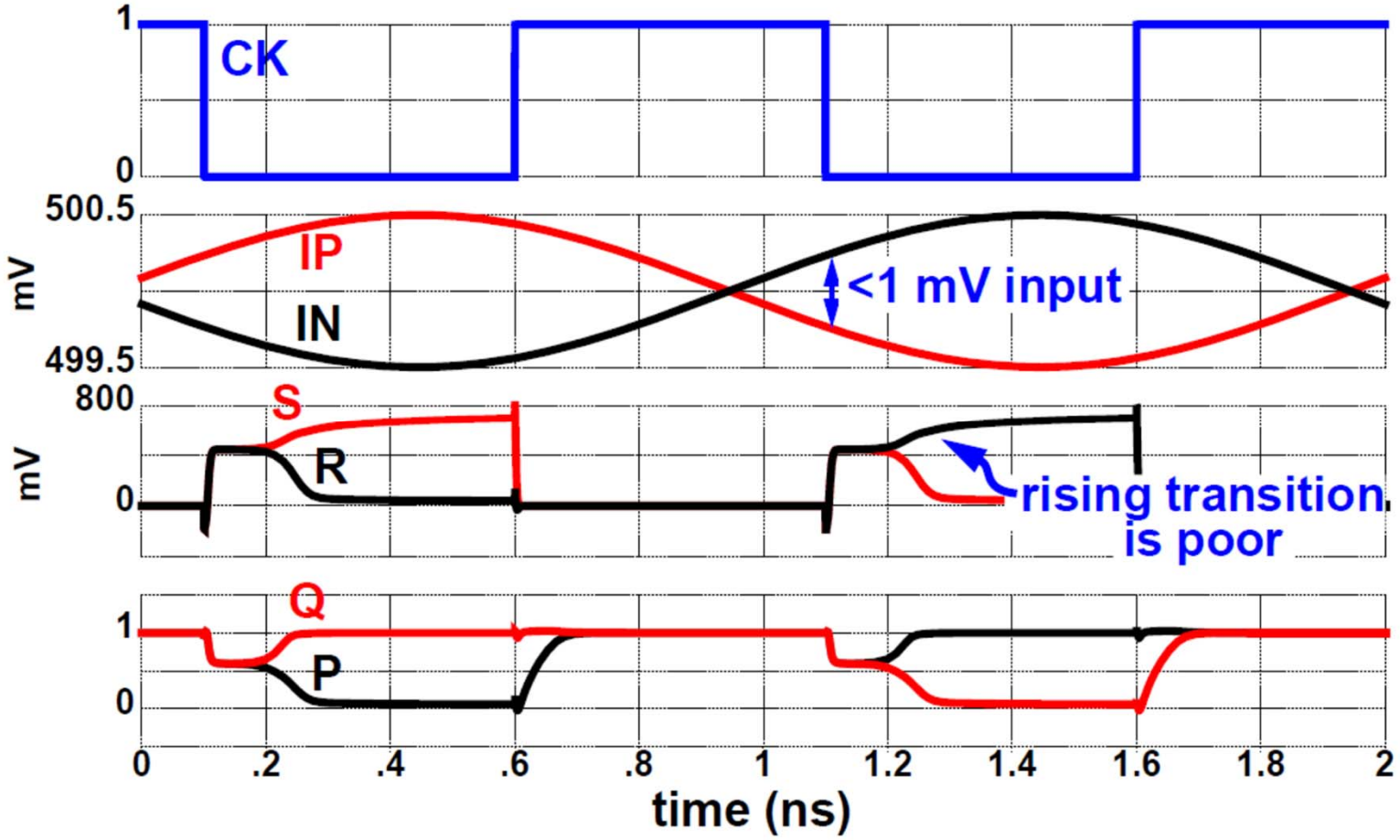
Comparator: Track and Latch

- **CK goes Low: 'Latch' Mode**

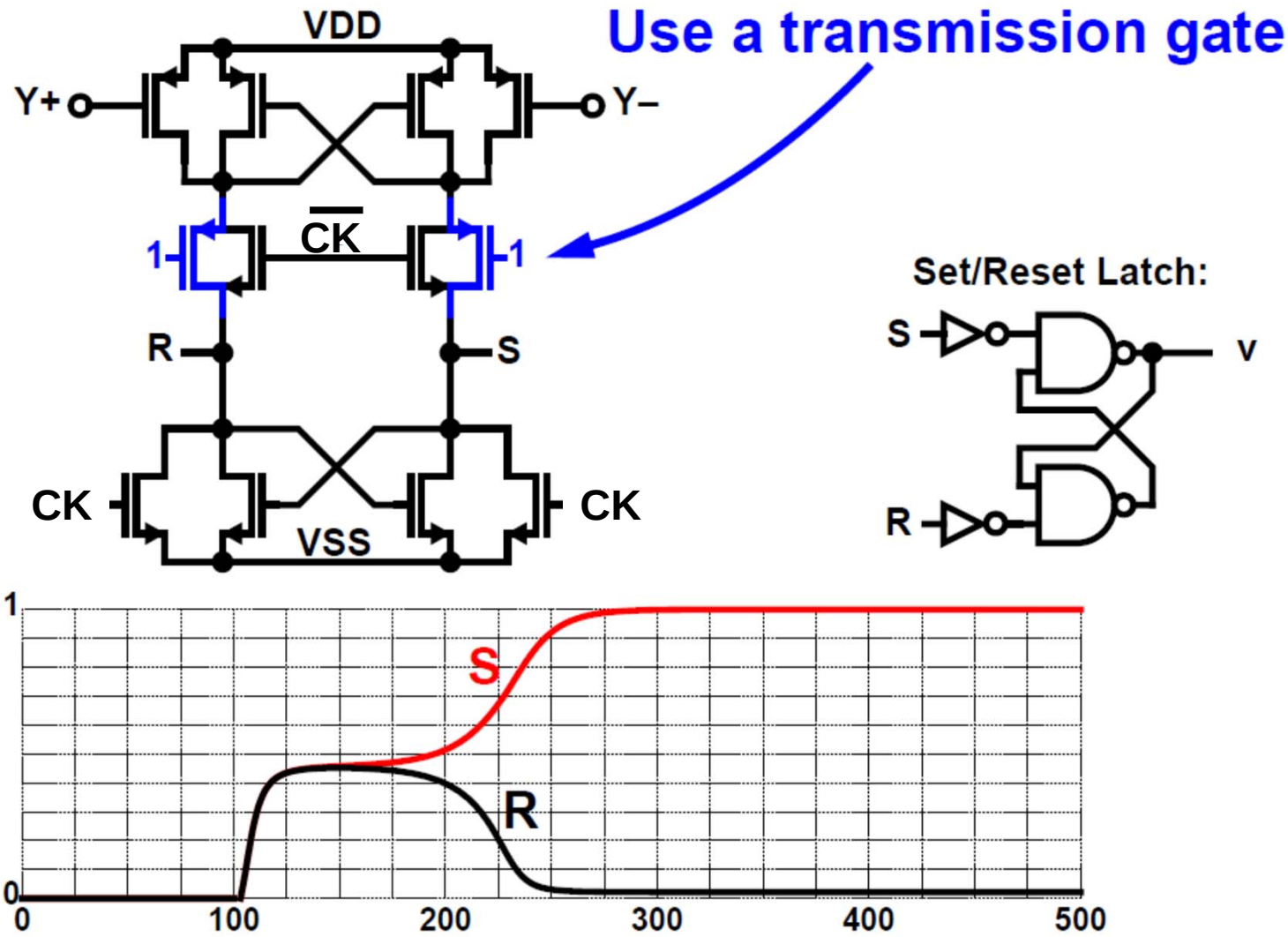


Example Waveforms

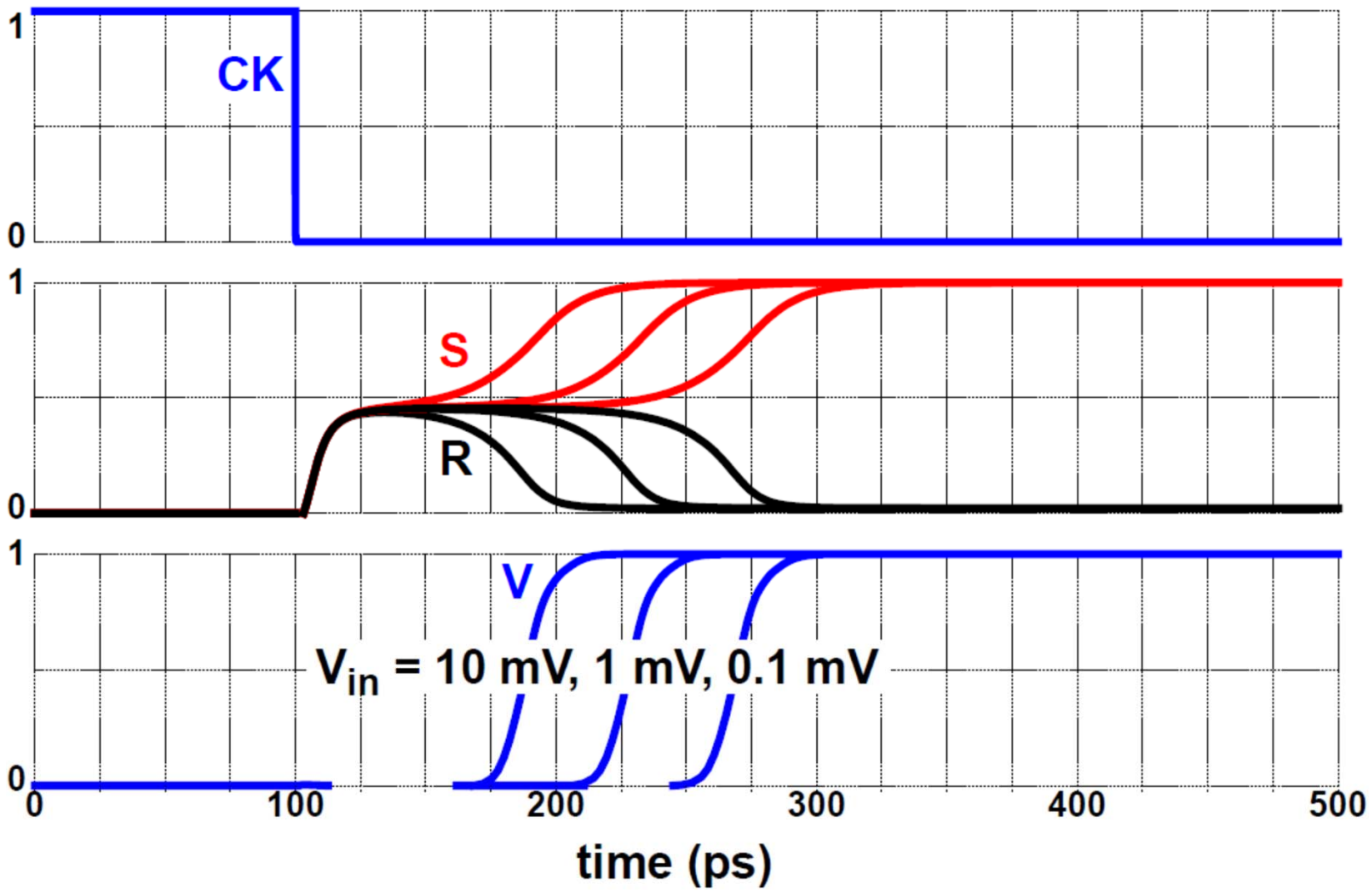
- **Quick design in 65nm with VDD=1V**



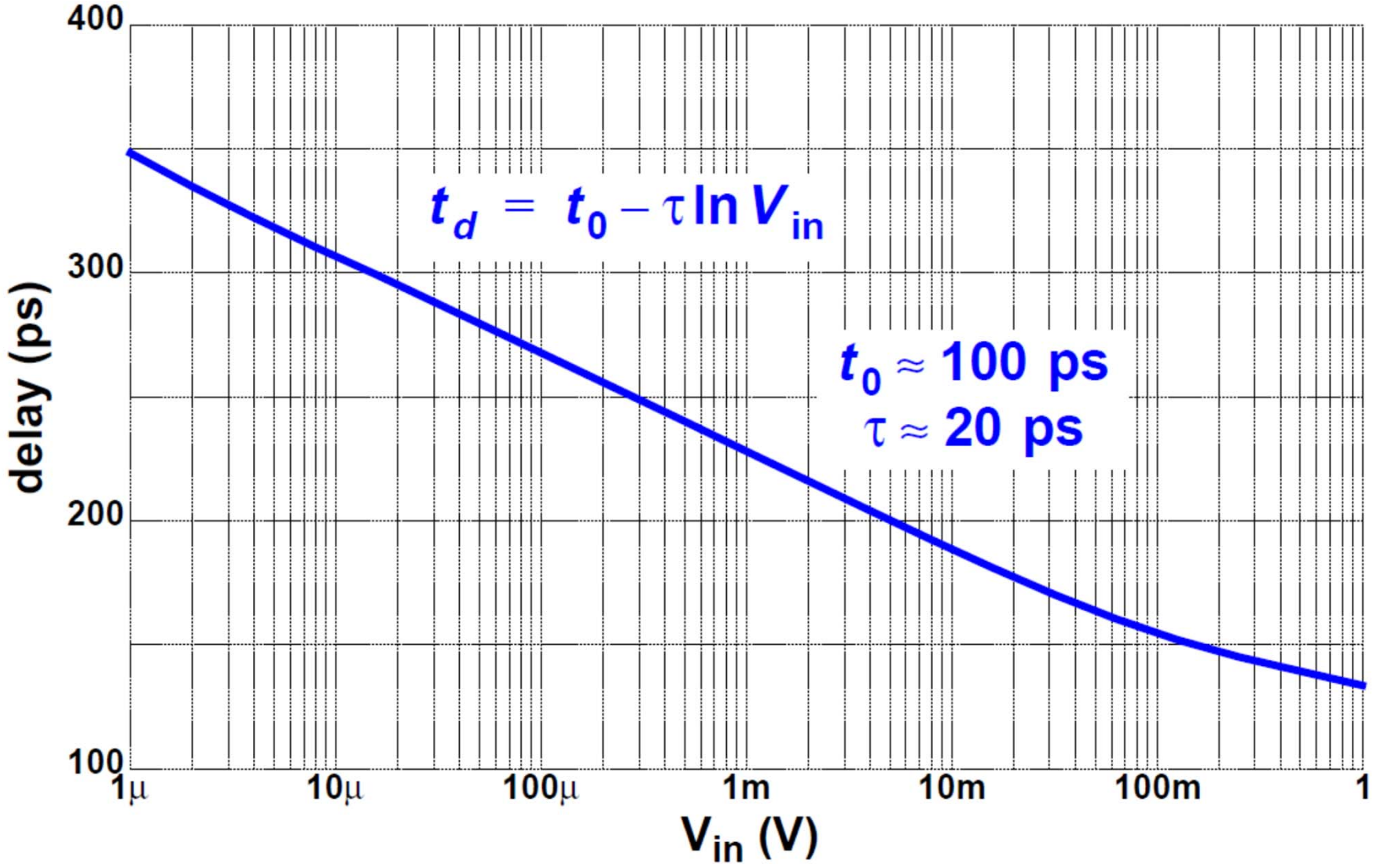
Better Design



Responses for Various V_{in}



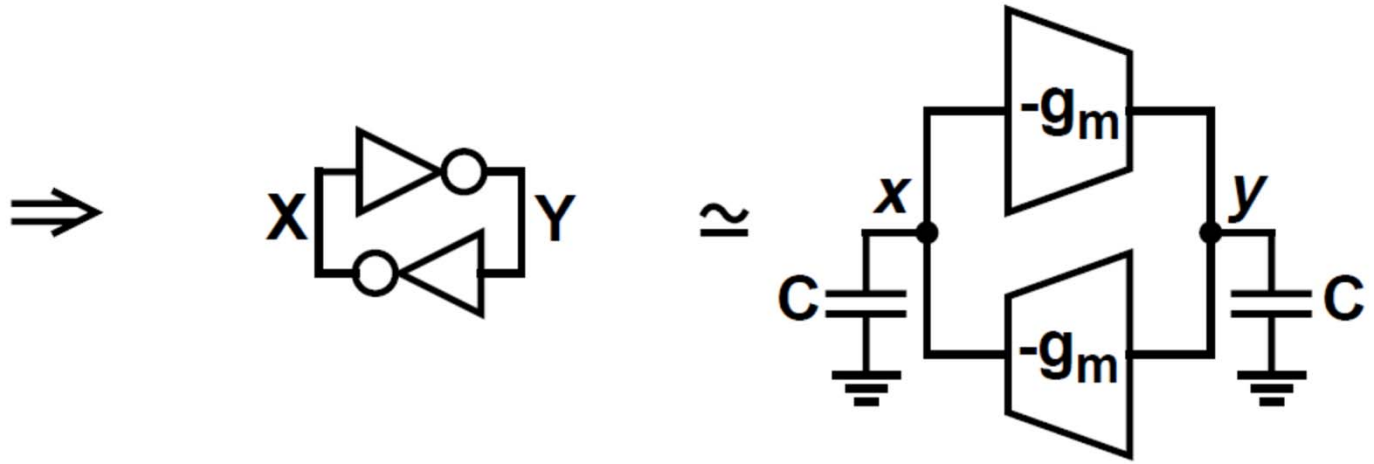
Delay vs V_{in}


400
300
200
100
delay (ps)
$t_d = t_0 - \tau \ln V_{in}$
$t_0 \approx 100$ ps
$\tau \approx 20$ ps
1µ
10µ
100µ
1m
10m
100m
1
V_{in} (V)

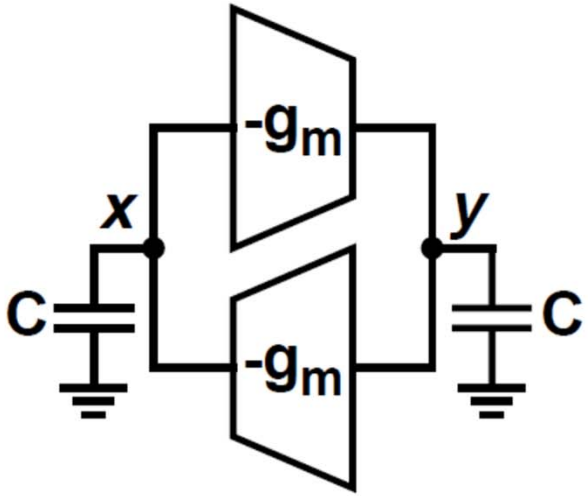
Latch Mode Dynamics

- For V_{in} near the trip point, an inverter is essentially just a transconductor:

- So near balance the comparator looks like this:



Small-Signal Analysis



$$C\dot{x} = -g_m y$$
$$C\dot{y} = -g_m x$$

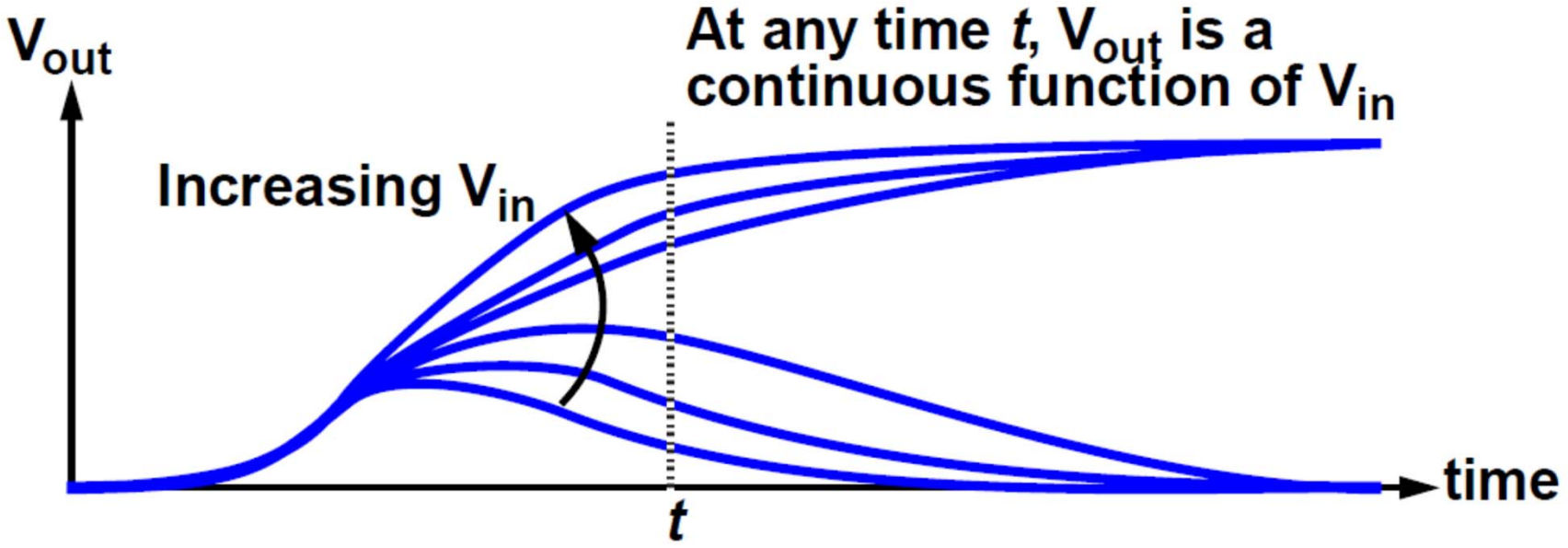
$$v_d = x - y$$
$$v_{cm} = \frac{x+y}{2}$$

$$C\dot{v}_d = g_m v_d \qquad C\dot{v}_{cm} = -g_m v_{cm}$$
$$v_d(t) = v_{d0} e^{t/\tau} \qquad v_{cm}(t) = v_{cm0} e^{-t/\tau}$$
$$\tau = \frac{C}{g_m}$$

- **Differential component grows exponentially**
- **CM component decays exponentially**

Metastability

- **Metastability is fundamentally unavoidable**
- **Assuming the universe is continuous and deterministic, a comparator can be unresolved for any length of time**



Probability of Error

$$P_E = P\{\text{not resolved by time } t\}$$

$$= P\left\{V_{in} < e^{-(t-t_0)/\tau}\right\}$$

- Take t_0 = 100ps and τ = 20ps
- Then for t = 500ps (1 GHz clock with a half-cycle between the comparator's clock and the clock of the subsequent latch),

$$P_E = P\{|V_{in}| < 2 \text{ nV}\}$$

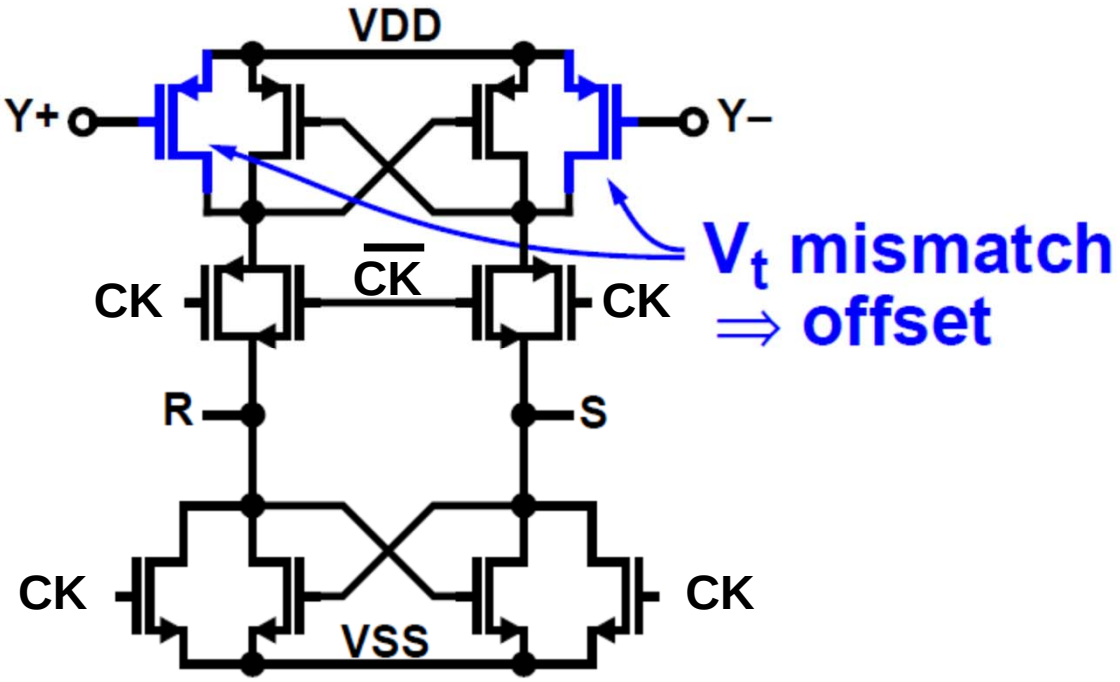
- Assuming V_{in} is uniformly distributed in [-0.5, +0.5] V, $P_E = 2 \times 10^{-9}$

  Metastability occurs twice a second!

Metastability Summary

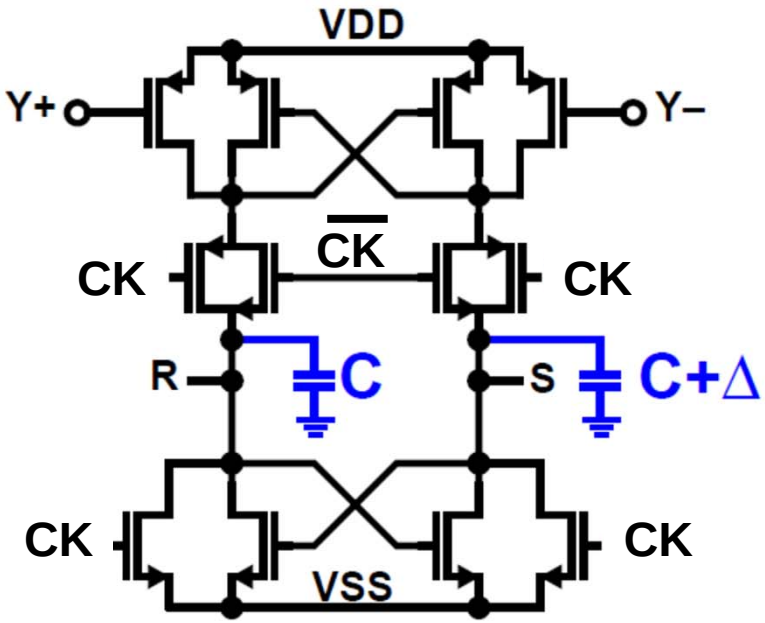
- **Metastability is unavoidable**
  - **All you can do is make τ small and give enough time for regeneration to make P_E small**
- **At best, metastability causes SNR degradation**
  - **At worst, it causes a system failure**
- **In Continuous-Time $\Delta\Sigma$ Lecture we will look at metastability further**
  - **Find SNR equation for a CT $\Delta\Sigma$ ADC**

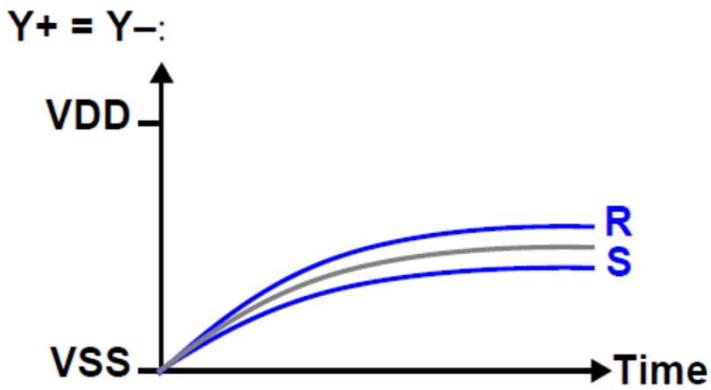
Offset



- **Sources of offset**
  - **Mismatch in the input differential pair**
  - **Mismatch in the regenerating devices**

Dynamic Offset

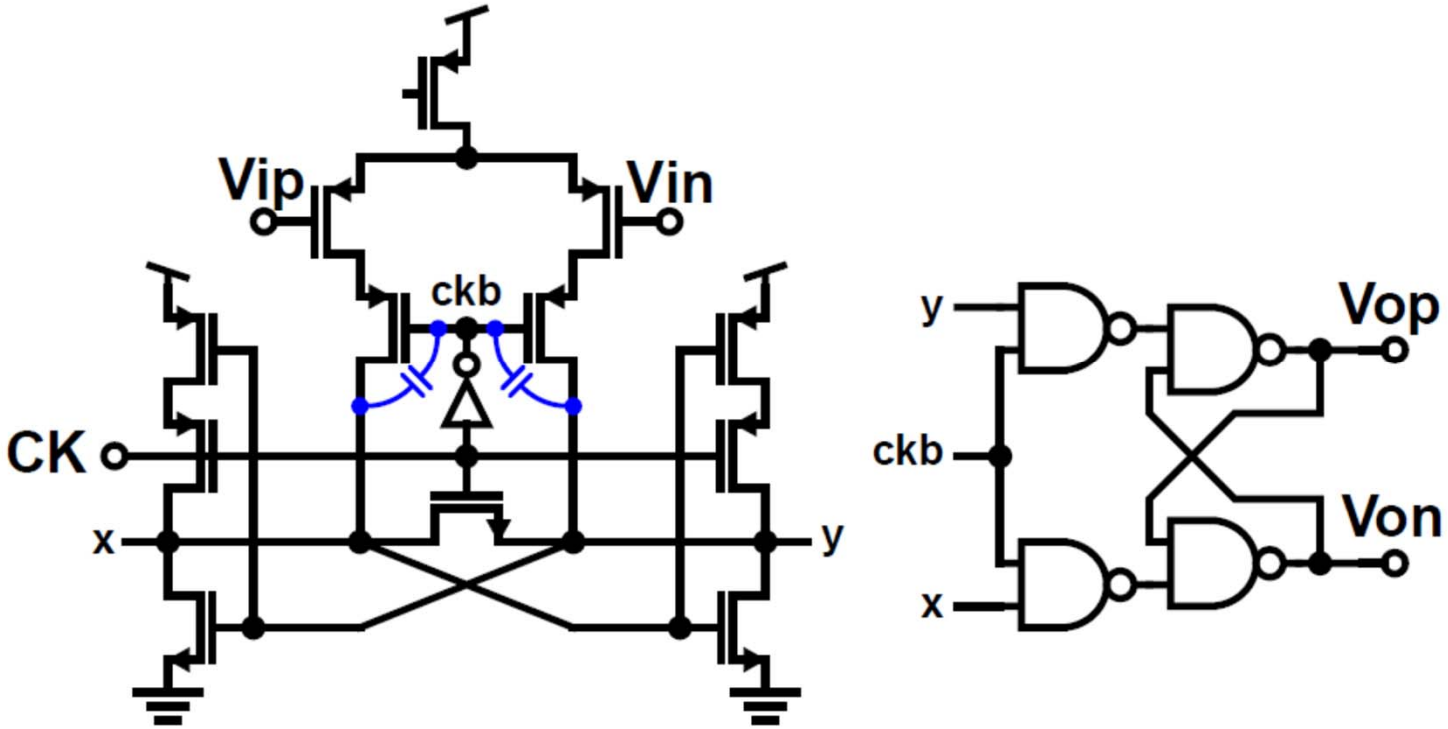




S rises more slowly than R
⇒ offset

- **Mismatched parasitic capacitance causes offset**
  - **20 mV/fF for this comparator**
- **We can fix this with better design**

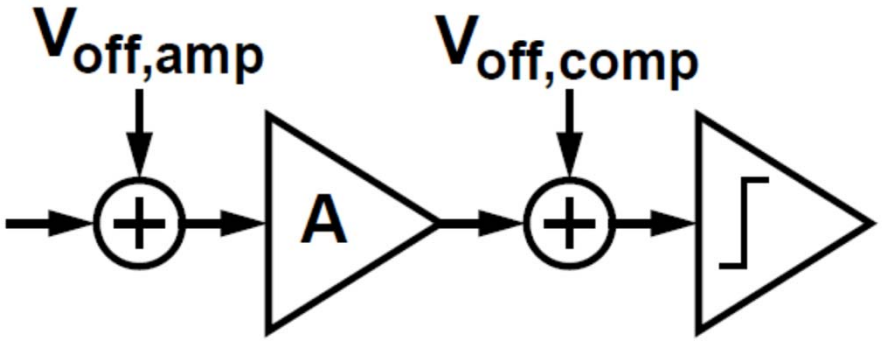
Improved Comparator



- **Reset when CK = 1, regenerates when CK = 0**
- **x & y don't step if biased properly**

  Mismatch in overlap capacitance still a problem

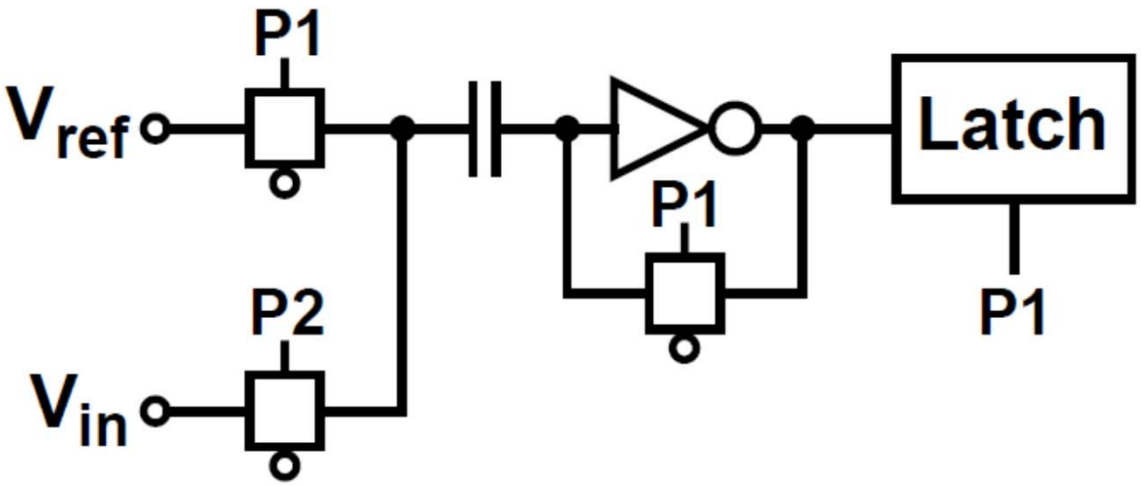
Reducing Offset with a Preamp



$$V_{off,tot} = V_{off,amp} + V_{off,comp}/A$$

- ☺ **Comparator offset is reduced by preamp gain**
  - **Amplifier offset dominates**
- ☺ **Amplifier also isolates driving stage from 'charge kickback'**
- ☹ **Amplifier bandwidth limits speed**

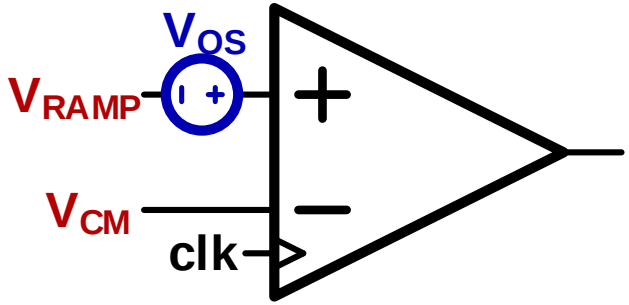
Auto-Zeroed SC Comparator



- During P1, the inverter/amplifier is biased at its threshold/offset voltage
- During P2, the difference between V_{in} and V_{ref} is amplified

Measuring Offset

- **In ideal schematic, differential comparator has no offset**
  - **Monte Carlo simulations will show offsets in comparator due to mismatch**
  - **Additional offsets will be seen in extracted layout (should be small with good layout)**



- **Traditional measurement**
  - **In a given MC trial, ramp the input across the threshold of the comparator, crossing point is the offset**
  - **Requires ~50-100 transient trials, each one ~10 cycles**

Measuring Offset

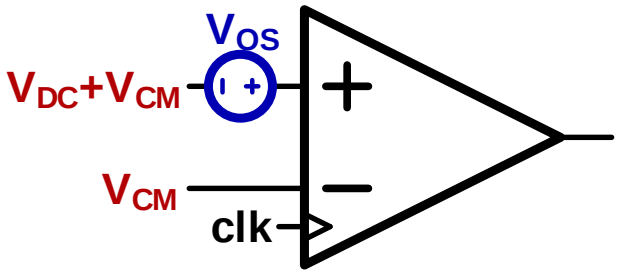
- **Alternative Method**

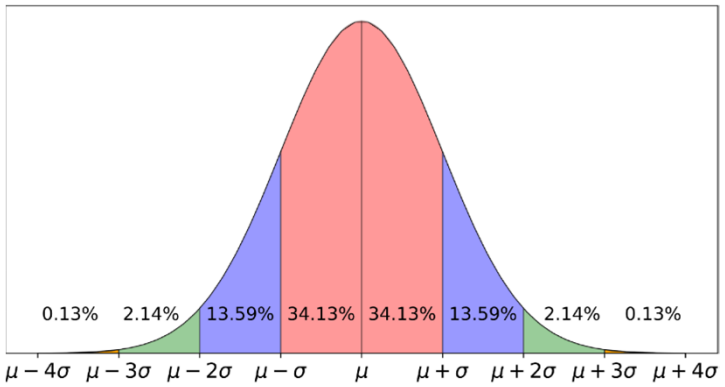
  In a single Monte Carlo trial, set a DC input voltage and run the transient for a single cycle

  Repeat ~100 transient single cycle MC trials

  Determine percentage of sims that output +1 or -1

  Assuming normal distribution, offset can be determined





- **Example: DC voltage = 1mV**

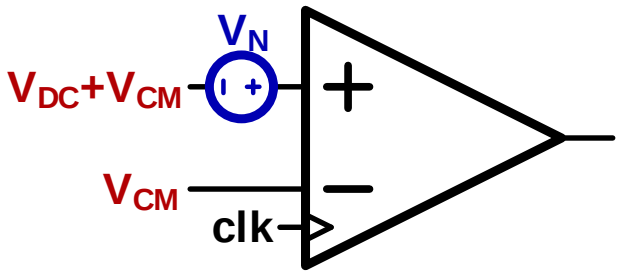
  84% output '+1',16% output '-1' → Offset is 1mV

  Wolfram Alpha: -inverse erfc(2*0.84)*sqrt(2)

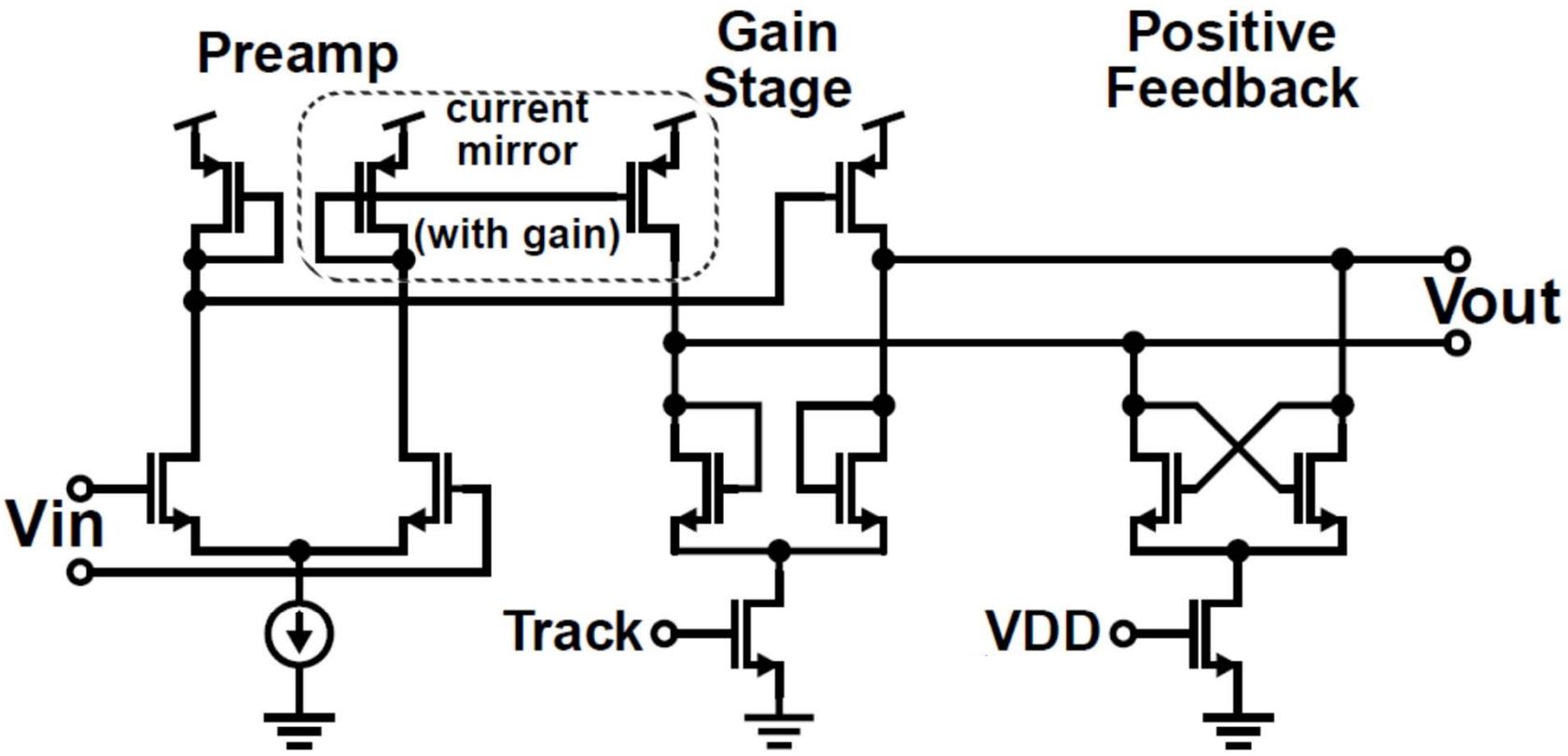
Measuring Noise

- **Output is latched, a traditional AC noise sim is insufficient**
- **Simulate using Offset measurement technique**
  - **In a given transient noise simulation, set a DC input voltage and run the transient for a single cycle**
  - **Repeat ~100 transient noise single-cycle simulations**
  - **Determine percentage of sims that output +1 or -1**
  - **Assuming normal distribution, offset can be determined**

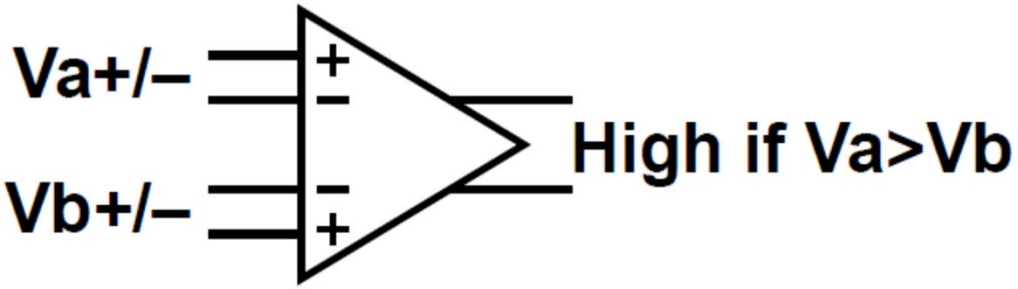
[Razavi 2015]



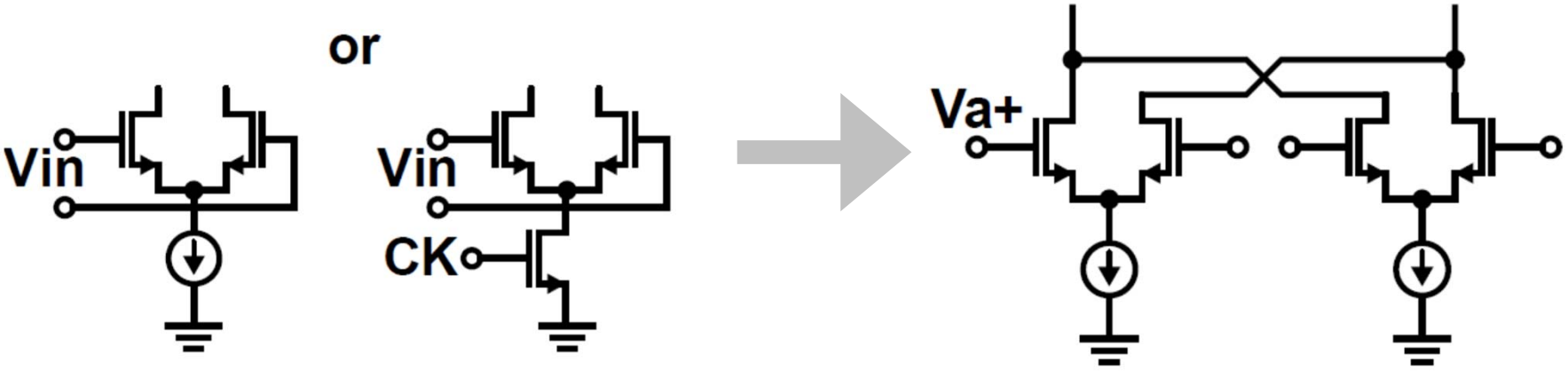
Comparator with Preamp



Dual-Difference Comparator

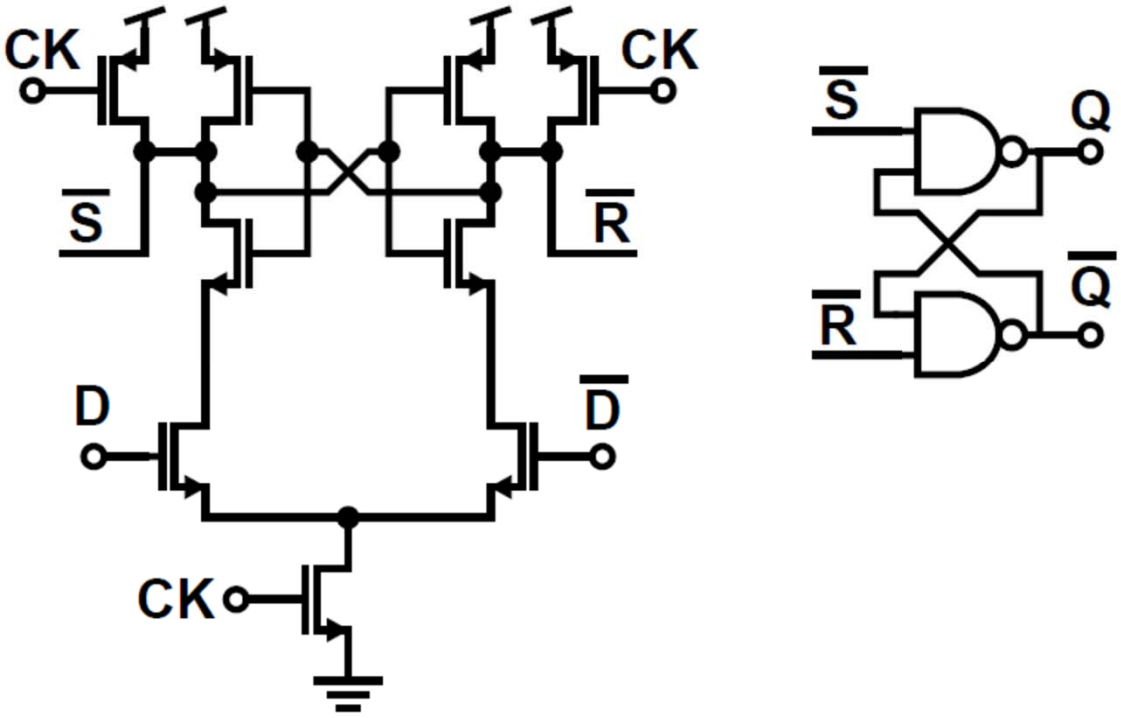


- **In any of our comparator circuits, make the following replacement**



- **Where should Va- go?**

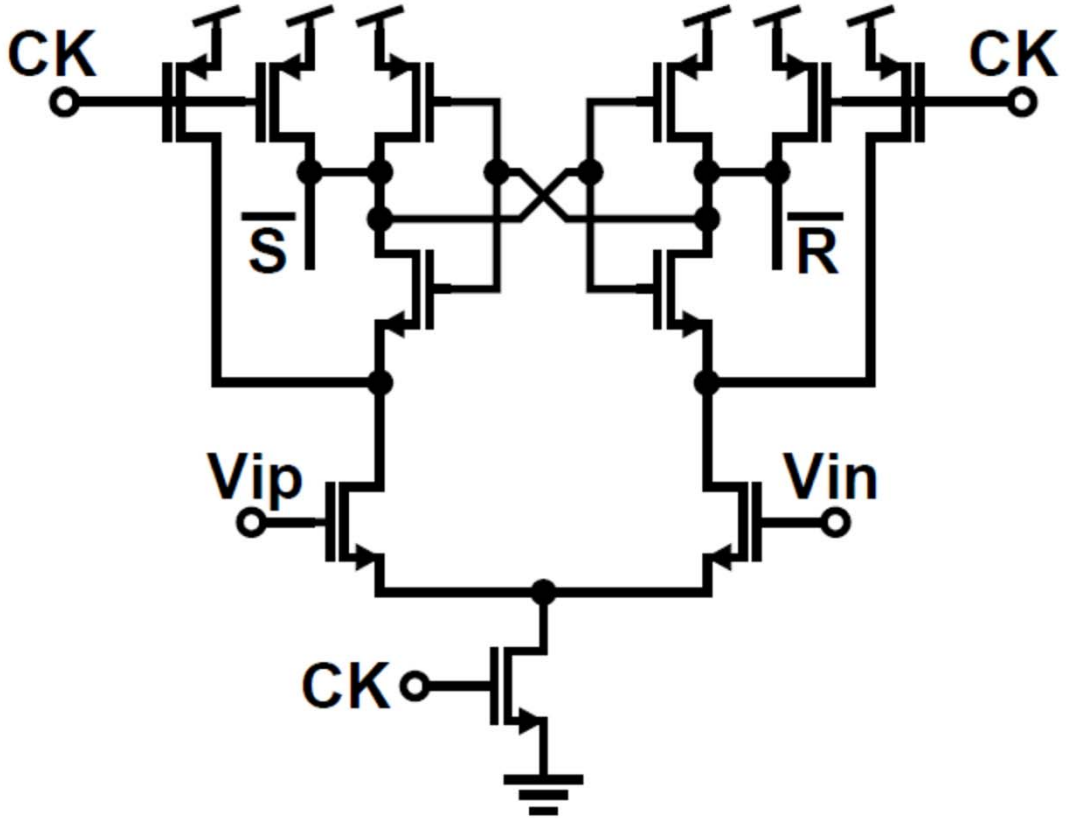
StrongArm Latch

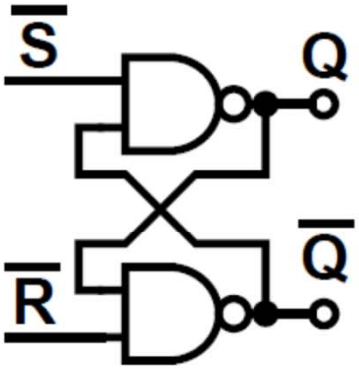


- **No static current**
- **Can be used as a comparator**

  Note that input CM voltage defines the bias point during regeneration

StrongArm Latch



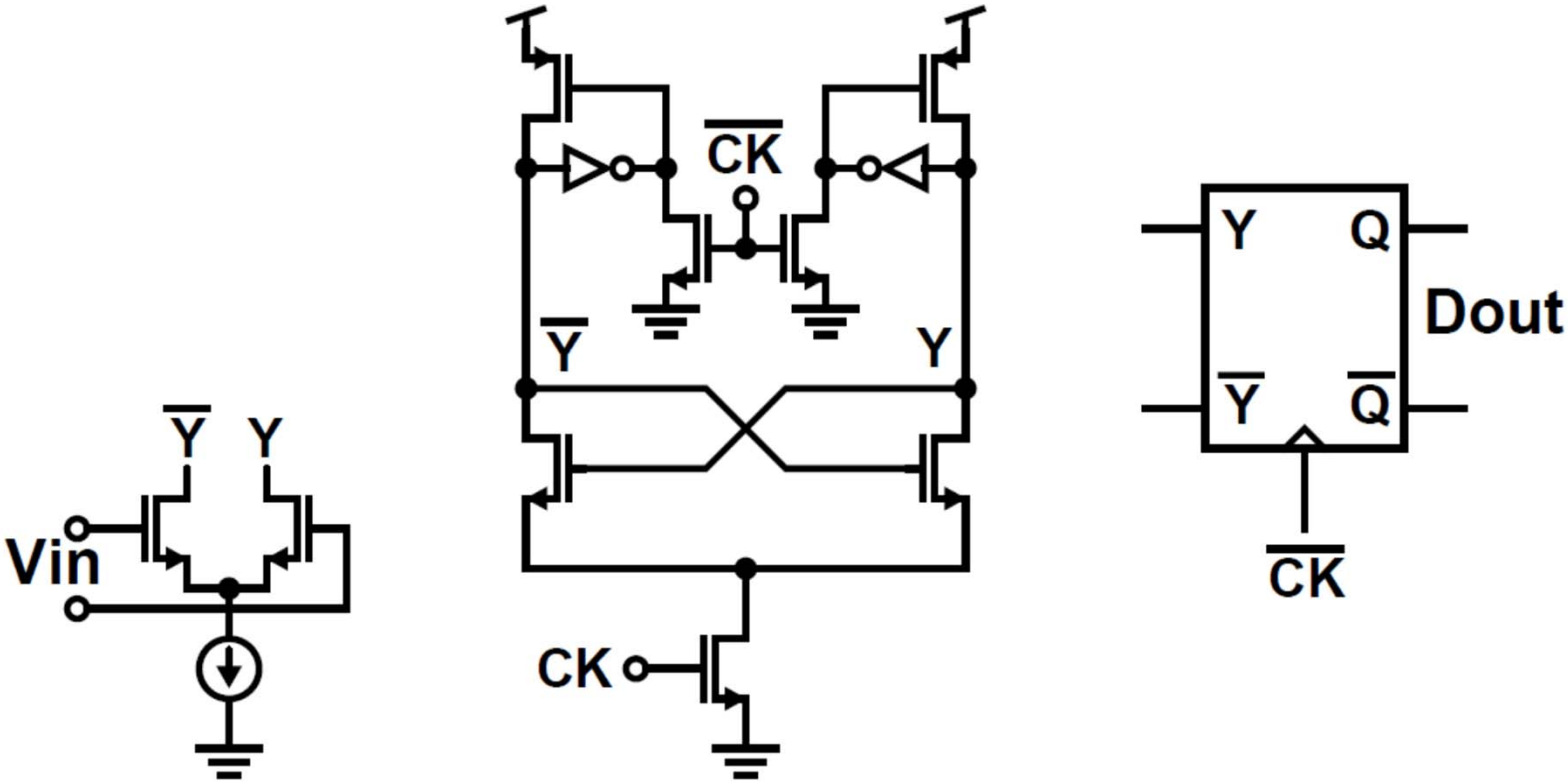


- **Well-defined initial state → less hysteresis**

  [2014 Abidi] 'Understanding the Regenerative…'

  [2015 Razavi], 'The StrongARM Latch'

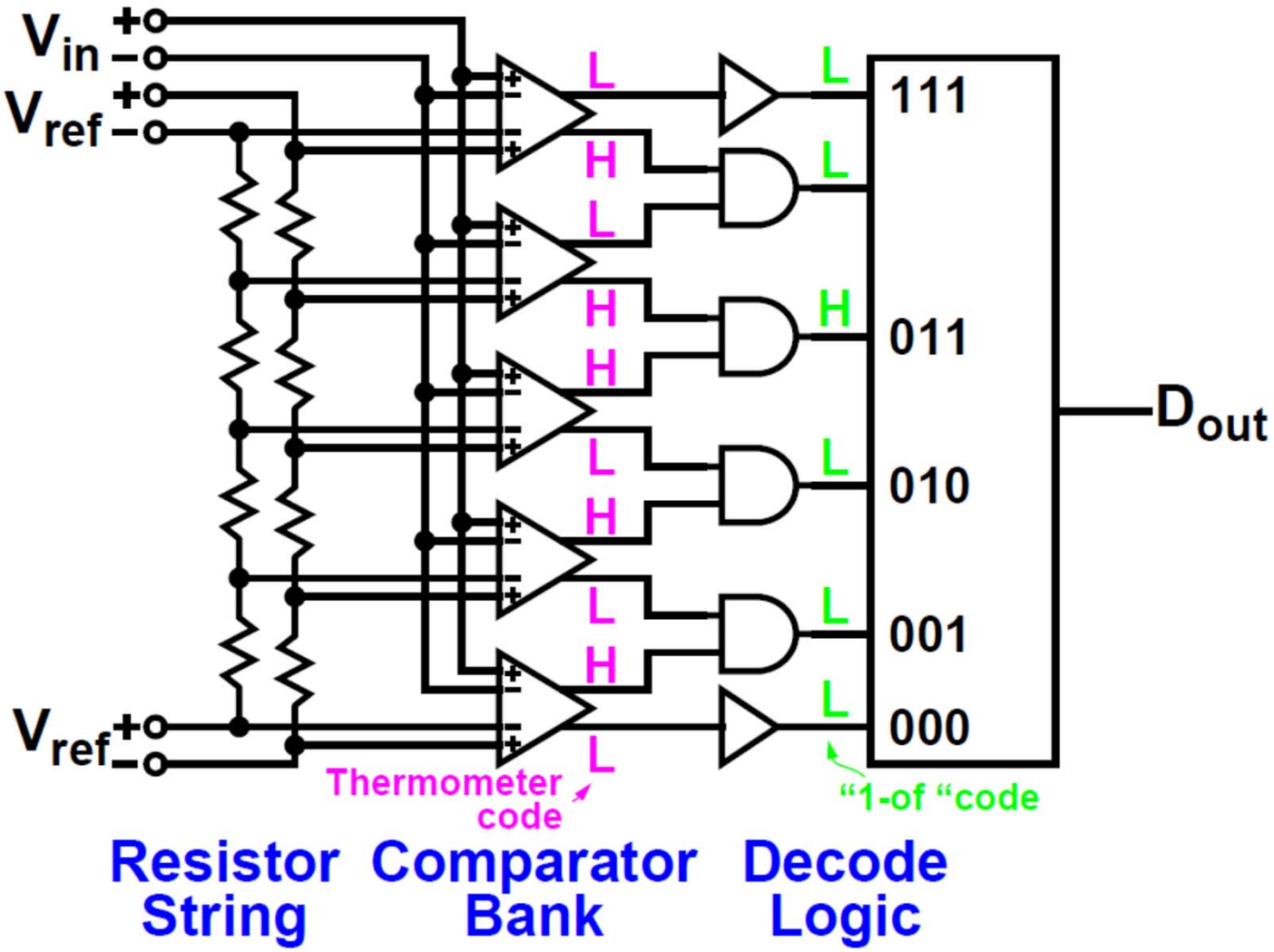
Yang's High-Speed Comparator



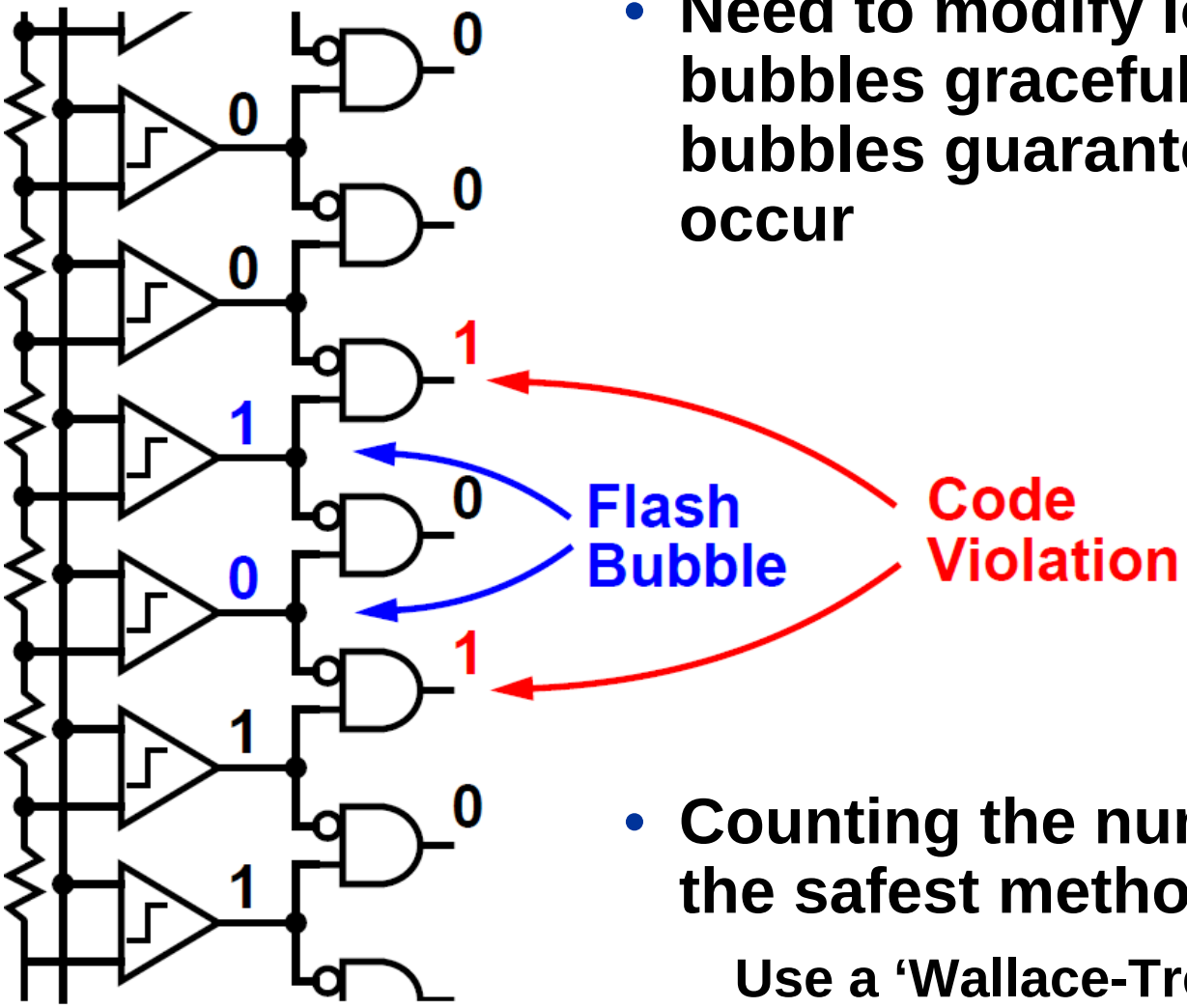
- τ_{nom} = 6ps in 65nm CMOS

  Used in a CTΔΣ ADC clocked at 4 GHz [Shibata2012]

Flash ADC


Vin
Vref
Vref
L
H
L
H
H
L
H
L
H
L
111
011
010
001
000
Dout
Thermometer code
"1-of "code
Resistor String
Comparator Bank
Decode Logic

Flash Bubbles

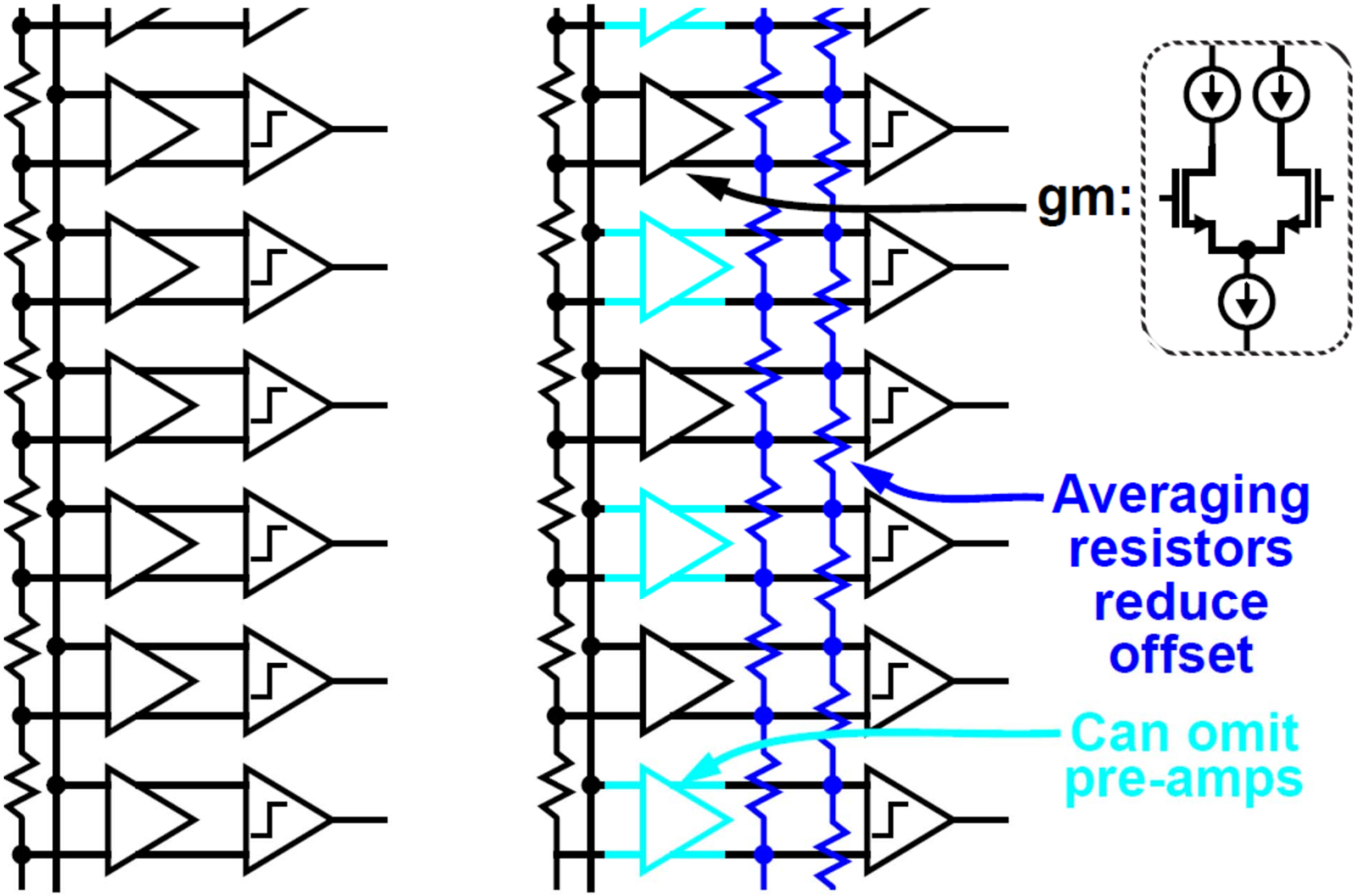


- Need to modify logic to handle bubbles gracefully unless bubbles guaranteed to not occur

- Counting the number of 1s is the safest method

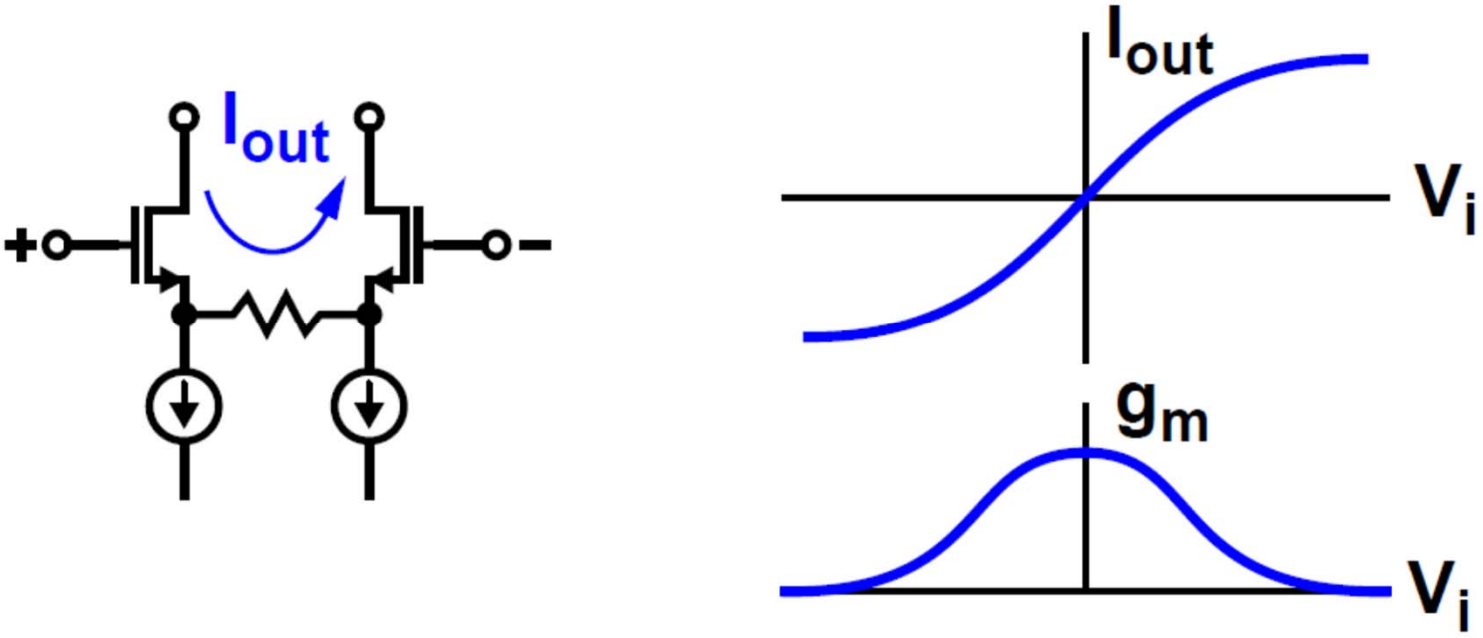
  Use a ‘Wallace-Tree Adder’

Averaging and Interpolation



Circuit of the Day: Linear Transconductors

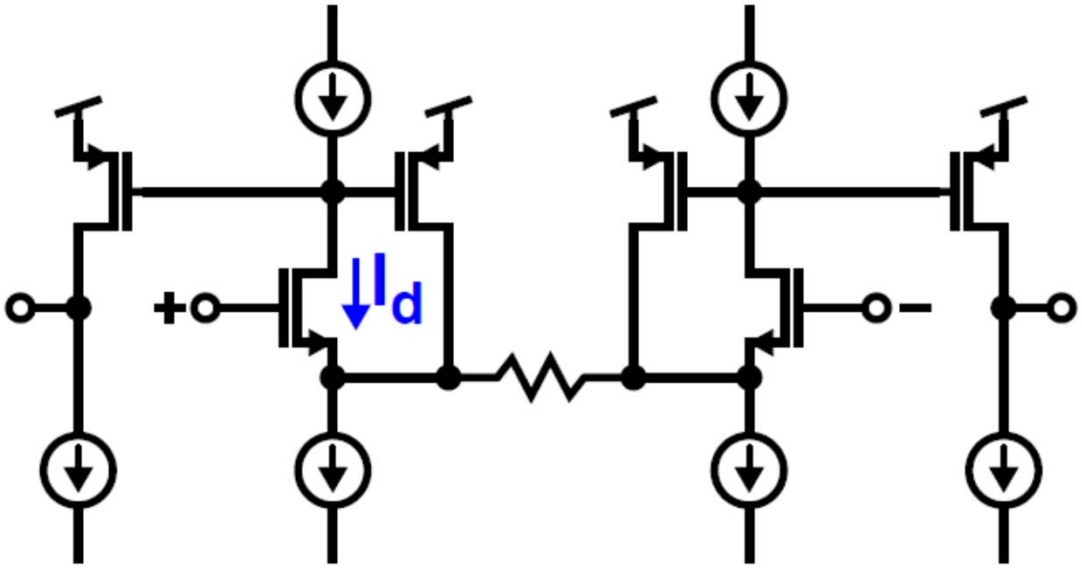
- **Degenerated Differential Pair**



- **V_{gs} varies nonlinearly with I_{out}**
  - **g_m is nonlinear**
  - **Increase I_{bias} to improve linearity**

Linear Transconductors

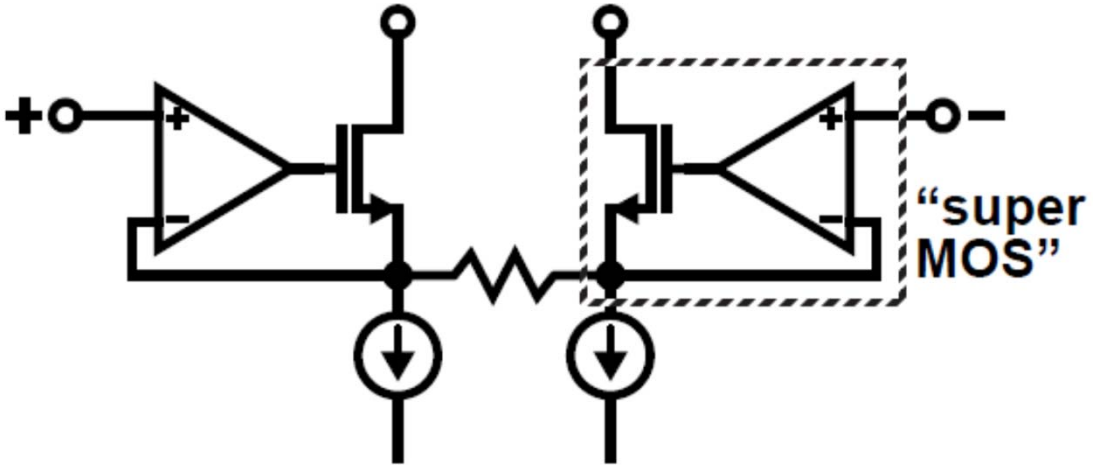
- **Force Constant V_{gs}**



- **I_d constant → V_{gs} constant**
- **Linearity dependent on current-mirror linearity**

Linear Transconductors

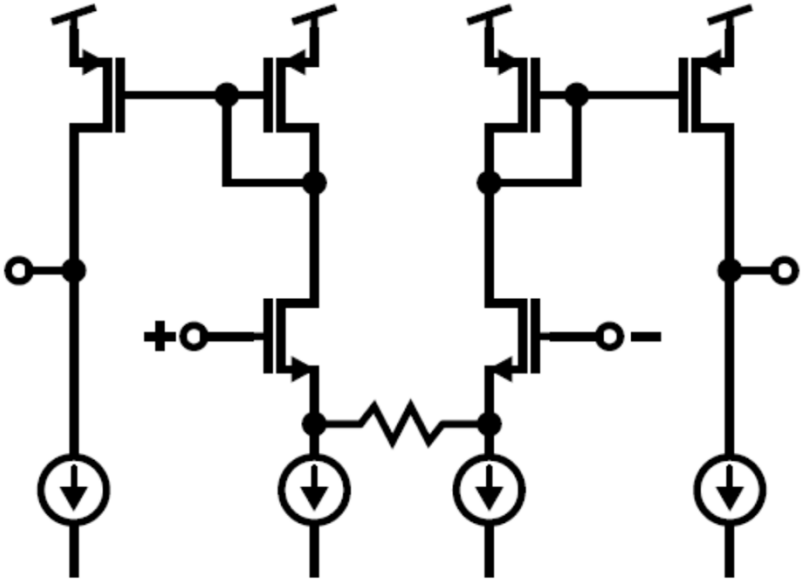
- **Add Op Amps**



- **Linearity limited only by op amp gain and BW**
- **High output resistance**
- **Output compliance depends on input swing**

Linear Transconductors

- **Mirror the Output Current**

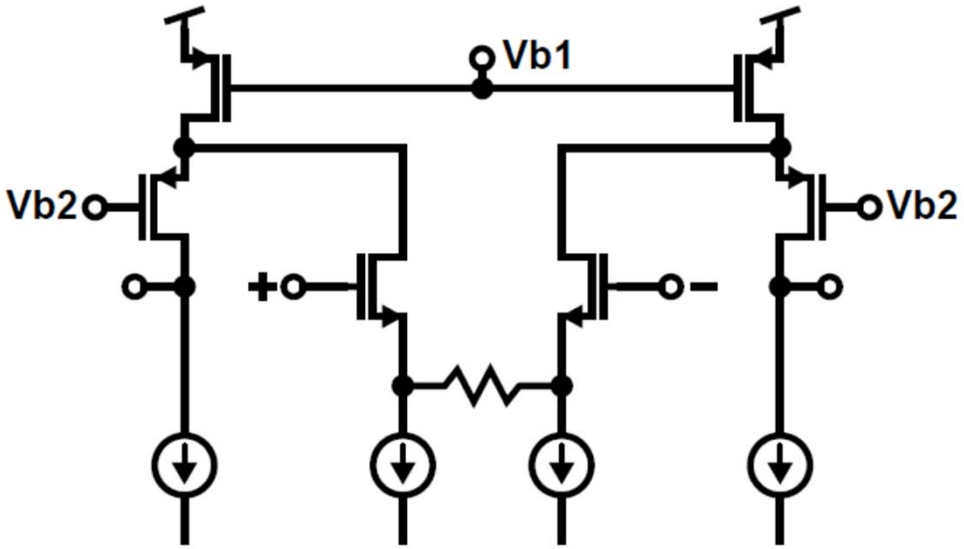


☺ **Output compliance is $VDD - 2V_{dsat}$**

☹ **Top of differential pair at $VDD - V_{gs}$**

Linear Transconductance

- **Fold the Output Current**



☺ **Increased headroom for differential pair**

☺ **Increased output resistance**

☹ **Extra cascode in output branch**

Homework #3 (Due Feb 11)

- **Read 'The StrongARM Latch' [Razavi 2015]**
  1. **Design a version of this comparator including the subsequent RS latch**
     A. **Make sure your schematic is complete and legible**
  2. **State the power consumption at F_{ck} = 100 MHz, regeneration time constant (τ), t_0, rms noise and the mean and standard deviation of the offset**
     A. **Use nominal PTV**
     B. **Summarize the specifications in a table**
     C. **Include both hand calculations and simulation results**

What You Learned Today

- **Example Comparator Circuit**
- **Comparator metrics**
  - **Metastability and regeneration time constant**
  - **Offset measurement**
  - **Noise measurement**
- **Flash ADC**