Lecture 2
MOD*N* and the ΔΣ Toolbox

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Lecture Plan

Date	Lecture (Wednesday 2-4pm)		Reference	Homework
2020-01-07	1	MOD1 & MOD2	PST 2, 3, A	1: Matlab MOD1&2
2020-01-14	2	MOD*N* + ΔΣ Toolbox	PST 4, B	2: ΔΣ Toolbox
2020-01-21	3	SC Circuits	R 12, CCJM 14	
2020-01-28	4	Comparator & Flash ADC	CCJM 10	3: Comparator
2020-02-04	5	Example Design 1	PST 7, CCJM 14	
2020-02-11	6	Example Design 2	CCJM 18	4: SC MOD2
2020-02-18	Reading Week / ISSCC			
2020-02-25	7	Amplifier Design 1		Project
2020-03-03	8	Amplifier Design 2		
2020-03-10	9	Noise in SC Circuits		
2020-03-17	10	Nyquist-Rate ADCs	CCJM 15, 17	
2020-03-24	11	Mismatch & MM-Shaping	PST 6	
2020-03-31	12	Continuous-Time ΔΣ	PST 8	
2020-04-07	Exam			
2020-04-21	Project Presentation (Project Report Due at start of class)			

Circuit of the Day: Level Translator

- VDD1 > VDD2, e.g.

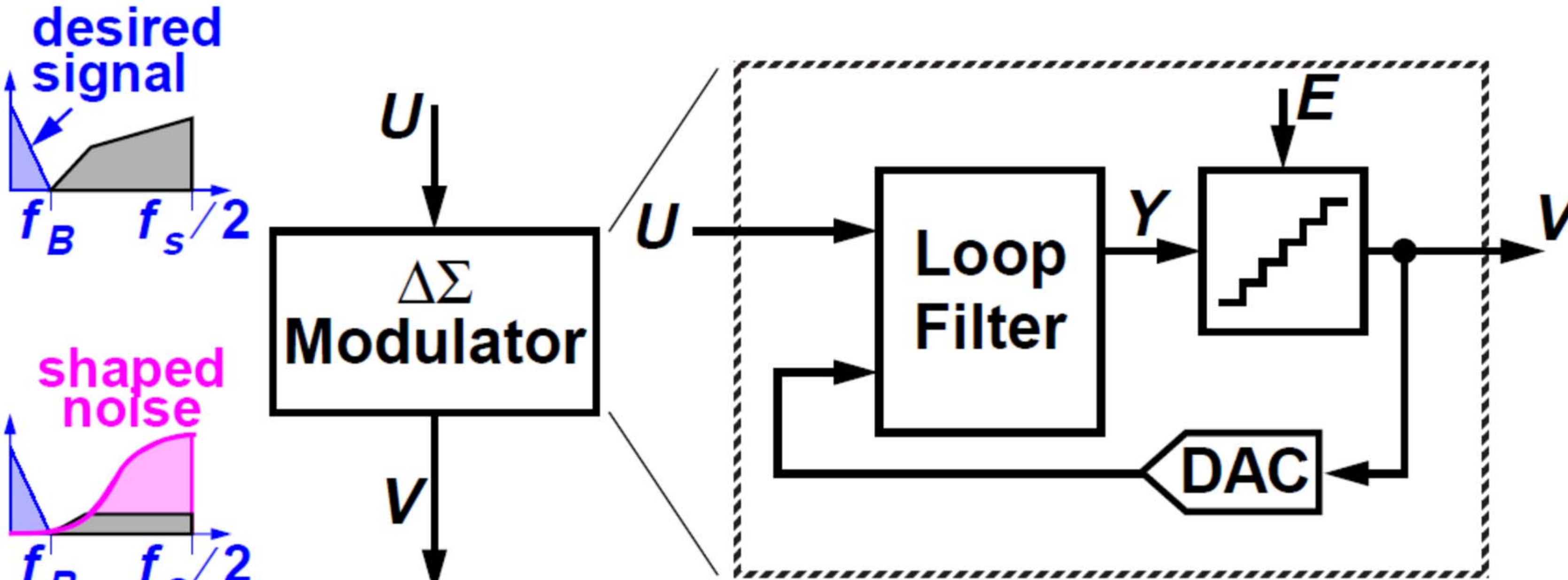
- VDD1 < VDD2, e.g.

- Constraints
  - CMOS, 1-V and 3-V devices, no static current

What you will learn…

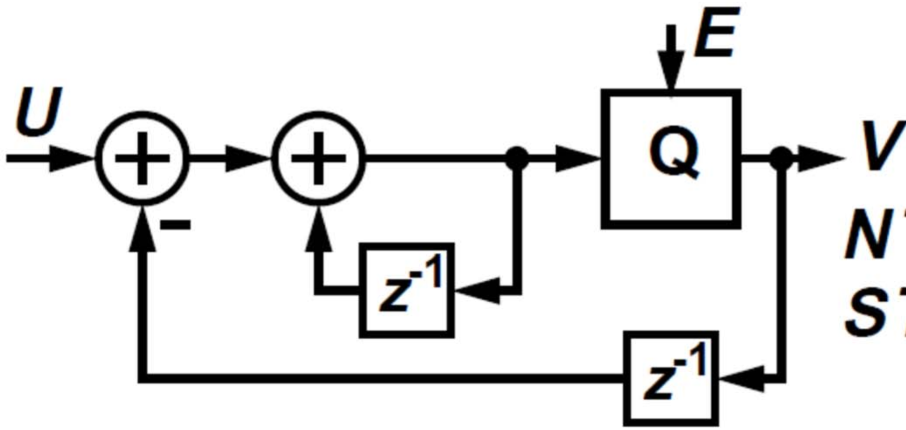
- N^{th}-order modulator (MODN)
- High-level design with the ΔΣ Toolbox

Review: A ΔΣ ADC System

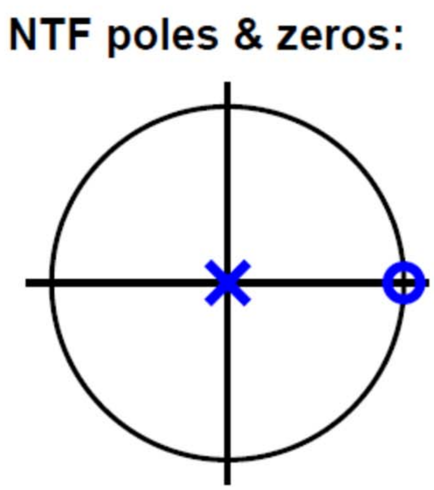


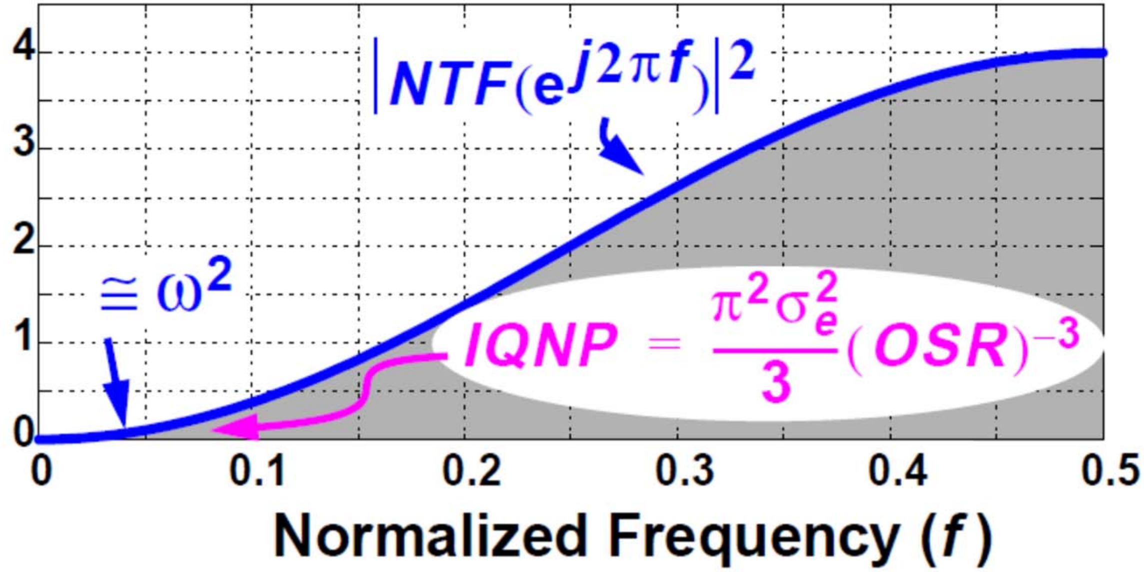
$$V(z) = STF(z)U(z) + NTF(z)E(z)$$

$STF(z)$: signal transfer function
$NTF(z)$: noise transfer function
$E(z)$: quantization error

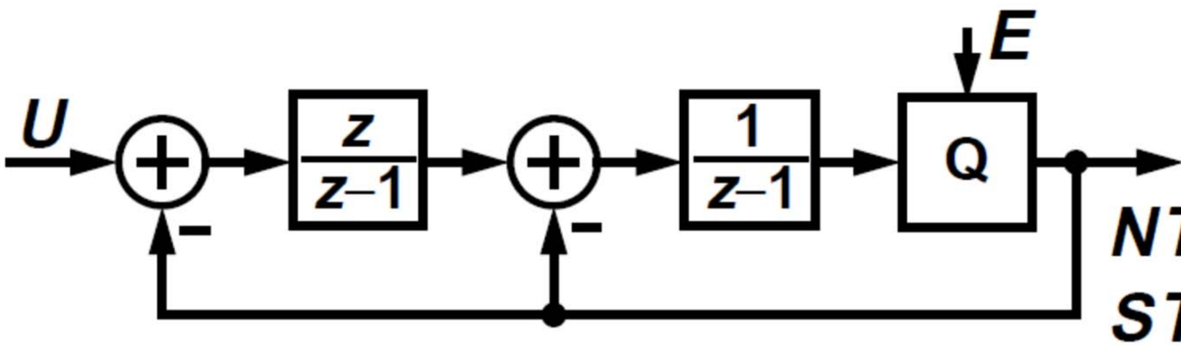


$$NTF(z) = (1 - z^{-1})$$
$$STF(z) = 1$$



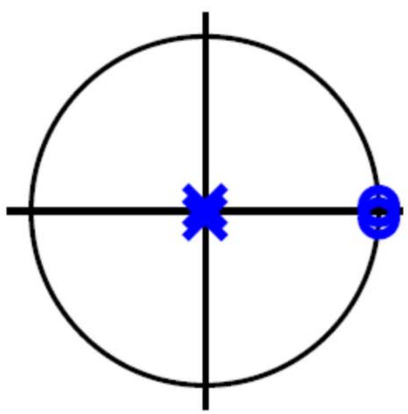


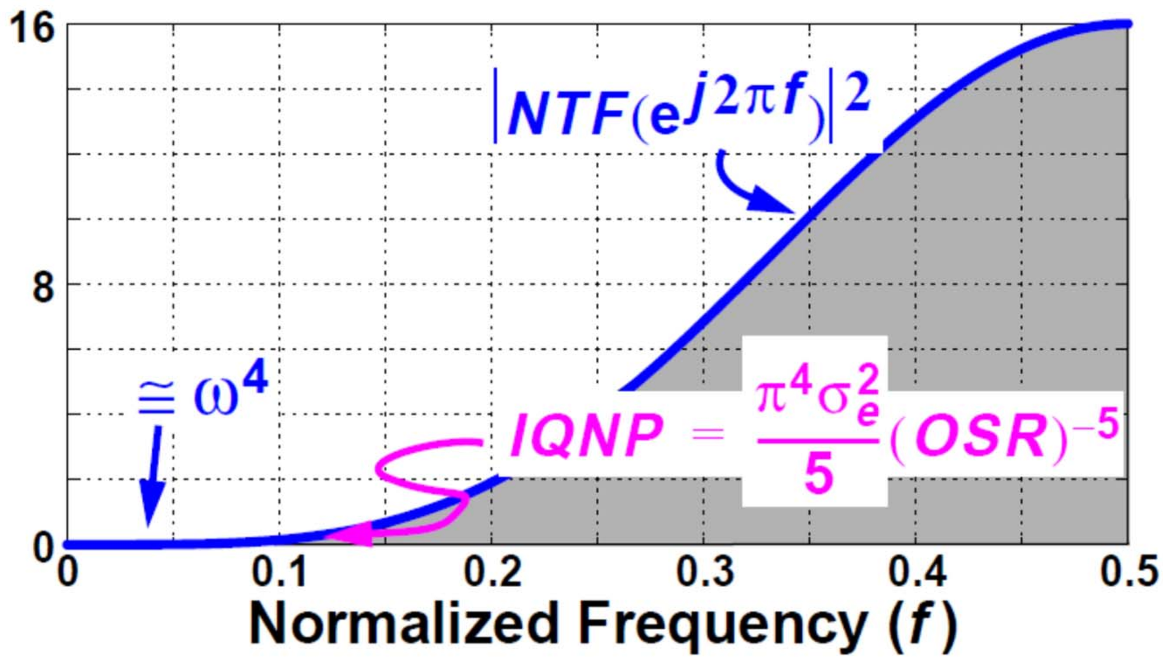
Review: MOD2



$$NTF(z) = (1 - z^{-1})^2$$
$$STF(z) = z^{-1}$$

NTF poles & zeros:

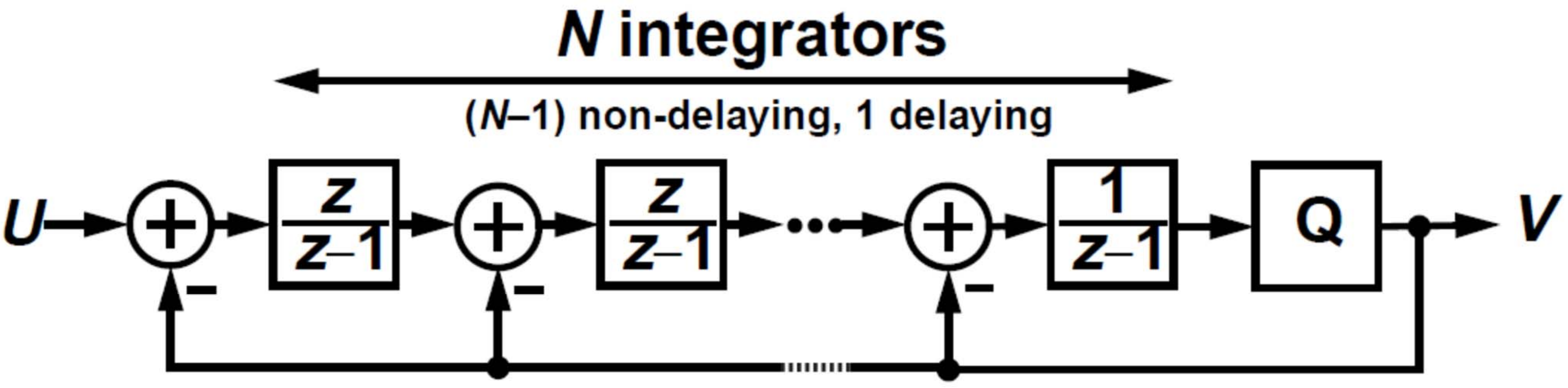




Review Summary

- **ΔΣ works by spectrally separating the quantization noise from the signal**
  - **Requires oversampling $OSR \equiv f_s/2f_B$**
  - **Achieved by the use of *filtering and feedback***
- **A binary DAC is *inherently linear*, and thus a binary ΔΣ modulator is too**
- **MOD1-CT has *inherent anti-aliasing***
- **MOD1 has $NTF(z) = 1 - z^{-1}$**
  - **Arbitrary accuracy for DC inputs**
  - **9 dB/octave SQNR-OSR trade-off**
- **MOD2 has $NTF(z) = (1 - z^{-1})^2$**
  - **15 dB/octave SQNR-OSR trade-off**

MOD*N*

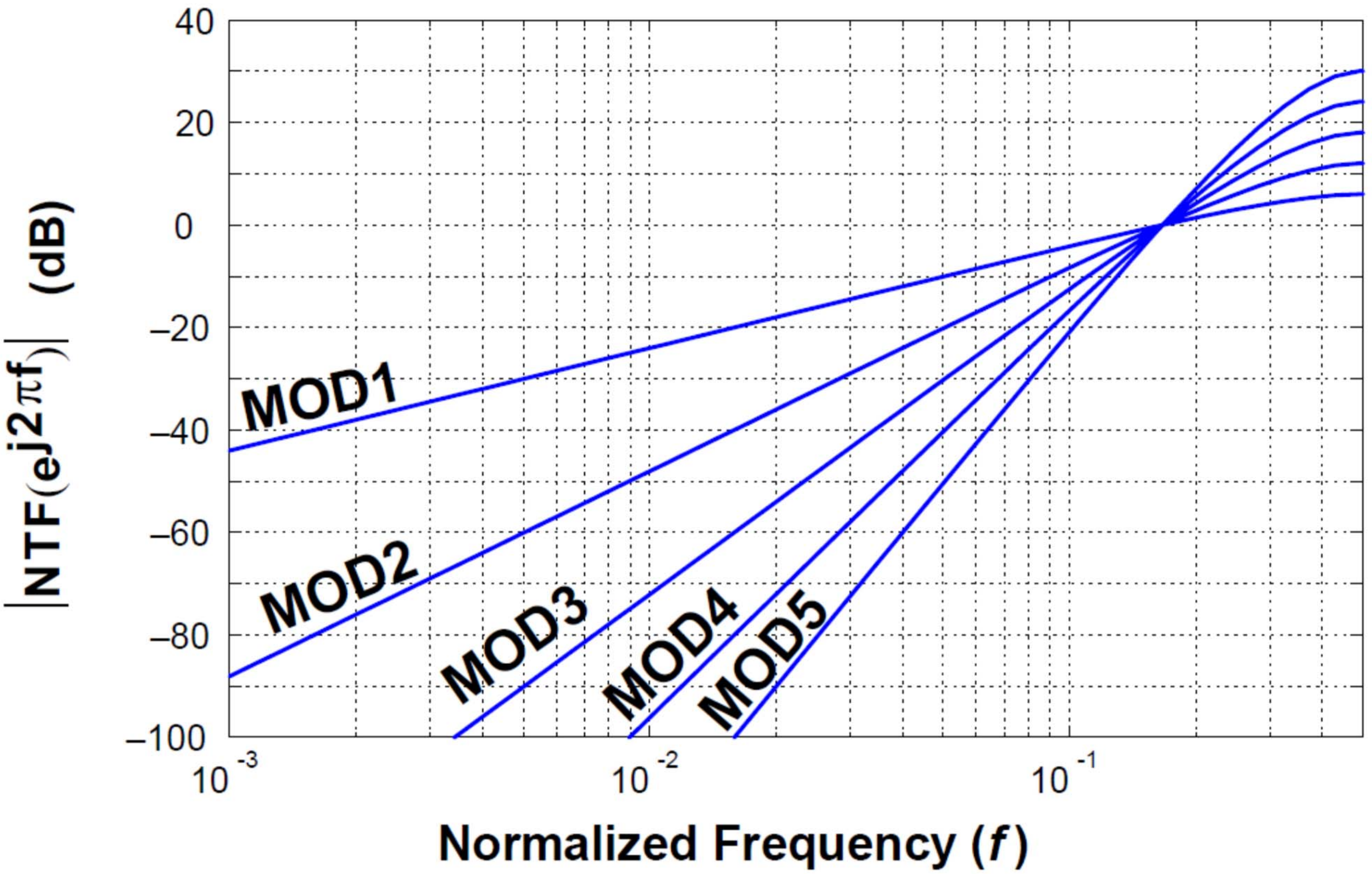


$$STF(z) = z^{-1}$$

$$NTF(z) = (1 - z^{-1})^N$$

- **MOD*N*'s NTF is the *N*th power of MOD1's NTF**

NTF Comparison



Predicted Performance

- **In-band quantization noise power**

$$IQNP = \int_0^{0.5/OSR} \left|NTF(e^{j2\pi f})\right|^2 \cdot S_{ee}(f)df$$

$$\approx \int_0^{0.5/OSR} (2\pi f)^{2N} \cdot 2\sigma_e^2 df$$

$$= \frac{\pi^{2N}}{(2N+1)OSR^{2N+1}}\sigma_e^2$$

- **Quantization noise drops as (2*N*+1)th power of OSR**
  - **(6N+3) dB/octave SQNR-OSR trade-off**

NTF Zero Optimization

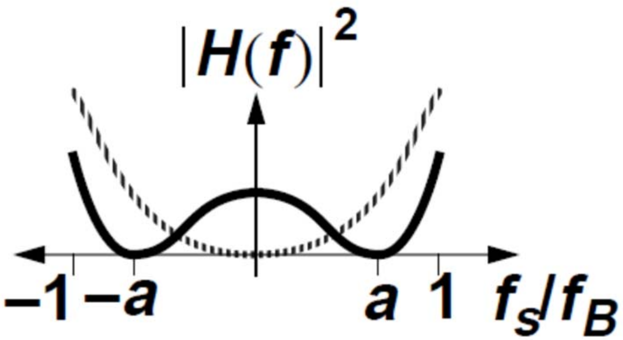
- **Improve NTF Performance by minimizing the integral of $|NTF|^2$ over the passband**
  - **Normalize passband edge to 1 for ease of calculation**
  - **Need to find the a_i which minimizes the integral**

$$\int_{-1}^{1}(x^2 - a_1^2)^2 dx\,, N = 2$$

$$\int_{-1}^{1}x^2(x^2 - a_1^2)^2 dx\,, N = 3$$

$$\int_{-1}^{1}(x^2 - a_1^2)^2(x^2 - a_2^2)^2 dx\,, N = 4$$

$$\vdots$$



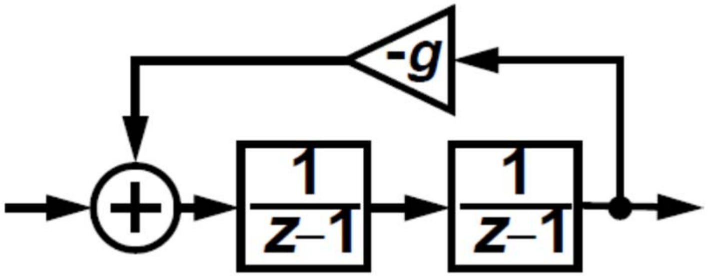
Solutions Up To Order = 8

Order	Optimal Zero Placement Relative to f_B	SQNR Improvement
1	0	0 dB
2	$\pm 1/\sqrt{3}$	3.5 dB
3	$0, \pm\sqrt{3/5}$	8 dB
4	$\pm\sqrt{3/7 \pm \sqrt{(3/7)^2 - 3/35}}$	13 dB
5	$0, \pm\sqrt{5/9 \pm \sqrt{(5/9)^2 - 5/21}}$	18 dB
6	$\pm 0.23862, \pm 0.66121, \pm 0.93247$	23 dB
7	$0, \pm 0.40585, \pm 0.74153, \pm 0.94911$	28 dB
8	$\pm 0.18343, \pm 0.52553, \pm 0.79667, \pm 0.96029$	34 dB

Topological Implication

- **Feedback around pairs of integrators:**

2 Delaying Integrators



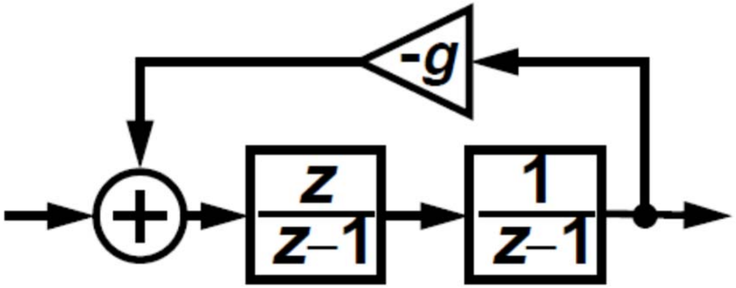
Poles are the roots of

$$1 + g\left(\frac{1}{z-1}\right)^2 = 0$$

i.e. $z = 1 \pm j\sqrt{g}$

Not quite on the unit circle, but fairly close if *g* << 1.

Non-delaying + Delaying Integrators (LDI Loop)



Poles are the roots of

$$1 + \frac{gz}{(z-1)^2} = 0$$

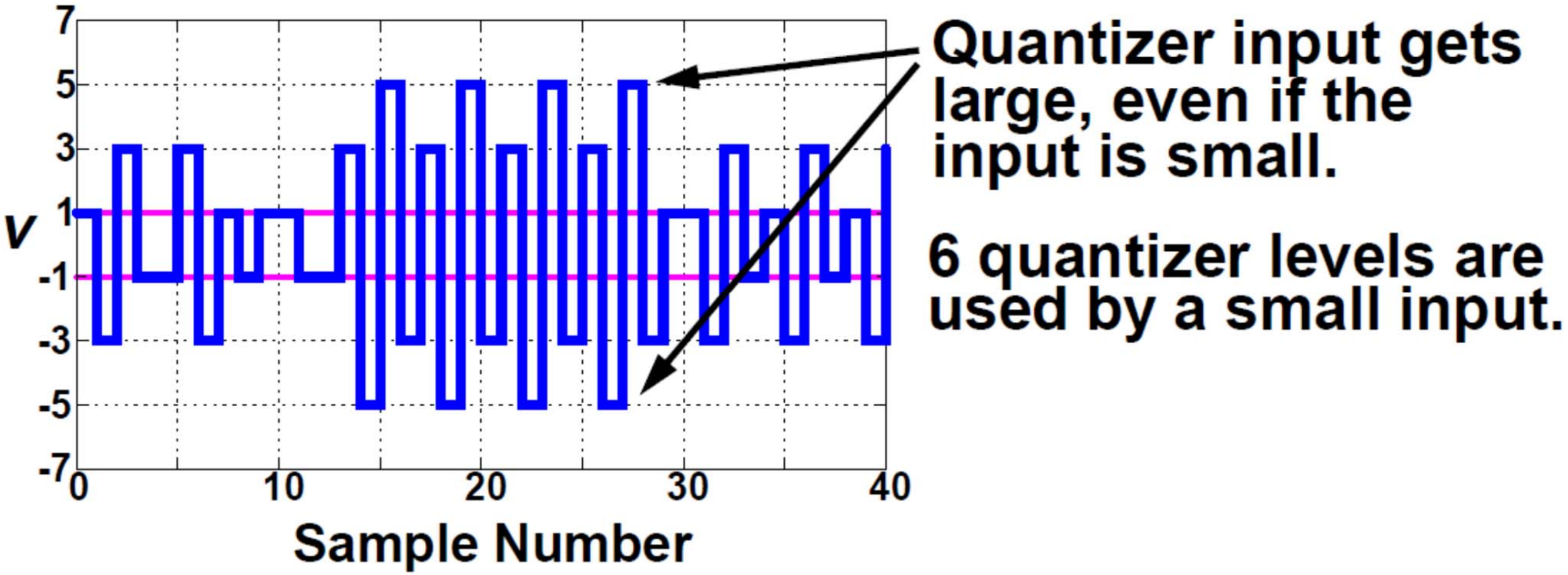
i.e. $z = e^{\pm j\theta}, \cos\theta = 1 - g/2$

Precisely on the unit circle, regardless of the value of *g*.

Problem with Single-Bit

- **A High-Order Modulator wants a Multi-bit Quantizer**

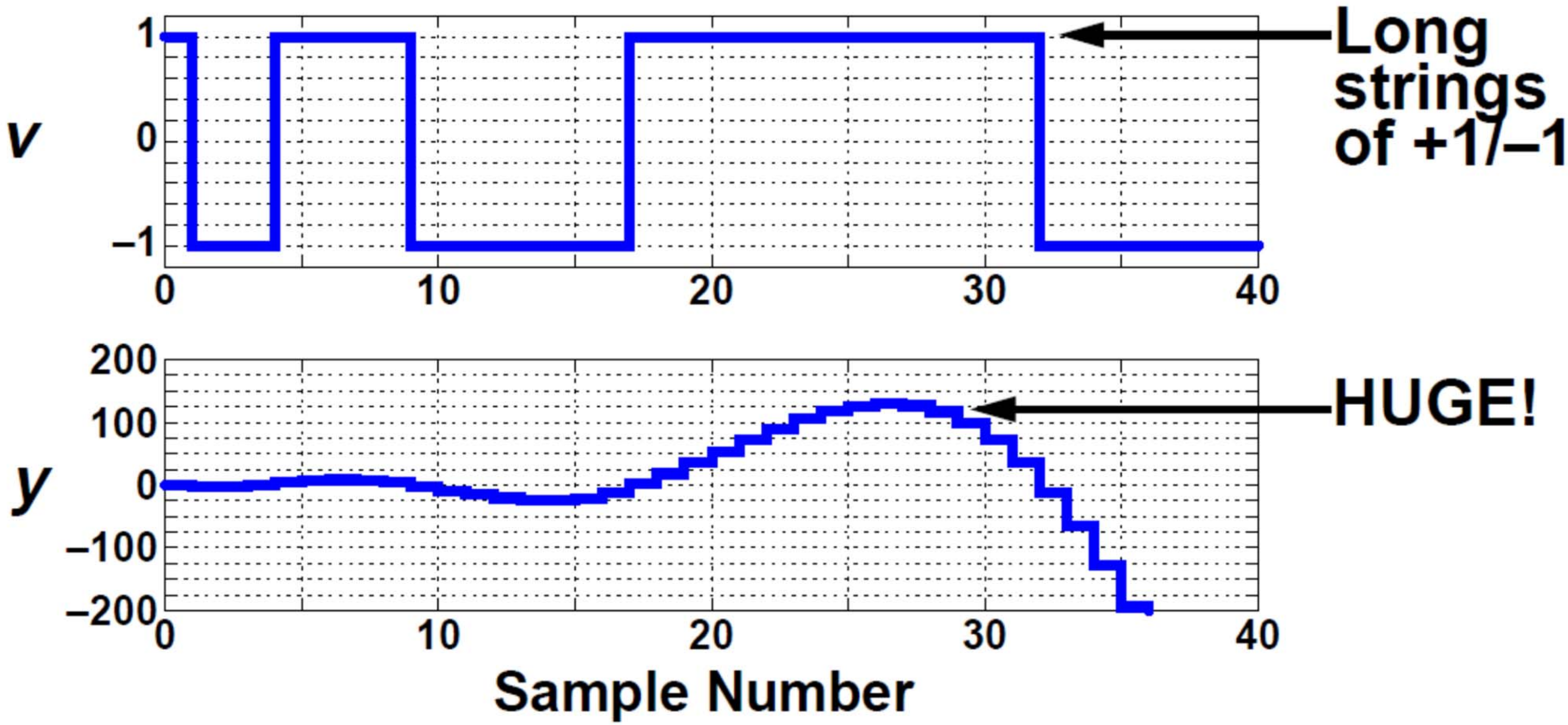
  E.g. MOD3 with an Infinite Quantizer and Zero Input



Simulation of MOD3-1b

- **MOD3 with Binary Quantizer**

  MOD3-1b is unstable, even with zero input

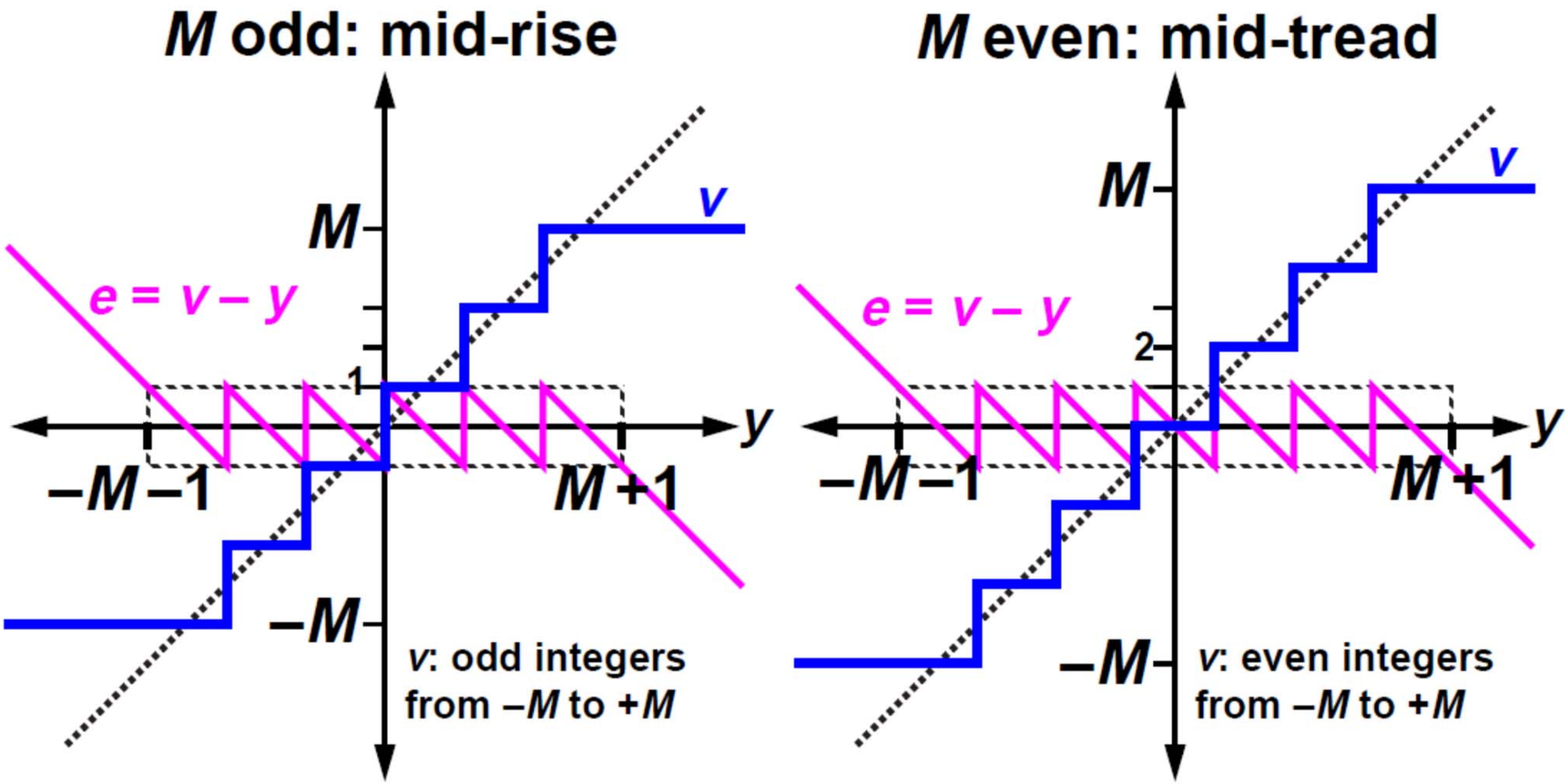


Solutions to the Stability Problem

- **Multi-bit quantization**
  - **Initially considered undesirable because we lose the inherent linearity of a 1-bit DAC**
- **More general NTF (not pure differentiation)**
  - **Lower the NTF gain so that quantization error is amplified less**
  - **Reducing the NTF gain reduces the amount by which quantization noise is attenuated**
- **Multi-stage (MASH) architecture**
- **Combinations of the above are possible**

M-Step Symmetric Quantizer

- $\Delta = 2\ (nlev = M + 1)$
- **No-overload range:** $|y| \leq nlev \rightarrow |e| \leq \Delta/2 = 1$



Multi-bit Quantization

- A modulator with $NTF = H$ and $STF = 1$ is guaranteed to be stable if $|u| < u_{max}$ at all times

  $u_{max} = nlev + 1 - \|h\|_1$

  $\|h\|_1 = \sum_{i=0}^{\infty} |h(i)|$

- In MOD*N* $H(z) = (1 - z^{-1})^N$

  $h(n) = \{1, -a_1, a_2, -a_3, \cdots (-1)^N a_N, 0 \cdots\}, a_i > 0$

  $\|h\|_1 = H(-1) = 2^N$

- $nlev = 2^N$ implies $u_{max} = nlev + 1 - \|h\|_1 = 1$

  MOD*N* is guaranteed to be stable with an N-bit quantizer if the input magnitude is less than $\Delta/2 = 1$

  This result is quite conservative

- Similarly, $nlev = 2^{N+1}$ guarantees that MOD*N* is stable for inputs up to 50% of full-scale

Inductive Proof of $\|h\|_1$ Criterion

- Assume STF = 1 and $|u(n)| \le u_{max}, \forall n$
- Assume $|e(i)| \le 1$ for $i < n$ (induction hypothesis)

$$|y(n)| = \left|u(n) + \sum_{i=1}^{\infty} h(i)e(n-i)\right|$$

$$\le u_{max} + \sum_{i=1}^{\infty} |h(i)||e(n-i)|$$

$$\le u_{max} + \sum_{i=1}^{\infty} |h(i)|$$

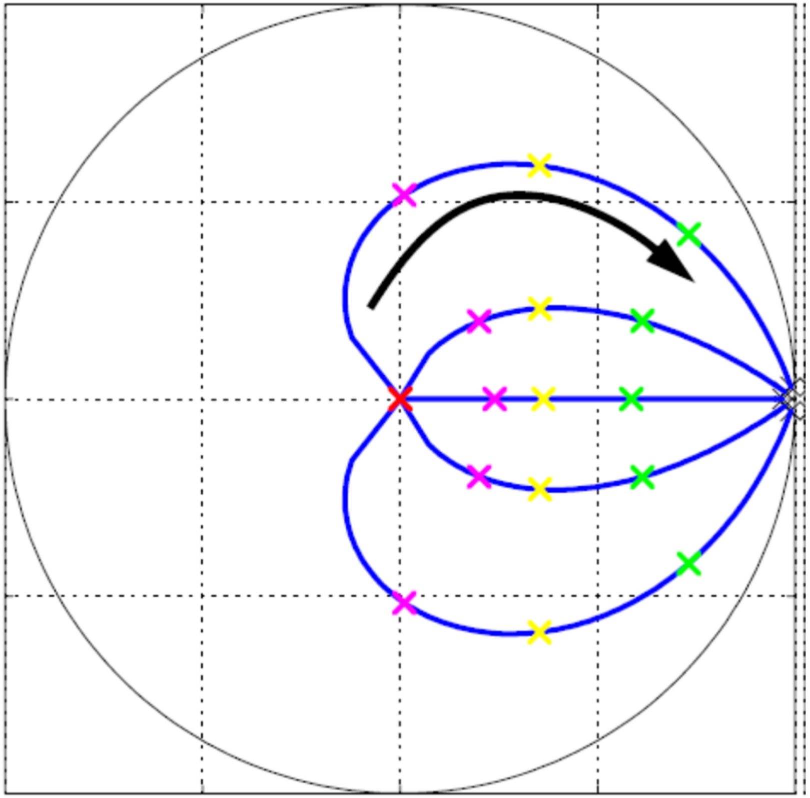
$$= u_{max} + \|h\|_1 - 1$$

- Since $u_{max} = nlev + 1 - \|h\|_1$

  → $|y(n)| \le nlev$, $|e(n)| \le 1$
- So by induction $|e(i)| \le 1$ for all $i > 0$

More General NTF

- **Instead of $NTF(z) = A(z)/B(z)$ with $B(z) = z^n$, use a more general $B(z)$**
  - **Roots of *B* are the poles of the NTF and must be inside the unit circle**



Moving the poles away from z=0 toward z=1 makes the gain of the NTF approach unity

Lee Criterion for Stability

- **Stability criteria in a 1-bit Modulator [Lee, 1987]:**

$$\|H\|_\infty \le 2$$

The infinity-norm of *H* is the measure of the "gain" of *H* over frequency

$$\|H\|_\infty \equiv \max_{\omega \epsilon [0,2\pi]} \left(\left| H(e^{j\omega}) \right| \right)$$

- **Is the Lee criterion <u>necessary</u> for stability?**

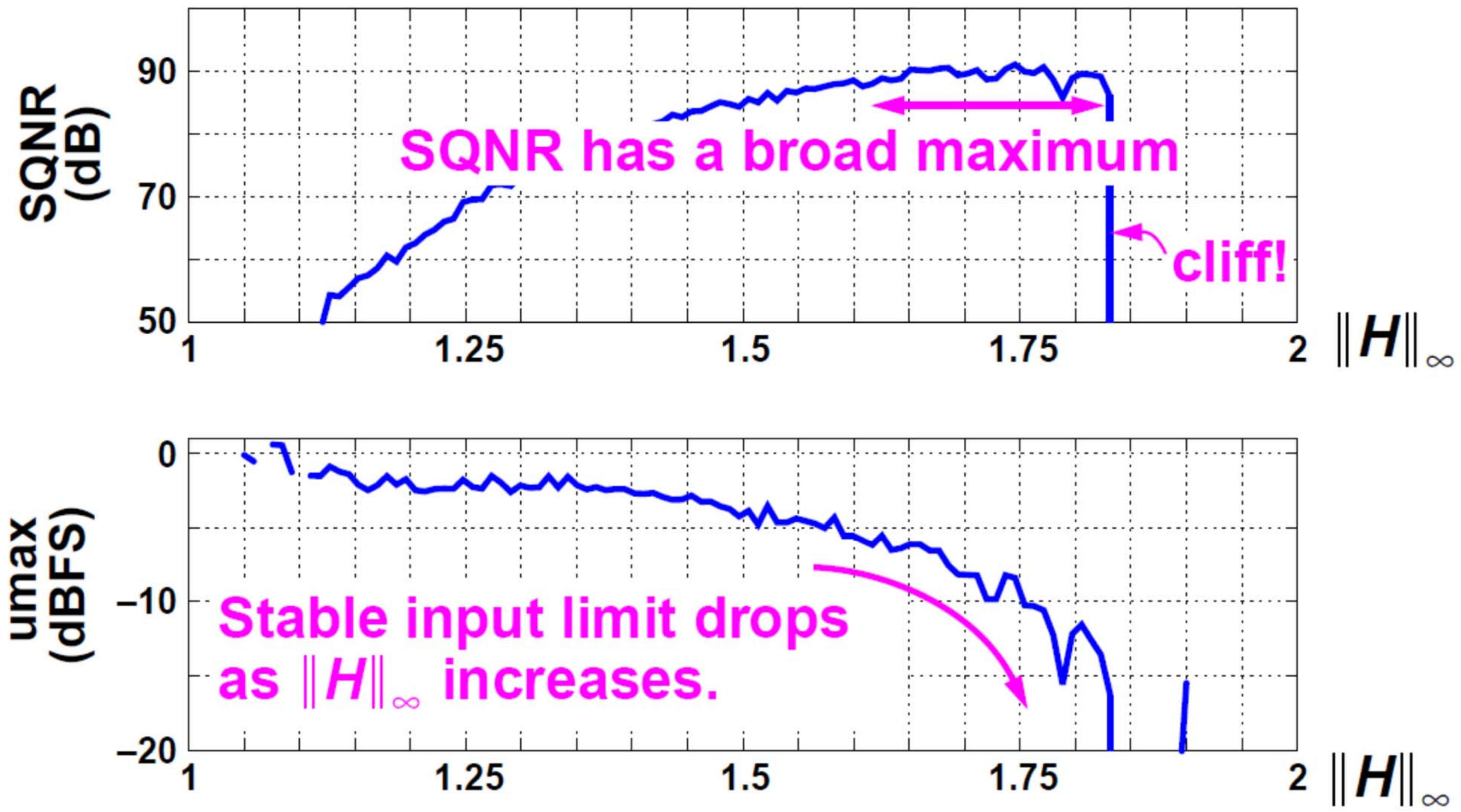
No. MOD2 is stable (for DC inputs less than full-scale) but $\|H\|_\infty = 4$**.**

- **Is the Lee criterion <u>sufficient</u> to ensure stability?**

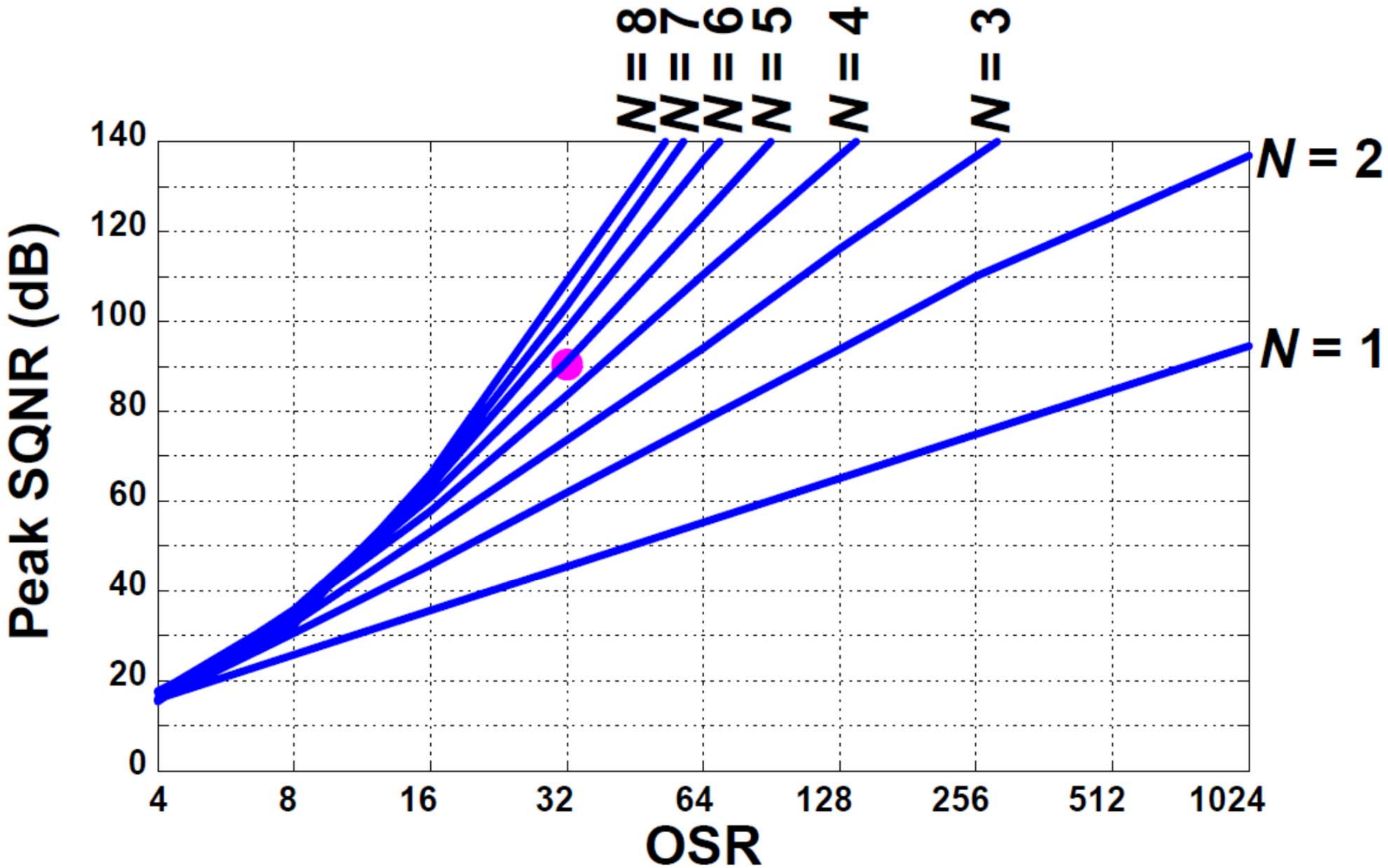
No. There are lots of counter-examples, but $\|H\|_\infty \le 1.5$ **often works.**

Simulated SQNR vs $\|H\|_\infty$

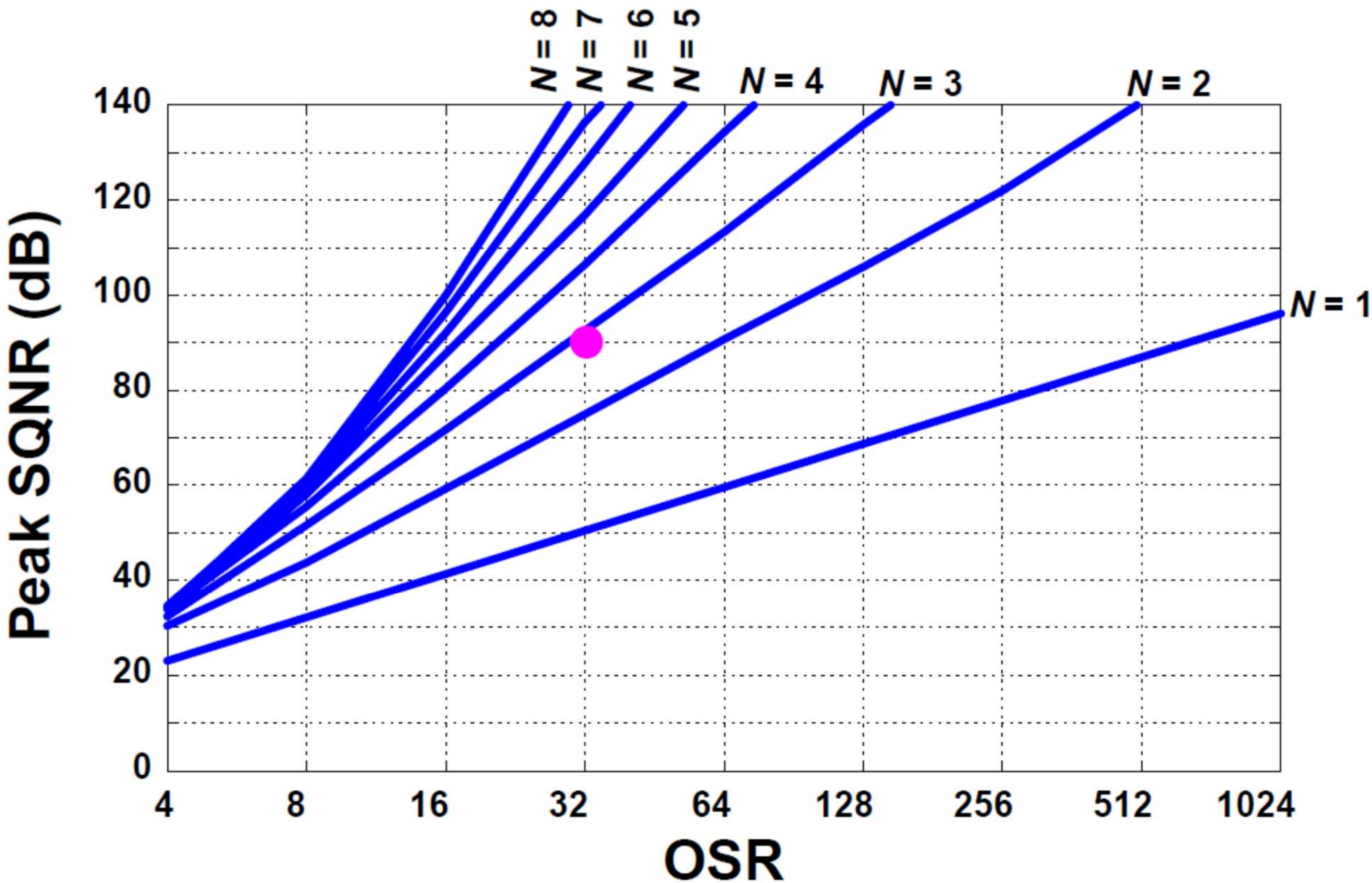
- **5th-order NTFs, 1-bit Quantizer, OSR = 32**



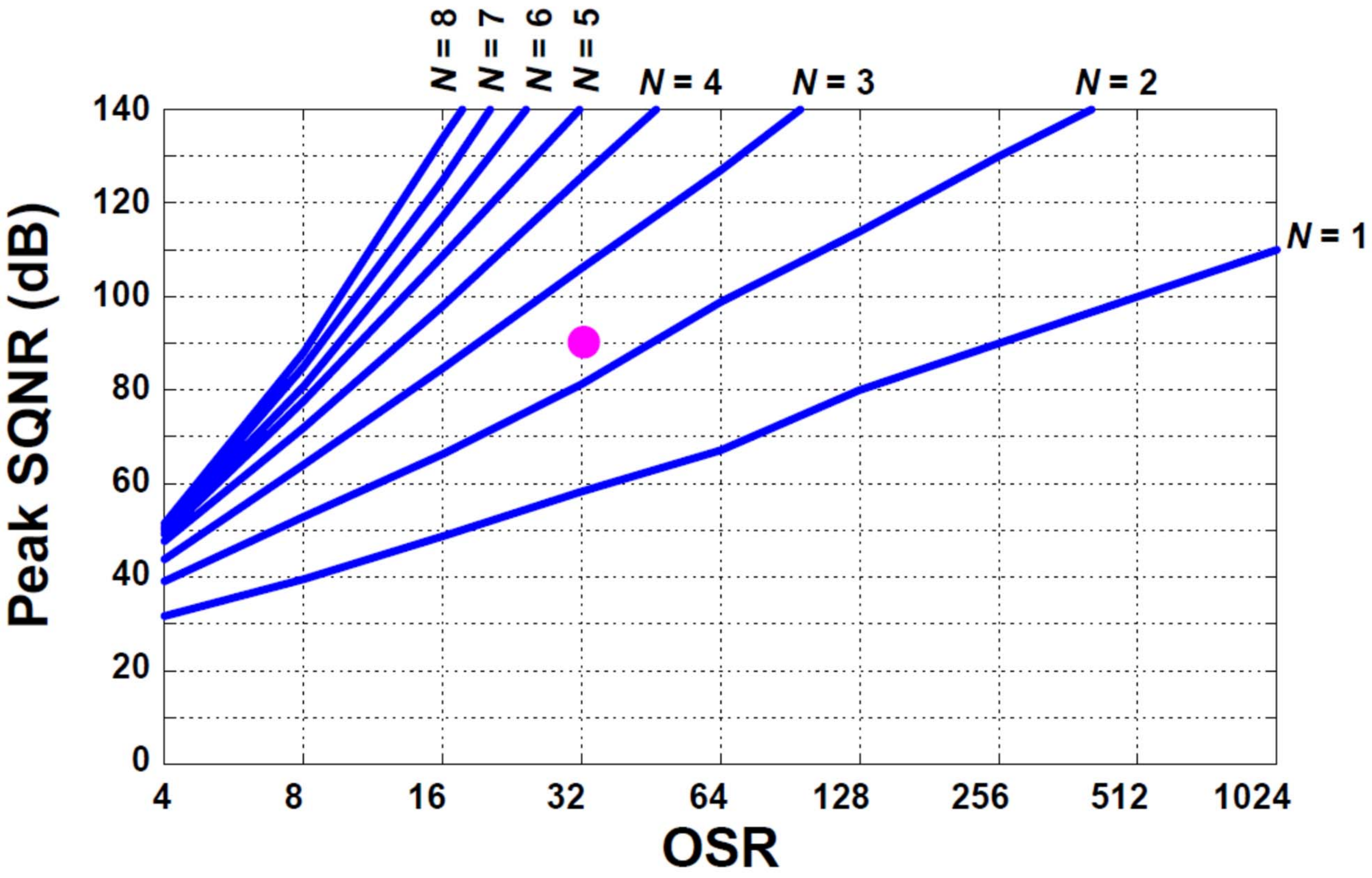
SQNR Limits for 1-bit Modulation



SQNR Limits for 2-bit Modulators

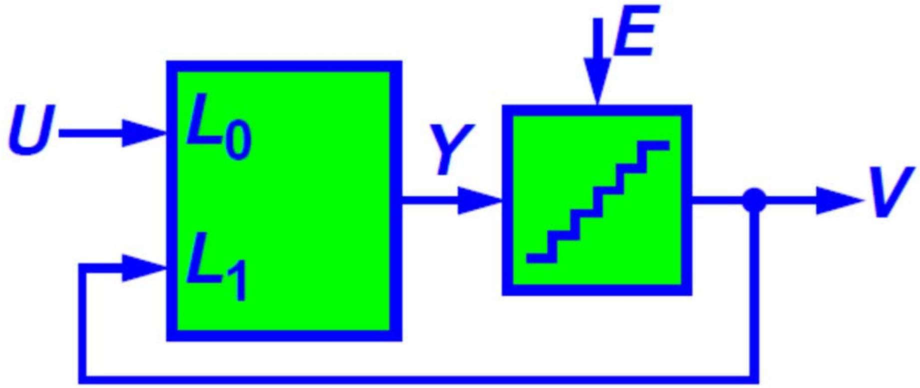


SQNR Limits for 3-bit Modulators



Generic Single-Loop ΔΣ ADC

- **Linear Loop Filter + Nonlinear Quantizer:**



$$Y = L_0 U + L_1 V$$
$$V = Y + E$$
$$\Rightarrow \boxed{V = STF \cdot U + NTF \cdot E}, \text{ where}$$

$$NTF = \frac{1}{1 - L_1} \quad \& \quad STF = L_0 \cdot NTF$$

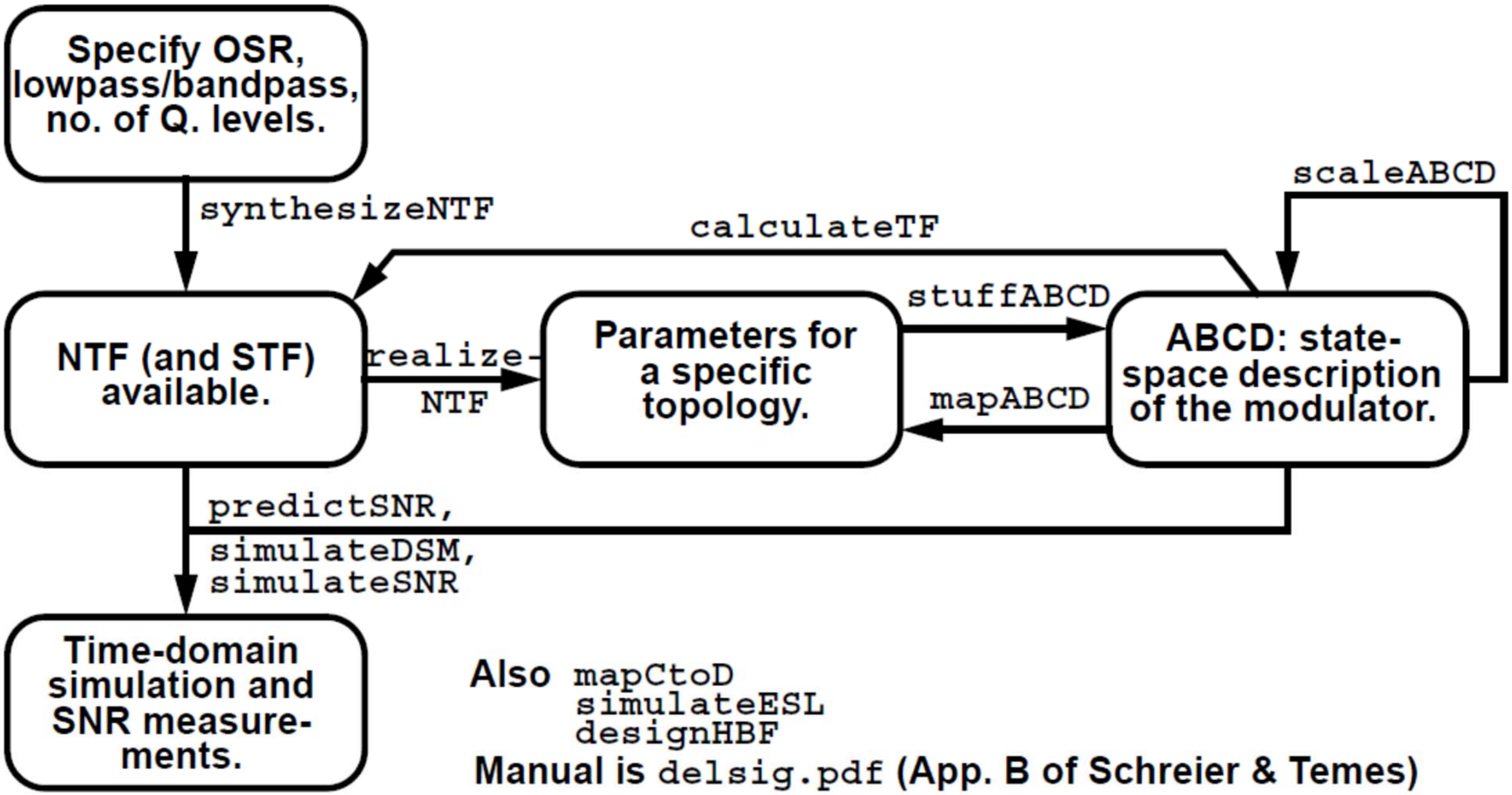
Inverse Relations:

$L_1 = 1 - 1/NTF$, $L_0 = STF\,/\,NTF$

ΔΣ Toolbox

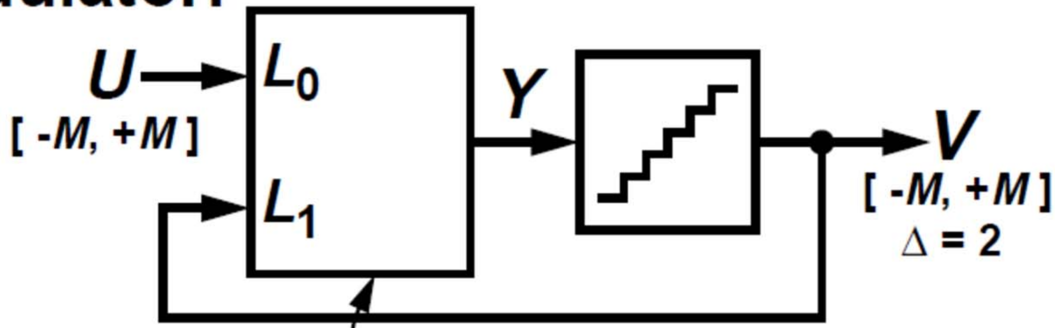
- **Search for ‘Delta Sigma Toolbox’**

  `http://www.mathworks.com/matlabcentral/fileexchange`



ΔΣ Toolbox Modulator Model

Modulator:

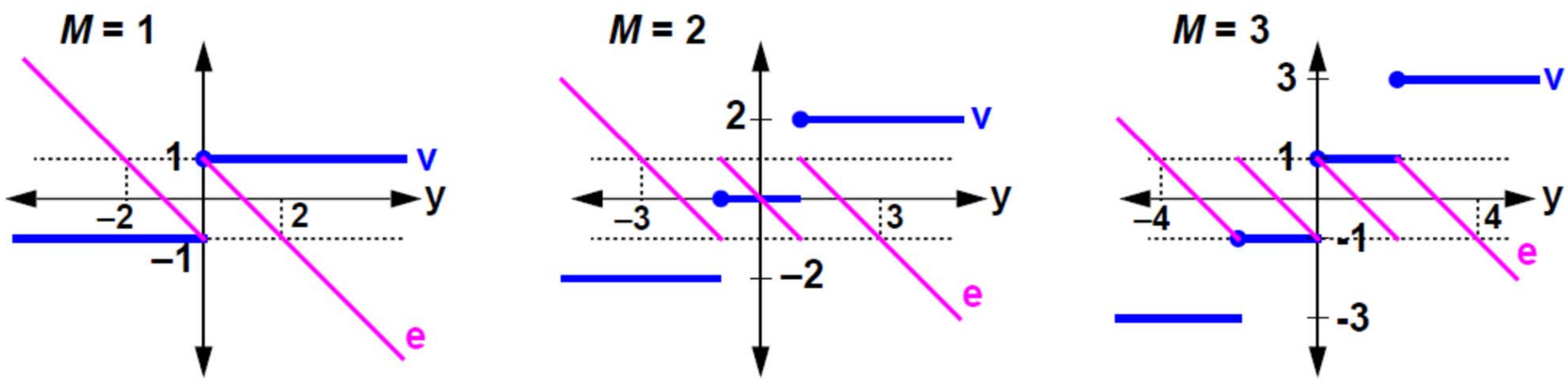


$$NTF = \frac{1}{1 - L_1}$$

$$STF = \frac{L_0}{1 - L_1}$$

Loop filter can be specified by NTF or by ABCD, a state-space representation

Quantizer:



Mid-tread quantizer;
v: even integers [–*M*,+*M*]

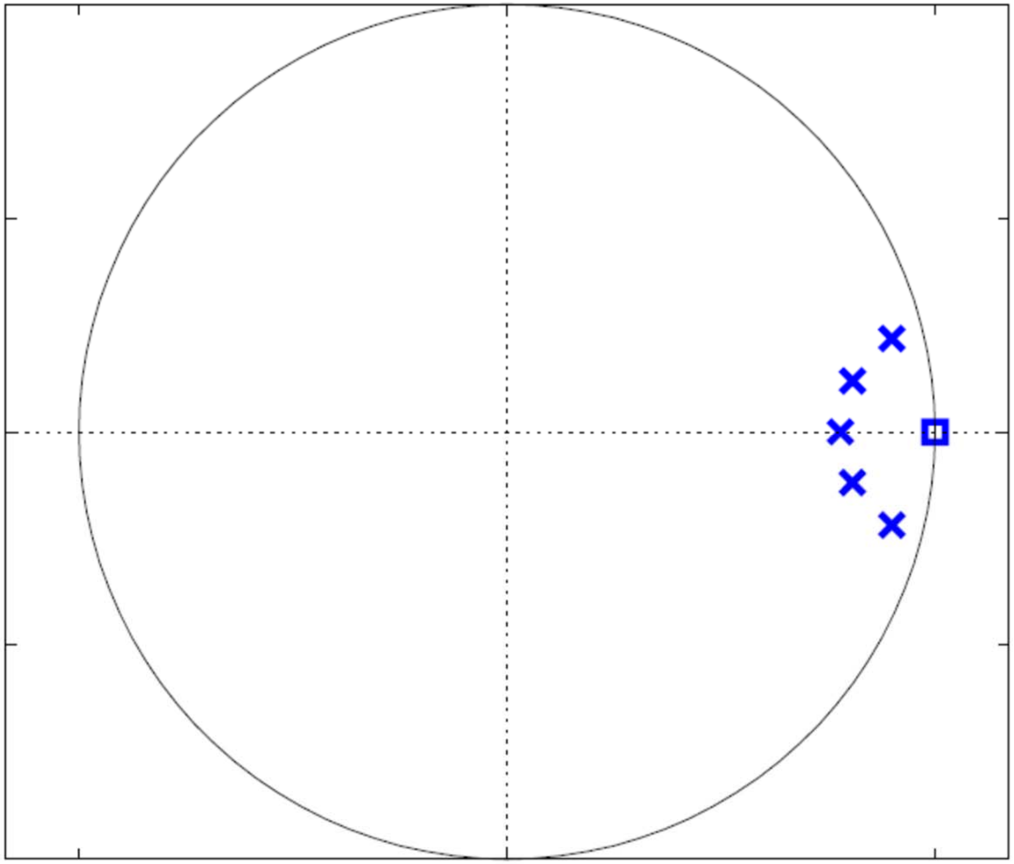
Mid-rise quantizer;
v: odd integers [–*M*,+*M*]

NTF Synthesis (`synthesizeNTF`)

- **Not all NTFs are realizable**
  - **Causality requires $h(0) = 1$, or in the frequency domain, $H(\infty) = 1$. Recall $H(z) = h(0)z^0 + h(1)z^{-1} + \cdots$**
- **Not all NTFs yield stable modulators**
  - **Rule of thumb for single-bit modulators: $\|H\|_\infty < 1.5$ [Lee]**
- **Can optimize NTF zeros to minimize the mean-square value of *H* in the passband**
- **The NTF and STF share poles, and in some modulator topologies the STF zeros are not arbitrary**
  - **Restrict the NTF such that an all-pole STF is maximally flat (almost the same as Butterworth poles)**

Lowpass Example (dsdemo1)

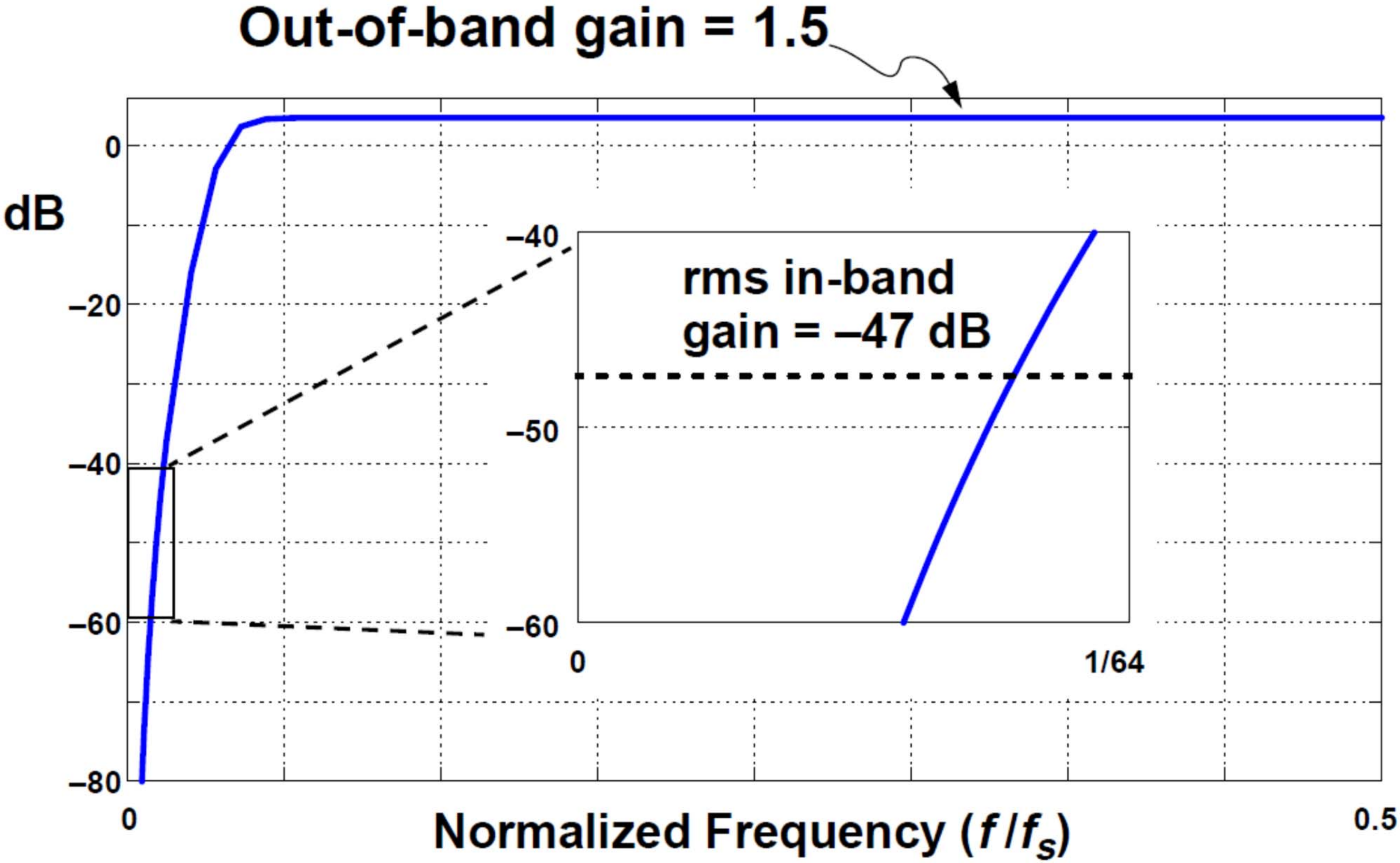
- **5^{th}-order NTF, all zeros at DC**
- **Pole/Zero diagram:**



```
OSR = 32;
H = synthesizeNTF(5);
plotPZ(H);

f = linspace(0,0.5);
z = exp(2i*pi*f);
H_z = evalTF(H,z);
plot(f,dbv(H_z));
g = rmsGain(H,0,0.5/OSR)
```

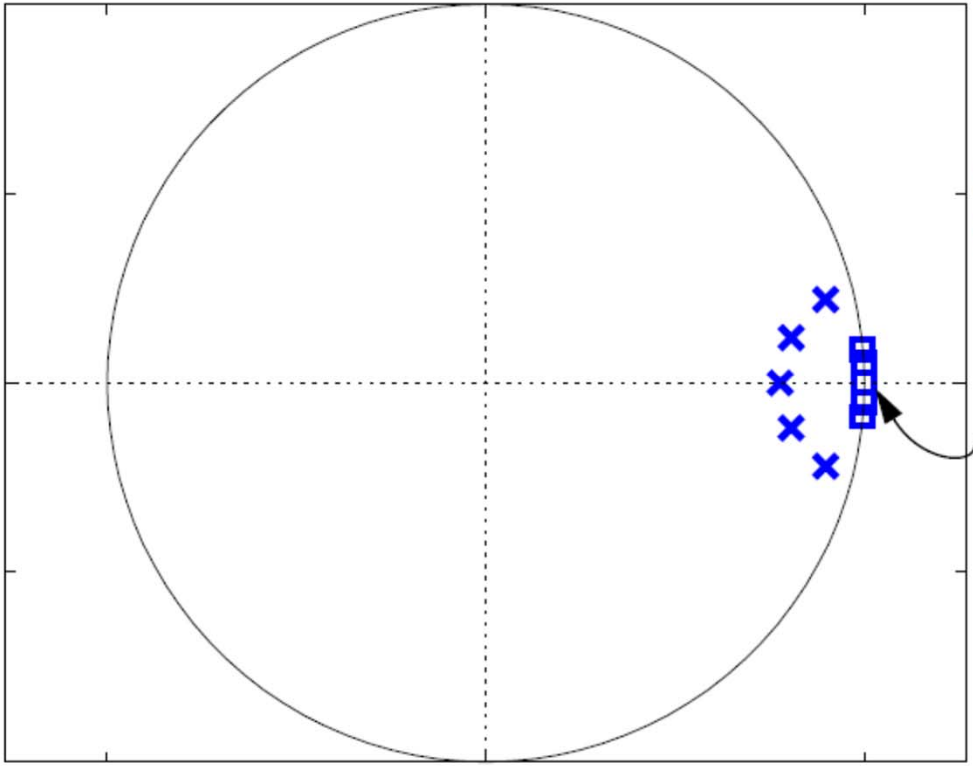
Lowpass NTF



Out-of-band gain = 1.5
dB
0
–20
–40
–60
–80
0
0.5
Normalized Frequency (f / fs)
–40
–50
–60
0
1/64
rms in-band
gain = –47 dB

Improved 5th-Order Lowpass NTF

- **Zeros optimized for OSR=32**

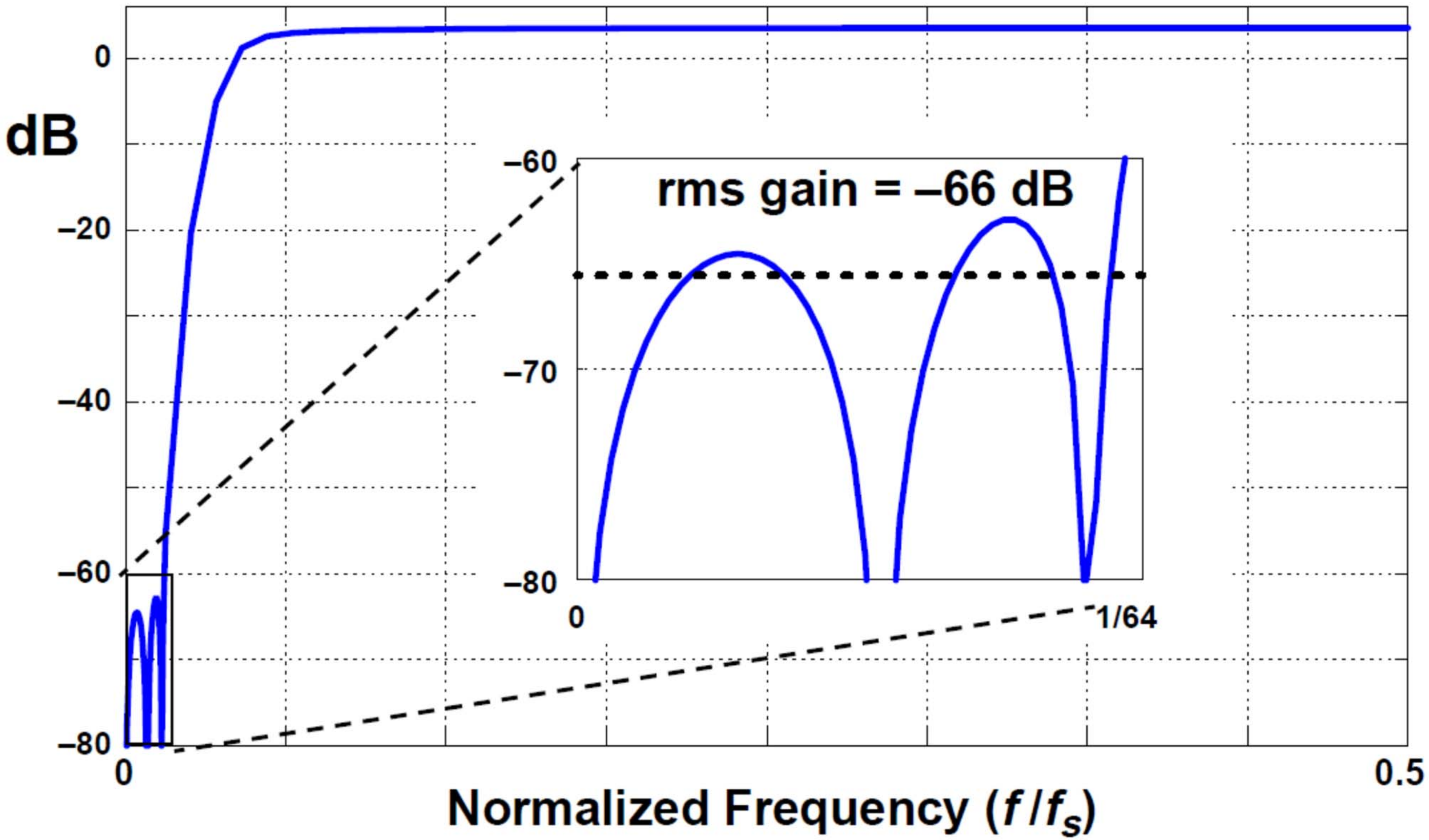


optimization flag

```
OSR = 32;
H = synthesizeNTF(5,OSR,1);
...
```

Zeros spread across the band-of-interest to minimize the rms value of the NTF.

Improved NTF

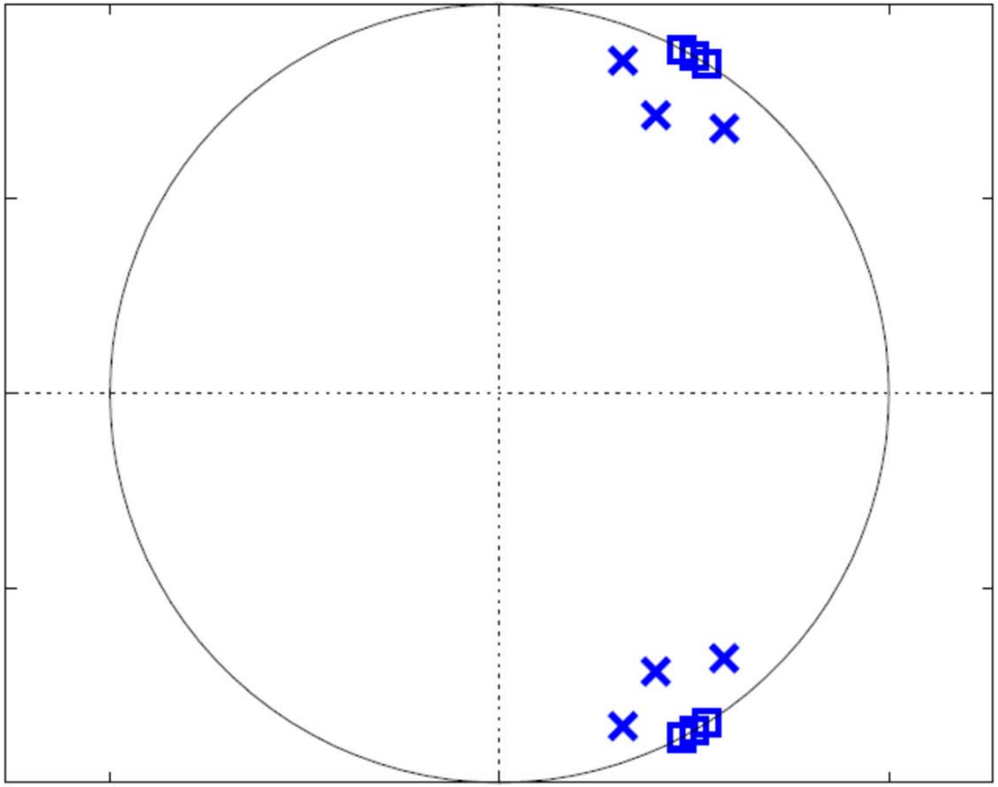


Bandpass Example

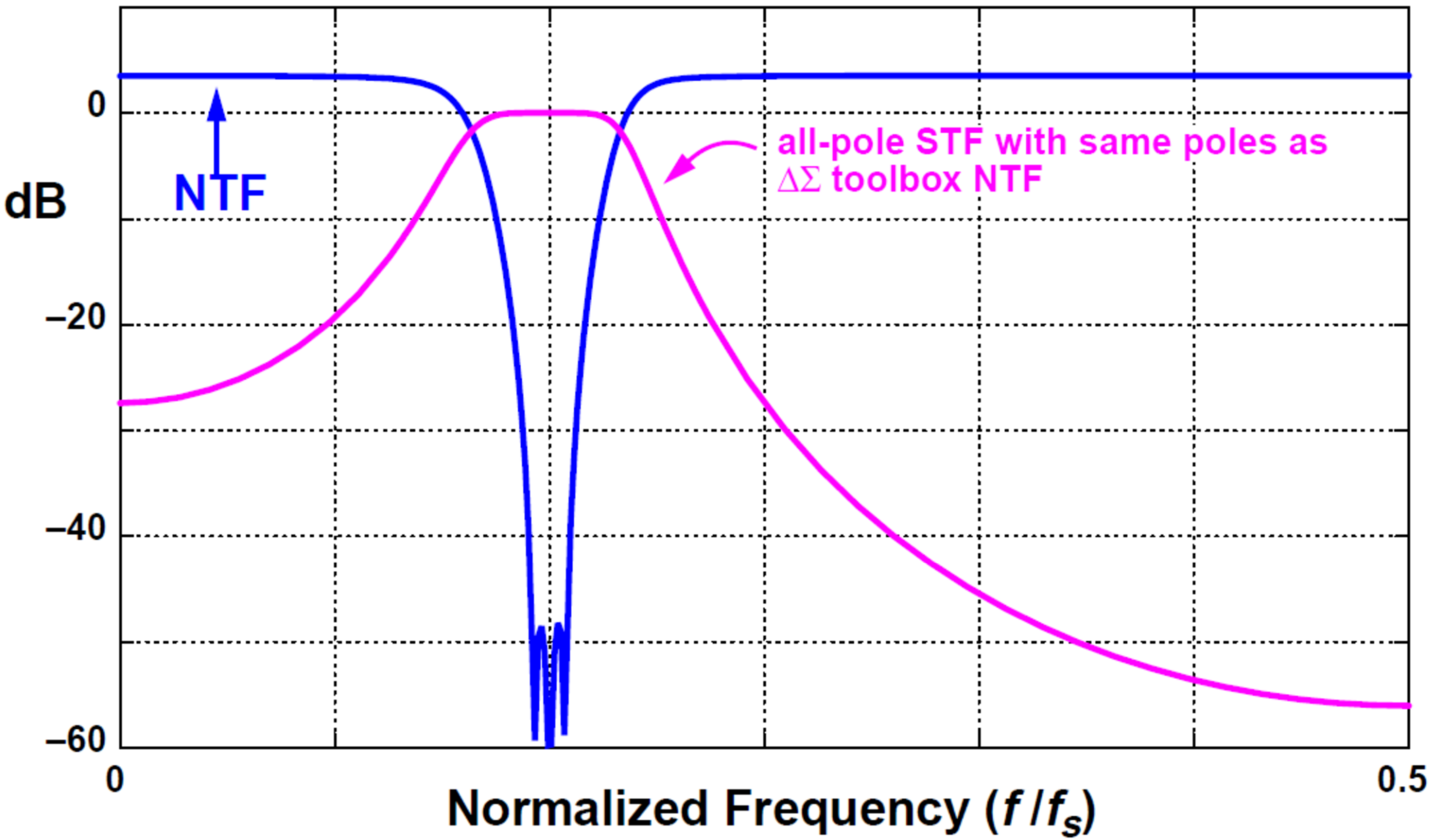
```
OSR = 64;
f0 = 1/6;
H=synthesizeNTF(6,OSR,1,[],f0);...
```

center frequency

[] or NaN means use default value, i.e. Hinf = 1.5



Bandpass NTF and STF



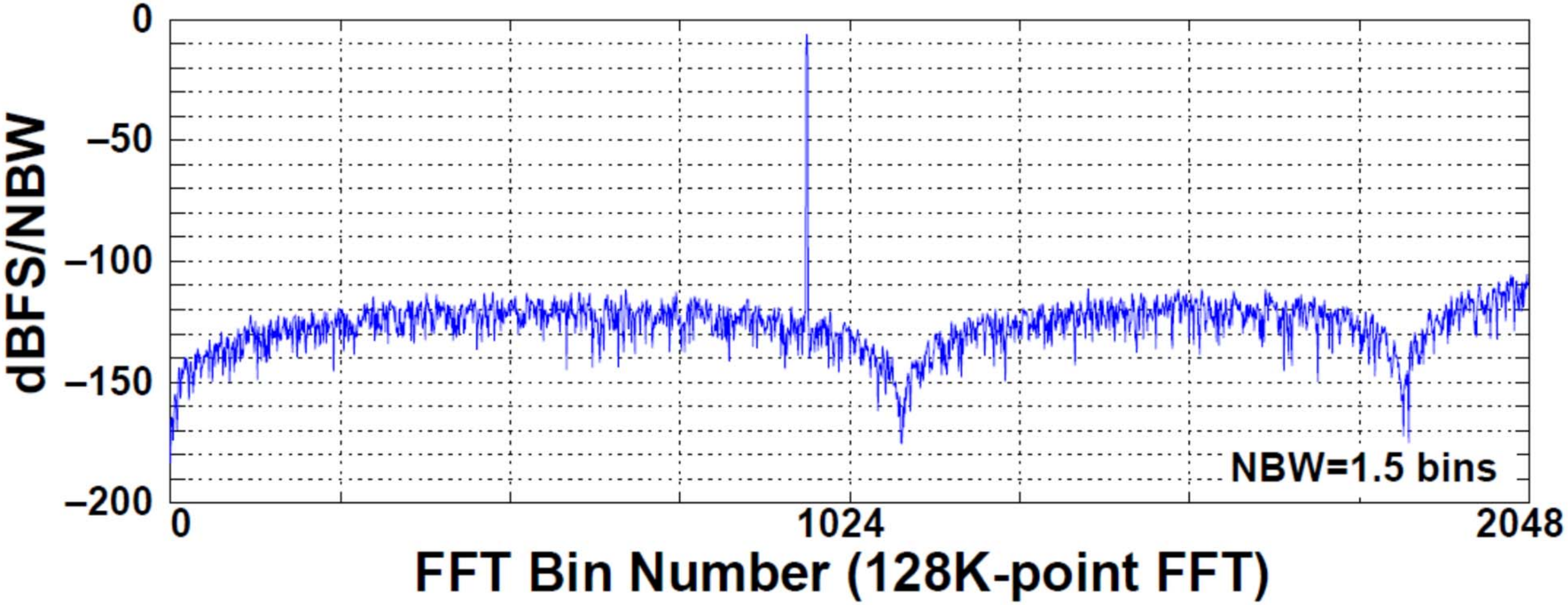
Summary: NTF Selection

- If OSR is high, a single-bit modulator may work
- To improve SQNR
  - Optimize zeros
  - Increase $\|H\|_\infty$
  - Increase order
- If SQNR is insufficient, must use a multi-bit design
  - Can turn all the above knobs to enhance performance
- Feedback DAC assumed to be ideal

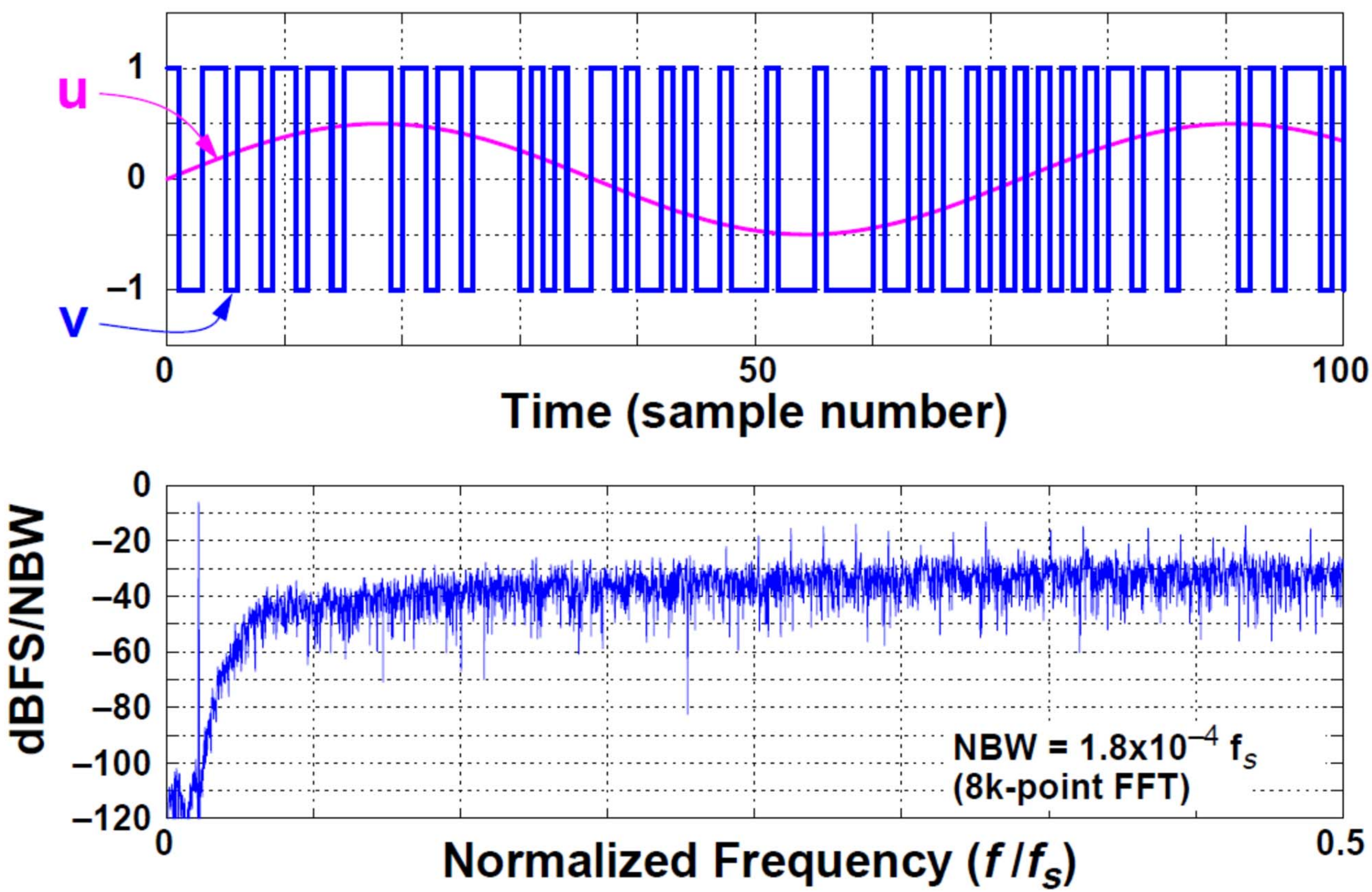
NTF-Based Simulation (dsdemo2)

```
order=5; OSR=32;
ntf = synthesizeNTF(order,OSR,1);
N=2^17; fbin=959; A=0.5; % 128K points
input = A*sin(2*pi*fbin/N*[0:N-1]);
output = simulateDSM(input,ntf);
spec = fft(output.*ds_hann(N)/(N/4));
plot(dbv(spec(1:N/(2*OSR))));
```

- In `mex` form; 128K points in < 0.1 sec

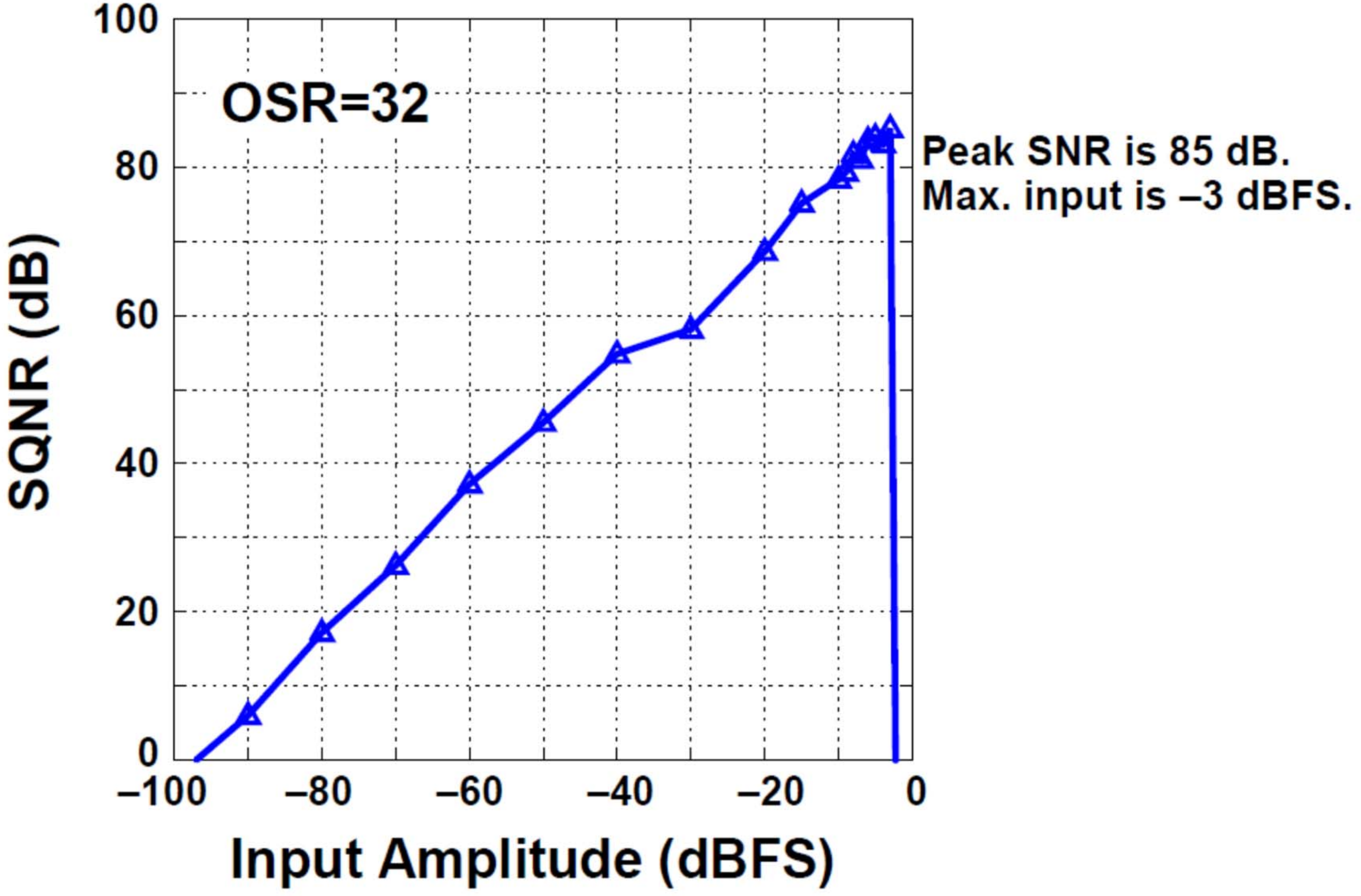


NTF-Based Simulation (dsdemo2)



SNR vs Amplitude (simulateSNR)

```
[snr amp] = simulateSNR(ntf,OSR);
plot(amp,snr,'b-^');
```



Homework #2 (Due Jan 28)

- **Extract code from `dsdemo1` and `dsdemo2` to:**

  1. **Create a 4th-order NTF with zeros optimized for OSR=32 and $\|NTF\|_\infty = 3$.**
     a) **Plot the poles/zeros and frequency response of your NTF.**

  2. **Simulate a 5-step (6-level) $\Delta\Sigma$ modulator with this NTF (Note: full-scale is *M* with an *M*-step modulator).**
     a) **Plot example input and output waveforms.**
     b) **Plot a spectrum and the predicted noise curve.**
     c) **Plot the SQNR vs input amplitude curve and note the maximum stable input.**

What You Learned Today

- N^{th}-order modulator (MOD*N*)
- High-level design with the ΔΣ Toolbox

Circuit of the Day: Level Translator

- **3V to 1V:**

- **1V to 3V:**