Ricky Yuen

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Canada

M.A.Sc., Electrical Engineering, Electronics
B.A.Sc., Computer Engineering

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Objective

To obtain a challenging position in the area of Mixed-Signal Design.

Technical Skills

Design:	Sigma-delta ADC, 6.4Gbps wireline transmitter, PLL, LNA, RF filter, PCB
Verification:	System level verification with Matlab and Verilog
Backend:	High-speed I/O and analog circuitry layout
Laboratory:	RF chip-level testing and characterization
Programming:	Verilog, VHDL, C++/C, Perl, Matlab, Assembly

Work Experience

Analog Designer, *Fresco Microchip Inc.*, Woodbridge, ON 03/05-Present

- Lead the design of a high speed, high resolution sigma-delta ADC for video application
- System level design and behavioral simulation of channel select IF filter

Intern, *Fujitsu Laboratories of America*, Sunnyvale, CA 03/04-07/04

- Implemented a testchip for a 6.4Gbps high-speed transmitter. A 3.2GHz PLL is designed as the timing source. The design is thoroughly verified with Matlab and Verilog simulations. Layout is done with 0.11um CMOS.
- Other projects include WLAN RF front-end design, phase noise modeling, integrated inductor modeling and characterization, digital design flow, and VHDL synthesis.

Analog Designer, *Sirific Wireless Corp.*, Waterloo, ON 05/02-08/02

- Designed a baseband filter opamp with 0.18um CMOS. The component noise contributions are analyzed with RF Spectre.
- Performed characterization of Sirific baseband testchip in laboratory.
- Developed RF transceiver simulation model with HDL and Matlab.

Research Assistant, *University of Waterloo*, Waterloo, ON 01/01-04/01

- A team member in designing a low-swing clock buffer with 0.13um CMOS. The clock buffer is characterized and its power consumption and bandwidth are compared with published clock buffers.
- Designed a PCB for ADC testchip. Worked with a graduate student in laboratory debug and testing.

RF Engineer, *Research In Motion, Limited*, Waterloo, ON 04/00-08/00

- Worked in a laboratory and characterized CDMA receiver components. Earned experience on usage of laboratory equipment.

IC Developer, *ATI Technologies Inc.*, Toronto, ON 09/99-12/99

- Developed a gated clock latch for Radeon graphics chip.
- A team member in the signal integrity project analyzing electro-migration problems in deep sub-micron process.
- Maintained TSMC 0.18um standard cell and ATI cell libraries.

Education

M.A.Sc. *University of Toronto*, Toronto, ON 2002-2004

- Master of Applied Science in Electrical & Computer Engineering
- Specialized in High-speed signaling in the Electronics group
- NSERC PGS-A scholarship recipient
- Teaching Assistantship in 3rd year Electronics course
- **Thesis**: A 6.4Gbps Transmitter with ISI and Reflection Cancellation

B.A.Sc. *University of Waterloo*, Waterloo, ON 1997-2002

- Bachelor of Applied Science in Electrical & Computer Engineering
- Two times Dean's Honour List recipient

References Available upon Request