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Analog to Digital Converter in Wireless Local Area Network IEEE 802.11a

Integrated Circuits for Digital Communications ECE1392F

Research Paper

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1. Abstract

The IEEE 802.11a standard is the wireless local area network (WLAN) standard for tomorrow's high demanding communication world. However, battery life of the device is a major problem for today's user because everyone wants to avoid the need of frequently recharging the battery of the device, i.e. laptops. As a result, power consumption of the device has to be low while maintaining adequate performance. Analog to digital converters (ADCs) are major power consumers in any device. Thus, it is worth the designer's time to choose an architecture that has the best trade off between power consumption and performance, i.e. resolution and speed. Pipelined ADC is more suitable for digitization later in the system, i.e. when I and Q data separation is done with SAW devices, since pipelined ADC usually have relatively less power consumption. Interpolation/averaging ADC aims toward a higher performance application, i.e. digitization of data before I and Q data separation; since interpolation ADC usually has higher power consumption but faster conversion rate. These two ADC architectures are in active research today as better trade off between power consumption and performance is demanded by the future.

2. Introduction

Everything is wireless! This is the aim of the research for our high-tech world in the future. Examples of application that are changing to wireless include home telephones, stereo speakers, keyboards and most importantly, our computer and communication networks. However, unlike the home telephones and keyboards, computer and communication networks require transmitting a large amount of data at very high connection speed and little loss of information. This is the goal of the third generation (3G) wireless and mobile system including the WLAN standard, IEEE 802.11a.

IEEE 802.11a is a standard that was approved by the IEEE committee back in 1999. It is a standard based on coded orthogonal frequency-division multiplexing (OFDM) modulation and it provides two to five times the data rate and as much as ten times the system capacity than its predecessor, IEEE 802.11b. The IEEE 802.11a WLAN standard operates in the 5GHz frequency band with a channel bandwidth of 20MHz and a variable data rate between 6 – 54*Mbit/sec* [7]. In any wireless application, power consumption of the device is as important as its performance. A typical transceiver chip for the 802.11a standard consumed about 800*mW* of power when operating in full speed and of that 800*mW* of power consumption, nearly 25% is taken by the ADCs [9]. Clearly, more power efficient ADCs with adequate performance should be used in order to extend the battery life of the device.

For the IEEE 802.11a standard, the ADCs usually require 8-10 bits of resolution while running at 40MHz for Nyquist rate ADC and even higher sampling rate for oversampled ADC. The number bits depends on the overall system architecture. If digitization is done before the in-phase (I) and quadrate (Q) data separation, the ADC is required to be high speed; otherwise, a slower but higher resolution ADC can be used. Figure 2-1 shows a typical system architecture for the WLAN 802.11a. This transceiver can be used with all the 802.11 standard, claimed in

[10]. The role of the ADC is to perform digitization of the received data so that the data can be decoded digitally by the baseband processor.

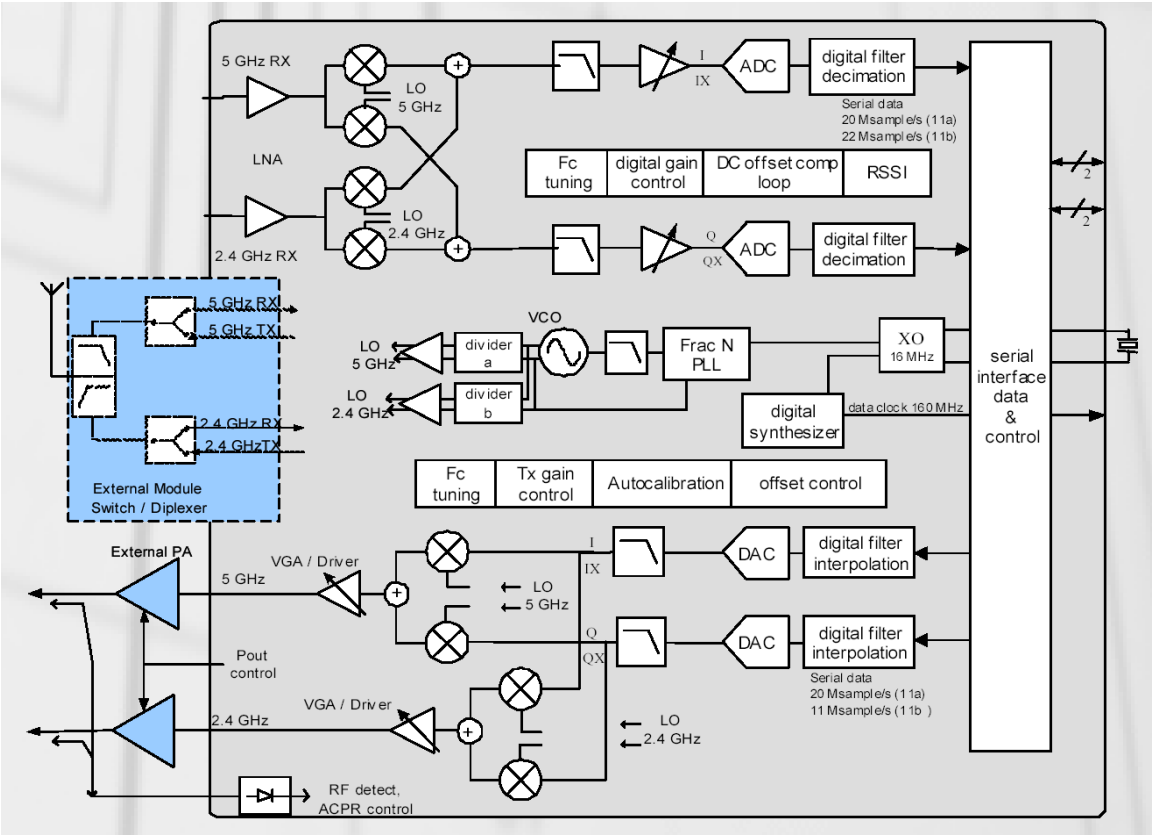

Figure 2-1 802.11a system architecture using direct conversion transceiver.

3. Interpolating and Averaging ADC

The interpolating and averaging ADC is based on the architecture of the flash ADC, which is the fastest of all ADC architectures. It tries to overcome the high power consumption disadvantage of the flash ADC by using analog preprocessing like pre-amplifying, interpolating, folding and averaging techniques [4]. As a result, lower input capacitance is seen by the input signal because the comparators are placed after the analog preprocessing. By making sure that the interpolation network does not load the preamplifiers, power can be saved [3].

The basic idea of an interpolating and averaging ADC is that the sampled input analog signal will go through a number of pre-amplification stages before the

comparison and digitization actually take place. In between the pre-amplification stages, interpolation will be done to get the required resolution of the digital output. Averaging at the output of the interpolation network with the help of passive elements can improve the accuracy of the digitization [1].

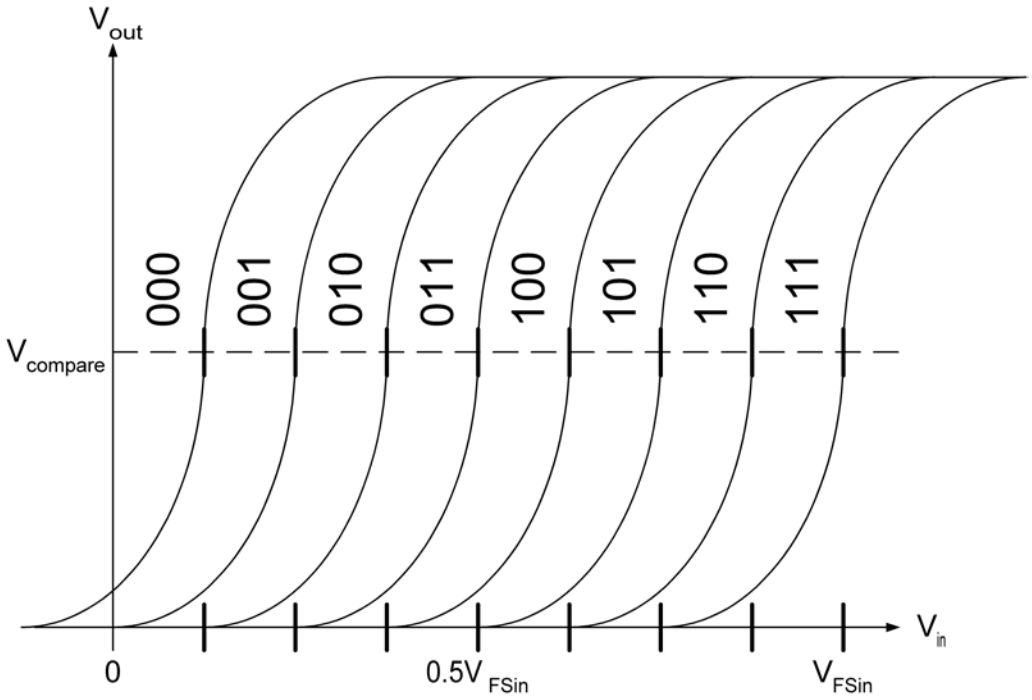

Figure 3-1 The transfer function and output of a 3-bit interpolation ADC.

Figure 3-1 illustrates the transfer function of the interpolation ADCs. This example is for a 3-bit resolution but the idea applies equally to higher resolution interpolation ADC. As seen, the input full-scale voltage (V_{FSin}) is divided into 8 equal parts by using differential amplifier type circuit. The sampled input voltage will be compared to all eight transfer functions simultaneously at every intersection points of the dotted line and the transfer functions, i.e. comparing to eight 1-bit flash ADC each with different input-output relationship. The result will be encoded into a 3-bit digital output.

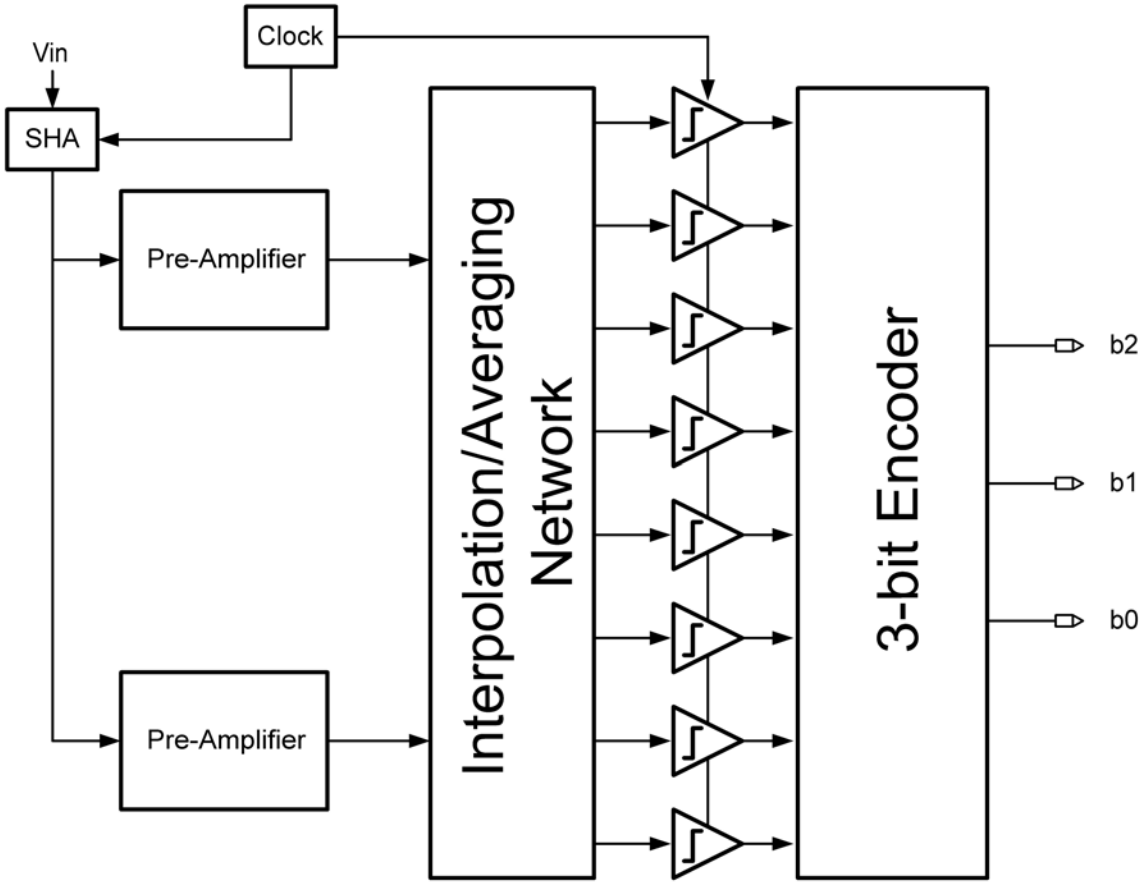

Figure 3-2 Block diagram of a 3-bit interpolating ADC.

The block diagram and operation of the interpolating and averaging ADC is shown in Figure 3-2. The sampled input analog voltage is fed into two pre-amplifiers and their outputs are interpolated eight times (interpolation factor = 4). The interpolated outputs are averaged with resistors to lower the non-linear characteristics of the interpolation networks. This averaging of the output is illustrated in Figure 3-3 below.

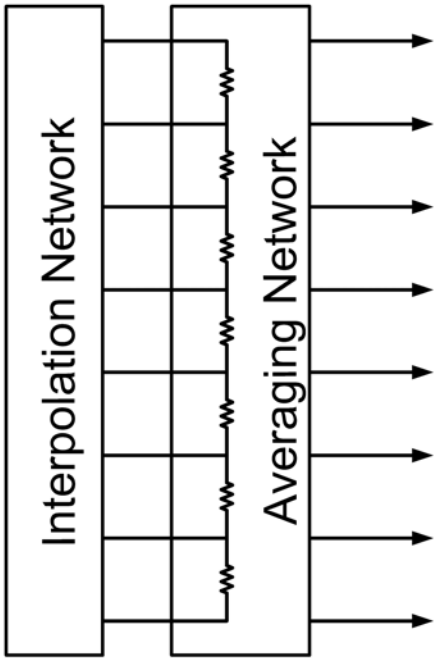

Figure 3-3 Interpolation and averaging network.

The averaged and interpolated outputs are compared with the sampled input voltage in regenerative comparators. The eight results will be encoded into a 3-bit digital word for the output.

J. Vandenbussche et. al. [4] makes use of the interpolation and averaging architecture to propose a high-speed and high-accuracy ADC for WLAN application like IEEE 802.11a. It has 8-bit of resolution and capable of running at an input frequency of 30MHz. The block diagram of the ADC is shown in Figure 3-4.

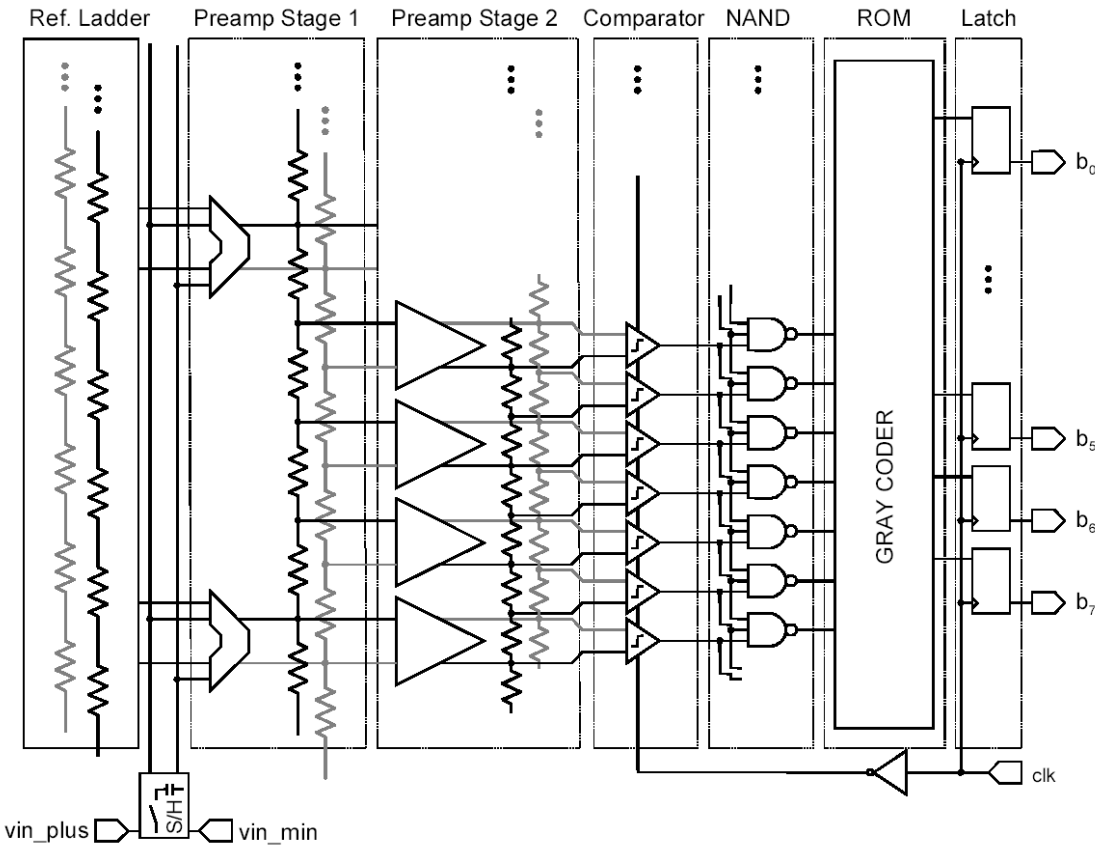

Figure 3-4 A 200 *MS/s* 8-bit Interpolating ADC [4].

The architecture shown in Figure 3-4 has two pre-amplifier stages with interpolation factor equals to 4 and 2 respectively. The resistive ladder on the left sets the reference voltages for the rest of the ADC stages. The rest of the stages are just as described previously. The ADC is fabricated in 0.35μm CMOS process and it consumes about 300mW when operating at full speed of 200MS/s. The interpolating and averaging ADC is able to achieve a SNR ratio of 43dB. The power consumption is relatively high for today's requirement. However, by using technology scaling, i.e. 0.13um process, the power consumption can be significantly deceased without changing of the circuit topology.

4. Pipelined ADC

A pipelined ADC is a Nyquist rate ADC. It uses the idea of breaking up stages with long delay and makes them operate in parallel with each other such that it achieves high throughput. However, the pipelined ADC has introduced a constant latency between the input and output signal.

Figure 4-1 shows the block diagram of a N-bit pipelined ADC. It consists of a two stages pipeline but the idea can be extended to pipelined-ADC with higher number of stages.

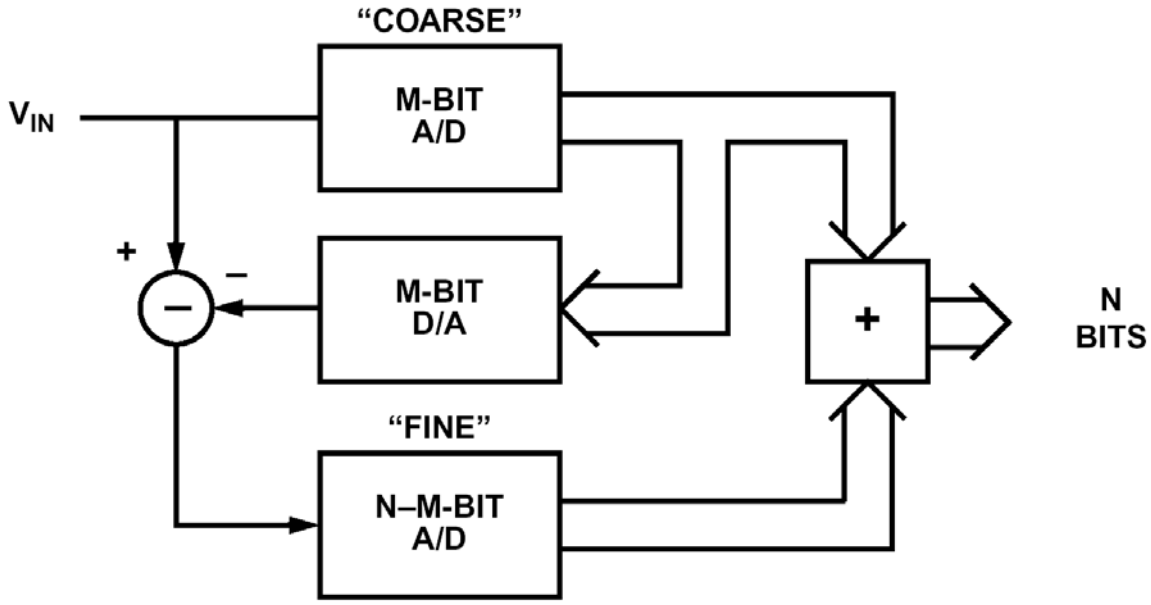

Figure 4-1 Block diagram of a 2 stages pipelined ADC.

The input voltage will go through a M-bit flash ADC, which will become the M-MSB of the digital output word produced by the first stage of the pipeline. The M-bit digital output of the first flash ADC will then be converted back to analog voltage by a M-bit digital to analog converter (DAC). This analog voltage is subtracted from the input voltage to become the residue voltage (V_s). A N-M-bit

flash ADC will convert this residue voltage to the final N-M LSB of the digital word, which is the second stage of the pipeline.

In this configuration, the second stage flash ADC needs resolution equal to N-bit. Thus, inter-stage amplifier is usually employed to relax this requirement. Another problem that the pipelined ADC faces is the comparator offset. The comparator offset usually led to digitization error in the digital output. Therefore, most pipelined ADC implementation adds a digital error correction block before the output to correct the digital output [2,8]. Figure 4-2 illustrates this structure below.

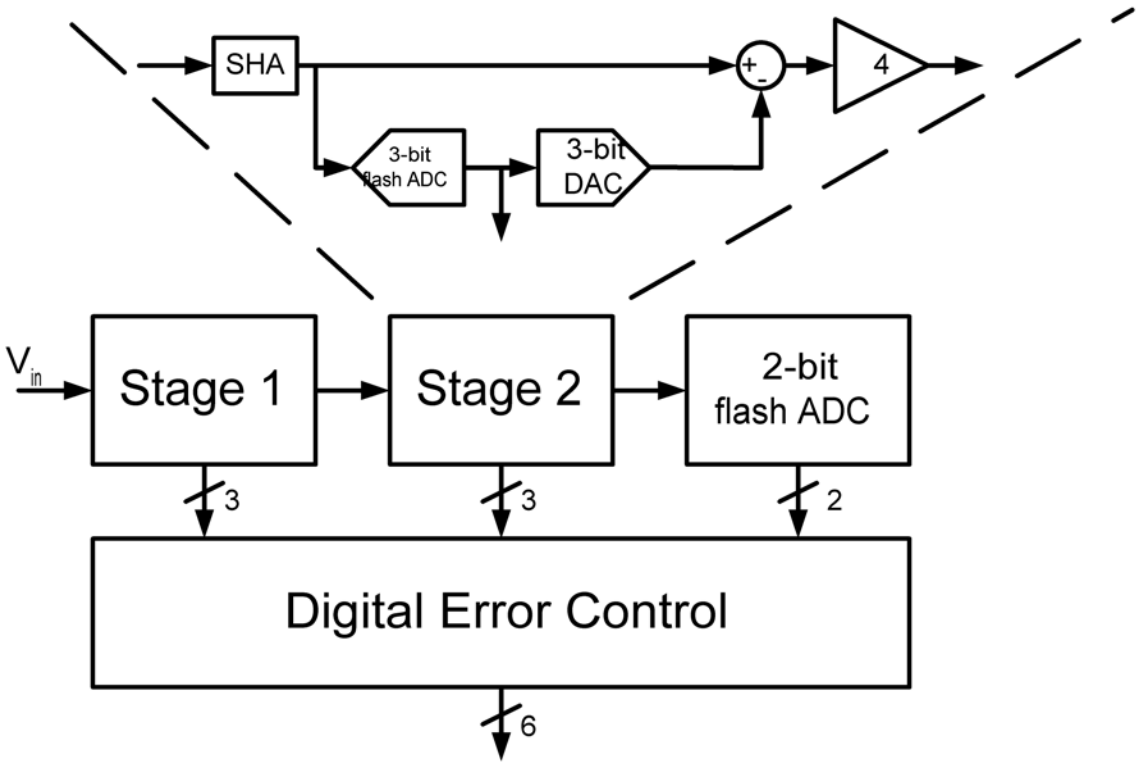

Figure 4-2 The block diagram of a 3 stage pipelined ADC with digital error control.

The idea of the digital error correction is to produce one more bit per stage (except the last stage) to serve as a conversion overlap between pipeline stages. By introducing this overlap, different kinds of correction scheme can be introduce to greatly reduce the error due to comparator offset.

S. Mathur et. al. designed a 12-bit pipelined ADC for the WLAN standard [5]. Although the maximum input frequency is 10*MHz*, analog signal separation can be done on the receive signal such that the inphase (I) and quadrature (Q) channels are separated before digitizing so that each channel only occupies 10*MHz* of bandwidth [7]. This is done with the use of surface acoustic wave (SAW) devices [7]. The structure of Mathur's pipelined ADC is shown in Figure 4-3.

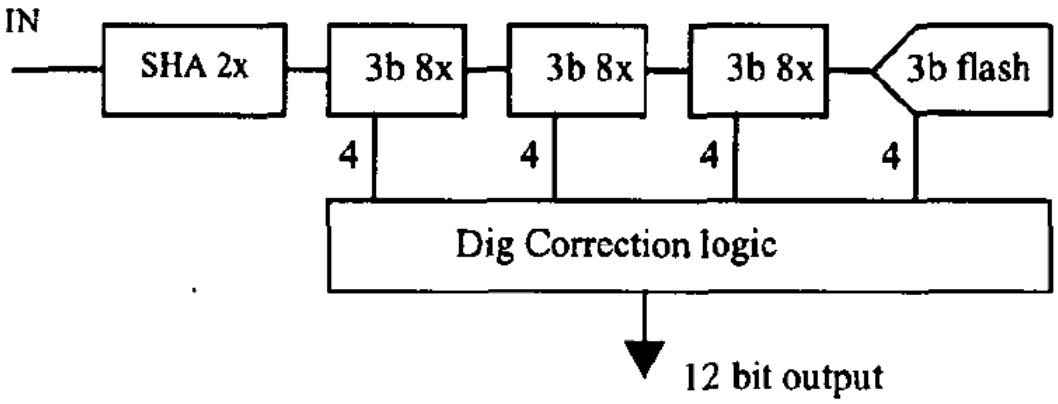

Figure 4-3 A 115*mW* 12-bit 50*MS/s* pipelined ADC [5].

The 12-bit output is divided into three 3-bit pipeline stages and a 4-bit final flash ADC stage. One extra bit for digital error correction is generated by the pipeline stages. The reasoning behind choosing 3 bits per stage is such that linearity, power consumption and speed can be compromised. Linearity increases as the first stage resolves larger number of bits. Power consumption decreases for fewer pipeline stages because less inter-stage amplifier is needed. However, speed is sacrificed because each stage has to resolve a higher number of bits. The pipelined ADC is implemented in a 0.18μm digital CMOS process for easy SoC integration. It has a sampling rate of 50*MHz* and a power consumption of 115mW.

5. Comparisons

From recent researches and technology advancement, both interpolation/averaging ADC and pipelined ADC promise to deliver adequate performance according to the IEEE 802.11a WLAN standard with low power consumption.

Pipelined ADC is more suitable for high speed and high resolution requirement. For medium resolution, 8-10 bit and even faster conversion rate, an interpolation/averaging ADC should be used. The power consumption of the two ADCs reported above is not a fair comparison because they fabricated using different processes with different supply voltages. The conclusion drawn here assumes that the same speed and process are used.

The advantage of digitizing earlier in the system architecture with a faster and higher power ADC is that the received data can be in digital form earlier. Processing the received data in digital form eliminates the linearity problem with analog component. Also, by enlarging the digital circuit boundary in the system, one can save chip area since digital components have a higher integration. This is a tradeoff between power consumption with the chip area and signal integrity. Usually, interpolation/averaging ADC is used when digitization is done earlier since they have a faster conversion rate. Pipelined architecture is used when digitization is done after the I and Q data separation to save power.

6. Conclusions and Future Directions

Recent research shows that by using redundant signed-digit (RSD) cyclic implementation, a variable resolution ADC can be designed [6]. Although this architecture only generates one bit per clock cycle and might not be suitable in today's wideband communication standard, the same idea can be applied in designing pipelined ADC. Circuitry can be designed to sense the channel condition and use the information to control the resolution of digitization. For

example, if the channel requires less resolution, a few pipeline stages can be shut down for power conservation.

In conclusion, depending on the system architecture, designer should choose an ADC architecture that will give them the best trade off between power consumption and performance. For digitization before the I and Q data separation, an interpolation/averaging ADC should be used since they give a faster conversion rate. If I and Q data separation is done with SAW devices, a pipelined ADC can be used since they give similar speed and slightly lower power consumption.

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