Analog to Digital Converters for Wireless LAN 802.11a

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Outline

Introduction IEEE 802.11a ADC Requirements Interpolation/Averaging ADC Pipelined ADC Recent Research Future Directions Conclusions

Introduction

IEEE 802.11a IEEE standard for Wireless LAN (WLAN) Operates in the 5Ghz frequency band Channel bandwidth of 20Mhz OFDM data modulation Variable data rate from 6-54Mbps

Typical 802.11a Transceiver



Note: Newlogic Inc. WiLD 802.11a radio

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ADC Requirements for IEEE 802.11a

8 - 10 bits of resolution
Low in power consumption
Input bandwidth of at least 20Mhz
Low in data latency

Interpolation ADC

- Fast in conversion rate
- Reduce effect of comparator offset
- Lower input capacitance
- Low in data latency
- Lower power consumption
- Averaging improves accuracy



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Interpolation ADC



4 bit ADC4X interpolation



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ADCs for IEEE 802.11a

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Pipelined ADC

- Less comparators neededLower power consumption
- Has latency problem
- Fast in conversion rate



Pipelined ADC

 One extra bit per stage
 Has digital error control
 Use redundancy to correct offset error



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Recent Research

- Interpolation ADC
- J. Vandenbussche, 2002
- 8 bit resolution
- Input bandwidth of 30Mhz
- 0.35um technology
- 300mW power consumption



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Recent Research

- Pipelined ADC
- S. Mathur, 2002
- 12 bit resolution
- Input bandwidth of 10Mhz
- Used only 4 stages to reduced latency
- 115mW power consumption
- 0.18um technology



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System Architecture and ADC

IEEE 802.11a has 20Mhz channel
 I and Q data each has 10Mhz
 Separation of I and Q data can be done in analog or digital domain

Digital domain separation

- Homodyne receiver
- Interpolation ADC
- Analog domain separation
 - Super-heterodyne receiver
 - Pipelined ADC

Future Direction

C. Aust designed variable resolution ADC based on the RSD cyclic algorithm 1 bit per clock cycle Too slow for IEEE 802.11a standard Apply this idea on pipelined ADC Dynamically change the number of pipeline stages to save power

Conclusions

- IEEE 802.11a is future standard for WLAN
- Required low power ADC
- High input bandwidth, 20Mhz
- Interpolation ADC
 - Moderate power consumption
 - Fast conversion rate
 - System with digital I/Q data separation
- Pipelined ADC
 - Lower power consumption
 - Moderate conversion rate
 - System with analog I/Q data separation