# *The Effect of $V_{DD}$ Noise on Phase Jitter*

## 1.0 Introduction

As the demand for better communication grow, higher system bandwidth is needed since larger amount of data is required to be transmitted in a given time. System today is running in the giga-hertz range, such as the microprocessor and the networking equipment, etc. The time period for the data is therefore less than a nano-second. In order to recover the data within the system, the clock that is driving the sample and hold circuit needs to be accurate down to the pico-second range.

Circuit designer is well aware of the fact that noise (thermal, shot or flicker, etc) will corrupt the signal within a system. To illustrate, consider a latch is used to sample the data that is on a wired channel and the clock signal used to drive the latch is corrupted by noise. The latch will be triggered at slightly different time, $\Delta t$, in every data period. If $\Delta t$ is large, it can severely change the result of the sampling since the data is changing at every nano-second for a 1GHz system.

Although circuit techniques as well as process enhancement has been done to reduce the effect of noise on the system, none of them can remove noise from the circuit completely. Thus, to ensure that the circuit is going to work in a noisy environment, it requires knowledge on how the noise will affect the operation of the circuit. In this paper, the effect of $V_{DD}$ noise on the phase jitter will be emphasized.

## 2.0 Phase Jitter

The output of a sinusoidal clock generator can be described mathematically by (1),

$$V_{out}(t) = A\cos(w_o t + \theta_o) \tag{1}$$

where $w_o$ is the frequency of clock is radian per second, $A$ is the peak amplitude and $\theta_o$ is the phase of the output waveform. However, when noise is present, it will create distort the clock waveform and create fluctuation in amplitude and phase. The output of the clock under influence of noise is described in (2),

$$V_{out}(t) = [A + V_n(t)]\cos[w_o t + (\theta_o + \theta(t))] \tag{2}$$

where $V_n(t)$ is the noise voltage and $\theta(t)$ is called the phase jitter of the clock output. To further illustrate the effect of phase jitter, consider the trapezoidal wave clock as shown in Figure 1.

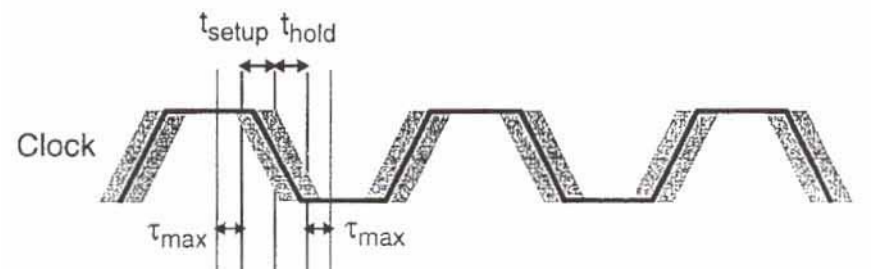


**Figure 1 Phase jitter in a trapezoidal wave clock signal.**

The solid black trapezoidal wave is the ideal clock output signal. The gray shaded regions represent the possibility of the occurrence of the clock edge. Due to noise, the clock transition can occur either some time before or after the ideal clock transition and this is referred to as phase jitter. In this particular example, it is assumed that noise causes no amplitude fluctuation.

Ricky Yuen
971339500


# 3.0 Time Varying Model

The phase jitter of an oscillator can be characterized by its phase impulse response [1]. Traditional phase jitter models [2] assumed the noise to phase jitter as a linear time invariant (LTI) system. Although this simplified resultant expression, the models are inadequate they are used in frequency domain analysis, which is called the phase noise spectrum. As a result, a linear time variant (LTV) model to characterize the effect of noise on the phase jitter is developed by Ali Hajimiri [1].

To prove why a LTV model is needed, consider the LC tank oscillator in Figure 2. Initially, the LC tank oscillator is producing a sinusoidal output with amplitude of $V_{\max}$. The current source $i(t)$ is injecting an impulse of current in time τ.

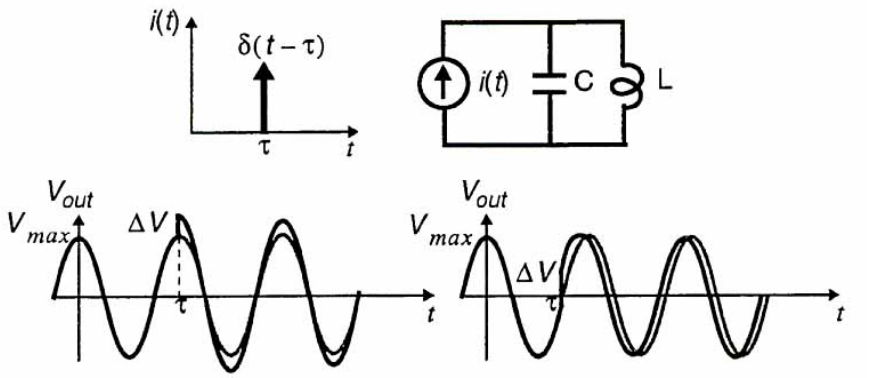


**Figure 2 The effect of an impulse signal on the phase of an oscillator.**

If τ happens to be occurring when the output of the oscillator is at its maximum, the impulse of current only creates a change in the amplitude of the $\Delta V$ in the output signal while the phase is not change. On the other

hand, if τ occurs during the transition of the output signal, the current impulse will create a phase change in the output signal with no amplitude change.

The above example illustrated that the effect of an impulse signal (noise) on the output of an oscillator depends on the time when the impulse is applied. This shows that a LTV model is needed to fully characterize the noise to phase jitter system.

## 4.0 Impulse Sensitivity Function

The equation (3) below found by Hajimiri is a LTV model that characterize the amount of phase shift caused by a given voltage (or current) impulse [1, 3].

$$\Delta\theta = \Gamma(w_o\tau)\times V_n(\tau) \tag{3}$$

$V_n(\tau)$ is the time varying noise voltage and $\Delta\theta$ is the amount of phase shift caused by $V_n(\tau)$ in the system. The function, $\Gamma(w_o\tau)$, describe how much phase shift will result from the noise voltage at time τ and the function is known as the Impulse Sensitivity Function (ISF). In this definition, the ISF has a unit of second per volt [sec/V]. For an oscillator with an oscillation frequency of $w_o$, the ISF is periodic with 2π.

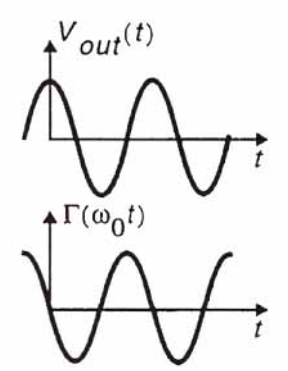


**Figure 3 The ISF of the LC tank oscillator.**

Figure 3 illustrates the use of the ISF on the LC tank oscillator previously described. As shown, the ISF has the maximum value when the output signal is at the transition and has a value of zero when the output is at its peak.

## 5.0 Characterization of the Clock Buffer in a Clock and Data Recovery System

As described in the introduction of the paper, it would be beneficial to characterize the effect of $V_{DD}$ noise on the clock and data recovery (CDR) system, Figure 4 [4], such that the design will work for a given minimum noise margin.

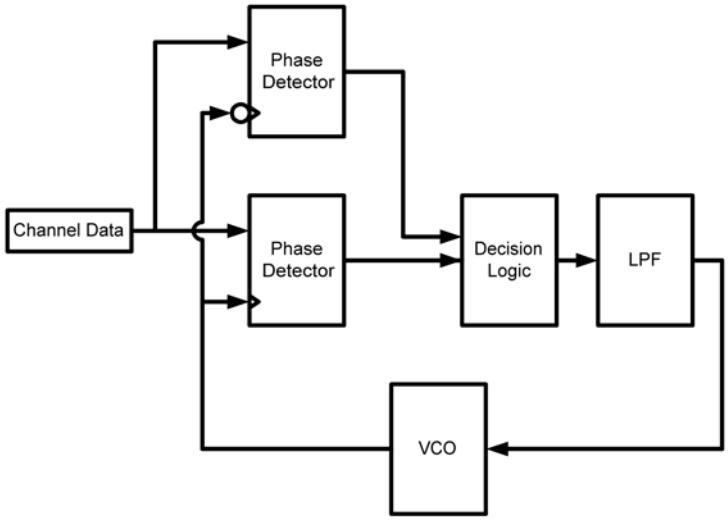


**Figure 4 A typical clock and data recovery system.**

An essential circuit in the CDR system is a clock buffer used to drive the phase detector for sampling of incoming data as shown in Figure 5. To characterize the effect of $V_{DD}$ noise on a traditional clock buffer, an ISF of the clock buffer is simulated.

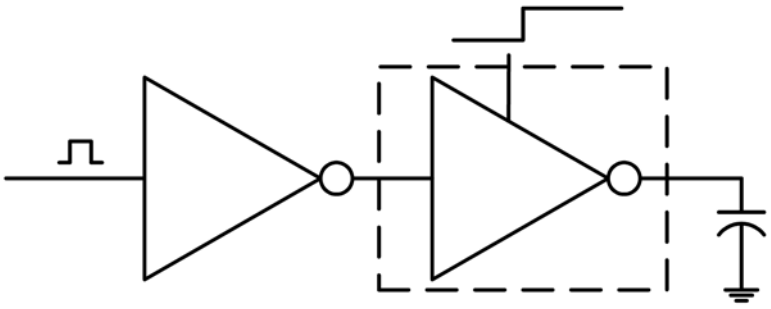

**Figure 5 A typical buffer used in a CDR system.**

Figure 6 shows the simulated ISF of the clock buffer. The top plot is the ISF while the bottom plot of Figure 6 shows the output transition of the clock buffer. Since only the positive edge of the clock is used to drive the following

stage, the negative edge will not be characterized, as it does not affect the operation of the rest of the circuit.

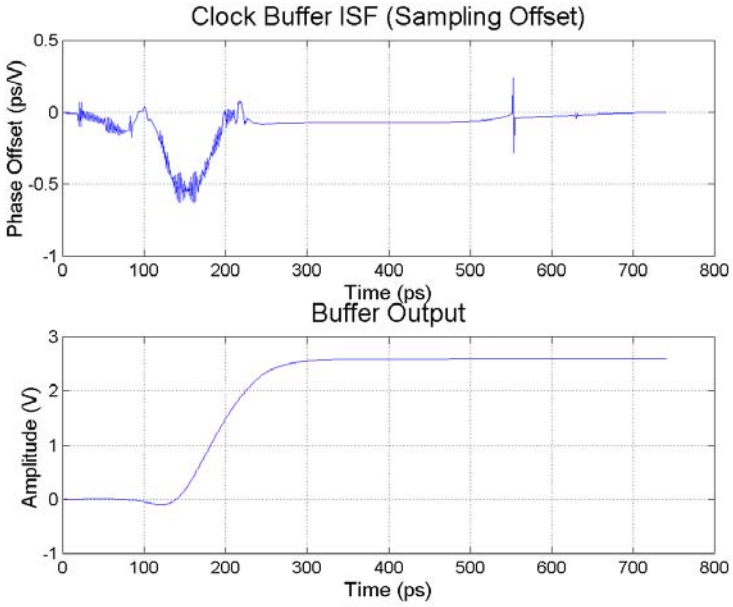


**Figure 6 The ISF of the clock buffer.**

As seen from the ISF, any noise that occurs during the output transition will create a negative phase shift of the clock edge. The maximum phase shift simulated is 0.5ps/V and that is resulted when the noise voltage appeared at the middle of the transition. The result is consistent with the finding from Hajimiri as the maximum of $\Gamma(w_o\tau)$ occurs at the middle of the oscillator transition.

# 6.0 Linearity

## *6.1 Property of Scalability*

An impulse response of a system satisfies the scalability and superposition properties. For the ISF to be useful in predicting the amount of phase jitter it creates at a particular time, the ISF should be scalable and additive. The ISF function in Figure 6 is measured with an impulse signal that is 1ps wide and 100mV in amplitude. The clock buffer is simulated again with 200mV and 300mV impulse signal. The resultant ISF are scaled by 1/2 and 1/3 respectively and plotted in Figure 7.

As shown in Figure 7, the scaled ISF overlapped nicely with the original ISF simulated with 100mV. This proved that the ISF for the clock buffer satisfied the scalability property.

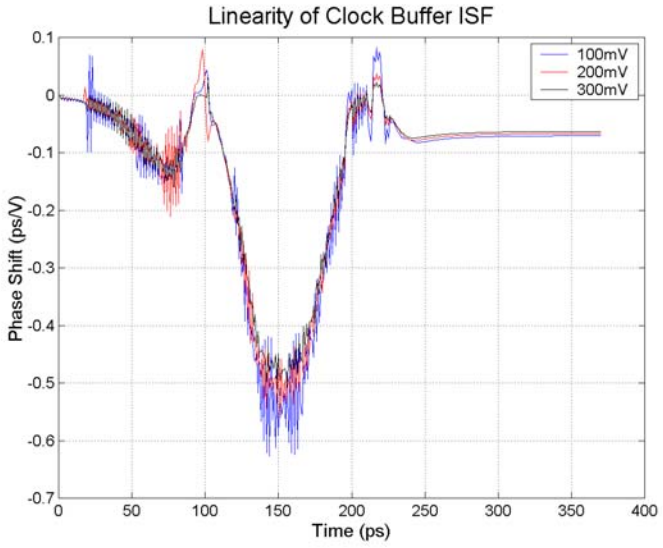


**Figure 7 Scalability of Clock Buffer ISF.**

### 6.2 Property of Superposition

Another property to verify for the ISF of the clock buffer is the property of superposition. To verify this property, $V_{DD}$ noise is applied to the clock buffer and the its ISF is measured. Next, $V_{DD}$ noise is injected into the phase detector alone and the ISF for the phase detector is measured. Their ISF are added together and is illustrated in Figure 8 as the red line. The blue line in Figure 8 shows the ISF of the system when $V_{DD}$ noise is injected into both the clock buffer and phase detector together. The two ISF plots again overlapped closely and this indicates that the ISF satisfies the superposition property.

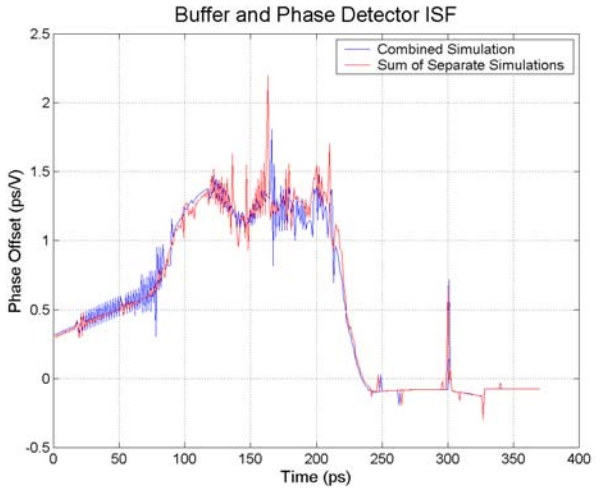


**Figure 8 Superposition property of ISF.**

## 7.0 General $V_{DD}$ Noise

To use the ISF to calculate the total phase error caused by the noise source, equation (4) can be evaluated.

$$\Delta\phi_{n-total} = \int_{nT}^{(n+1)T} V_{noise}(t)\Gamma(\omega_o t)dt \tag{4}$$

Since each value of the ISF represents the resultant phase error in pico-second due to 1V of noise signal at that particular time, the total phase error is then the sum of each noise voltage and ISF products over the time interval. This is equivalent to the dot product of the noise voltage and the ISF function as suggested by equation (4).

## 8.0 Result of ISF Estimation

The initial purpose of measuring the ISF is to predict the phase error results from the $V_{DD}$ noise. After measuring the ISF of the clock buffer and verifying its linearity, its accuracy must be confirmed.

In HSPICE, a 4Ghz, 100mV sinusoidal noise is applied to the power supply of the clock buffer. The phase error is then simulated for each delay of the sinusoidal noise source. The result is illustrated in Figure 9. The horizontal axis shows the delay of the sinusoidal noise source while the vertical axis gives the phase error caused by the sinusoidal noise source.

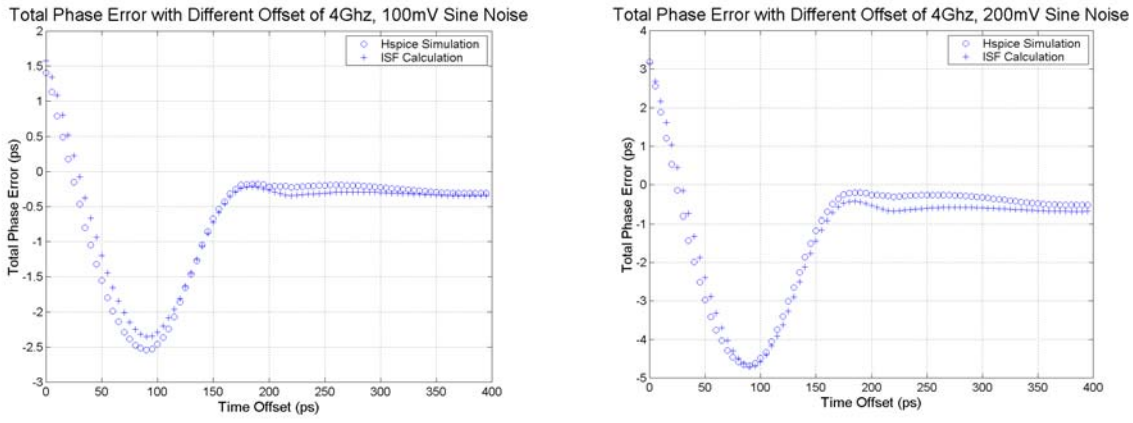


**Figure 9 Comparison between HSPICE and ISF calculation.**

As seen from Figure 9, the graph with small circle represents the result from HSPICE simulation and the graph with small plus sign is the result from ISF calculation. With zero delay of the sinusoidal noise, the 100mV noise signal creates 1.5ps phase error in the clock buffer. For a 200mV noise signal, it causes 3ps phase error. This again verifies the scalability of the ISF result. As the delay of the noise signal increases and passes the highest point of the ISF function (200ps), the amount of phase error reduced to a very small value.

The difference between the HSPICE simulation and the ISF calculation result differ by at most 0.5ps. This can be safely ignored since the simulation time step used is higher than this value and the error can be refer to the numerical error that is internal to the simulator itself.

## 9.0 Approximation in the Frequency Domain

To perform dot product as equation (4) suggested could be time consuming especially when the length of the time interval is long. However, as communication theory suggested, time domain convolution can be treated as frequency domain multiplication. This idea will greatly simplify the amount of calculation needed to perform when computing the total phase error.

Equation (4) can be re-written as,

$$\Delta\phi_{n-total} = \int \left( V^*_{noise}(f) \times \Gamma(f) df \right) \tag{5}$$

For $V_{noise}(t) = A\sin(w_o t + \theta_o)$, equation (5) can be simplified to (6),

$$\Delta\phi_{n-total} = \Gamma_R(f_o)\sin\theta_o - \Gamma_I(f_o)\cos\theta_o \tag{6}$$

where $\Gamma_R(f_o), \Gamma_I(f_o)$ are real and imagine components of the Fourier transform of the ISF function, as shown in Figure 10. Clearly, the amount of operations needed in equation (6) is much less than equation (4). The value of the Fourier transform of the ISF function can be pre-computed and stored in a table, which will further simplify the computational process.

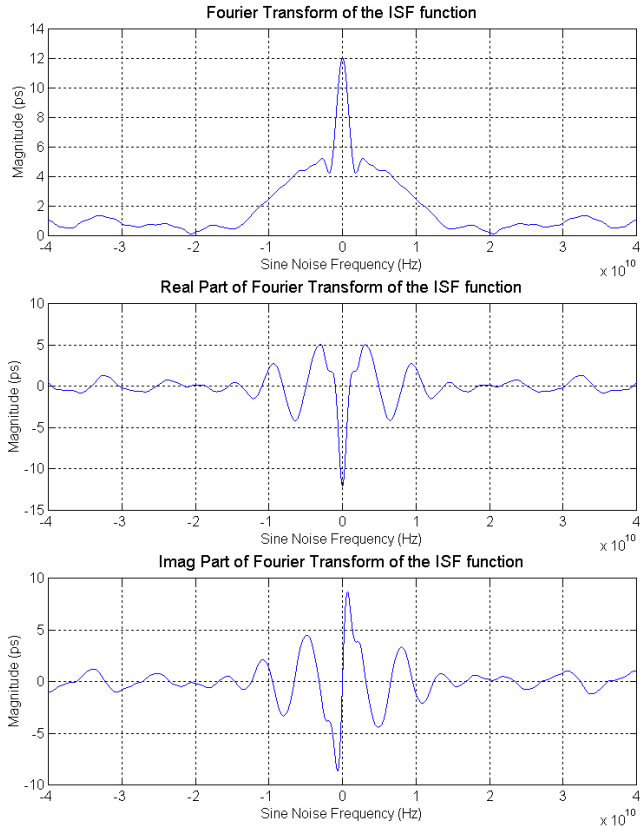


**Figure 10 Fourier transforms of the clock buffer ISF function.**

To verify the above expression, MATLAB simulations are done and their results are shown in Figure 11. The horizontal axis represents the sinusoidal noise frequency up to 40Ghz, and the total phase error is shown on the vertical axis. The plots for the ISF calculation using equation (4) and

equation (6) are plotted on the same graph and they overlapped completely as this shows that equation (6) is indeed valid.

Another verification of earlier result can be seen from Figure 11a. As the arrow points out, with $\theta_o = 0°$, a sinusoidal noise source with frequency equals to 4Ghz causes a phase error of 1.5ps and this agrees with earlier findings.

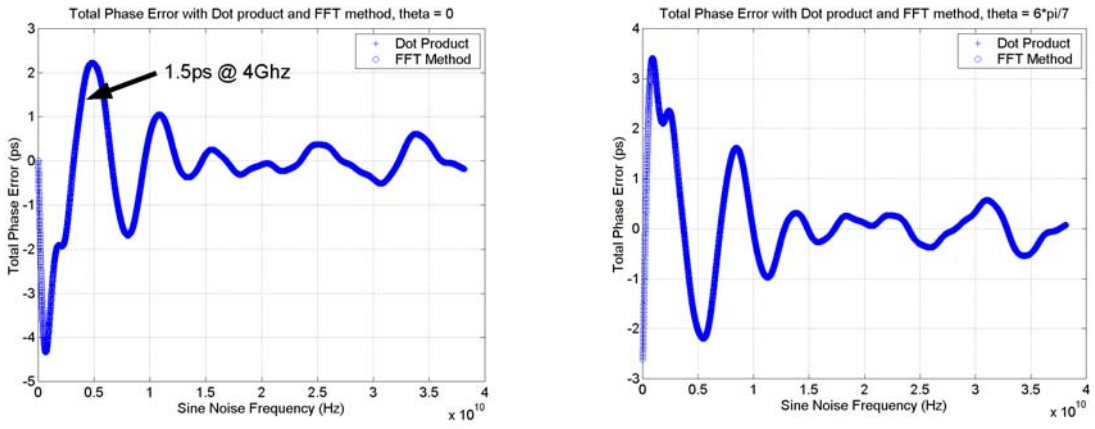


**Figure 11 Calculation of phase error in the frequency domain.**

## 10.0 Effect of Loading on ISF function

The load of the clock buffer plays a dominant role of the shape of the ISF function since it affects the rise time of the signal. Figure 12 shows the ISF of the same clock buffer when its load changes from 25fF to 100fF. As expected, with a small load of 25fF, the rise time of the clock buffer is the fastest and that yields an ISF that sustained only for 150ps (100ps-250ps). On the other hand, when the same clock buffer faces a load of 100fF, its rise time lengthens and its ISF still has significant contribution at 500ps.

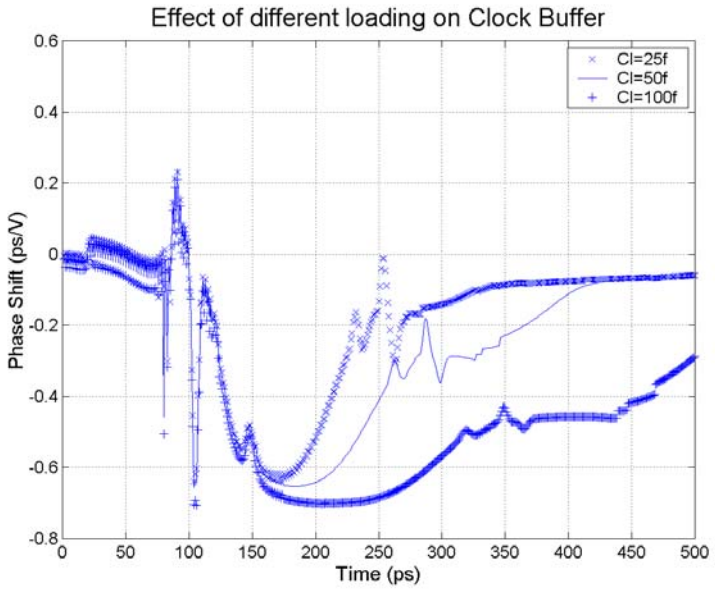


**Figure 12 Effect of loading on ISF of clock buffer.**

The effect does not appear to be linear with respective to the load the clock buffer faces. Things still need to be studied included:

1. ISF linearity for (load/rise-time)?
2. Property of superposition for cascaded clock buffers with identical loading.

# References

1. A. Hajimiri, T. Lee, A General Theory of Phase Noise in Electrical Oscillators, IEEE Journal of Solid-State Circuits, 1998.
2. J. Rutman, "Characterization of Phase and Frequency Instabilities in Precision Frequency Sources; Fifteen Years of Press," Proc. IEEE, vol.66, pp.1048-1174, Sept, 1978.
3. T. Lee, Oscillator Phase Noise: A Tutorial, IEEE Journal of Solid-State Circuits, 2000.
4. Hisakatsu Araki, "CDR Evaluation Model Specification", Fujitsu Laboratories Ltd., July 07, 2002.