

Laser Fired Emitter on n-type Silicon Using **Amorphous Silicon Passivation**

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INTRODUCTION

MOTIVATION

- High conversion efficiency of c-Si photovoltaics
- Excellent surface passivation using a-Si:H



FIG. 1: Schematic of the photovoltaic device with LFE, a-Si:H layers and isolation (oxide) layer.

- Low-thermal-budget fabrication process
- Amenable to thinner wafers
- Simple fabrication process

OBJECTIVES

- Demonstrate a-Si:H based LFE PV concept using SiO_x isolation layer
- Perform 2D modeling to evaluate the cell concept
- Conduct proof of concept experiments

LFE Spot i-aSi:H (40 nm) PECVD SiOx (105 nm) Back Contact (AI) (2 µm)

- Inverted cell
- n-type substrate
- Double-sided hydrogenated amorphous silicon (a-Si:H) passivation
- PECVD SiO_x Isolation layer
- ◆ Q-Switched Nd:YAG laser fired emitter (LFE)

SIMULATION OF THE CELL

- 2D modelling using Sentaurus
- a-Si:H representation with band-tail and band gap defects
- Lambertian front surface and completely reflective back surface

Half Grid Line Width \rightarrow



FIG. 2: A unit cell to represent the cell for 2D simulation. Surface passivation at the back is represented by low SRV between c-Si and SiO_x layer

PROOF OF CONCEPT

FABRICATION DETAILS

- Wafer: n-type FZ 20 Ω -cm, (100) orientation
- DC saddle field for a-Si:H deposition 170° C
- Ambient atmosphere 240°C anneal after amorphous deposition
- E-beam metallization
- Post device fabrication annealing in nitrogen atmosphere

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FIG. 3: Performance variation with (a) LFE pitch and damaged spot thickness (b) LFE diameter (c) Substrate thickness



FIG. 4: (a) Life time profile using µ-PCD (b) cell performance variation with LFE pitch (c) cell performance for annealing at different temperature, (d) IV characteristics for different annealing temperature (e) best cell performance after annealing.

SUMMARY

- Potential efficiency of 20%
- The cell structure is suitable for thin wafers
- Optimal LFE width is 15 µm with 5 µm thick laser-damaged zone

SUMMARY

- Demonstrated cell efficiency of >11%
- Optimum cell performance found at 150 µm LFE pitch
- Annealing up to 250°C increases cell performance with minimal lifetime gain, suggesting a mitigation of the laser-damaged zone

CONCLUSIONS

- Demonstrated viability of a-Si:H/SiO_x rear stack in an LFE PV device
- Proof of concept cell efficiency of >11% demonstrated
- Cell configuration has 20% efficiency potential

References

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