Zahidur Chowdhury

Back Amorphous-Crystalline Silicon Heterojunction Photovoltaic Device: A Parametric Study

Zahidur R. Chowdhury[1‡], and Nazir P. Kherani[1,2*]
[1]Department of Electrical and Computer Engineering, University of Toronto, Toronto, Ontario, Canada
[2]Department of Material Science and Engineering, University of Toronto, Toronto, Ontario, Canada
[‡]zr.chowdhury@utoronto.ca; *kherani@ecf.utoronto.ca

Abstract
Low temperature processed ultra-thin wafers for solar cell manufacturing can further lower the cost of silicon photovoltaics (PV) both at the cell level and panel installation. Excellent surface passivation quality is required to facilitate the fabrication of high efficiency PV cells using ultra-thin wafers. Fabrication of low cost cells using such processing schemes is viable because of the reduced material costs and lower thermal budget.

A novel low temperature (≤400° C) passivation scheme has been proposed for crystalline silicon surface passivation using native oxide-PECVD silicon nitride (SiNx) dual layers. High quality surface passivation has been reported for the passivation scheme [1]. Moreover, compared to other low temperature passivation schemes (*e.g.*, hydrogenated amorphous silicon) the proposed passivation has reduced parasitic optical absorption and light induced degradation effect.

A series of photovoltaic devices, including the Back Amorphous-Crystalline Silicon Heterojunction (BACH) cell, have been fabricated using this native oxide based passivation scheme. This article presents a systematic experimental study on the performance of the BACH cell with different cell design parameters; key cell parameters include interdigital gap between the back-contact doped regions, *n*-width and ratio of *p* to *n*-doped regions. Maximum photovoltaic conversion efficiency of 16.7% is obtained for an untextured cell illuminated under AM 1.5 global spectrum with V_{OC} of 641 mV, J_{SC} of 33.7 mA-cm^{-2} and fill-factor of 77.3% [2]. A study predicting the improved cell performance for a textured front surface with dual-layer ARC and suitable metal contacts with reduced resistivity will be presented in the talk. Also, cell efficiency projections for the optimized cell design parameter will be presented for an ultra-thin silicon wafer.

References
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