Novel method for fabricating high efficiency 10 μm thick c-Si solar cells

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***Abstract* — The most straightforward route to reducing the cost of c-Si photovoltaics is to make cells thinner. However, as cell thickness is reduced, light absorption is compromised. This necessitates the use of light trapping mechanisms to mitigate reduction in absorption. In this paper, we present a novel method to fabricate a high efficiency solar cell on a 10 μm thick silicon membrane. The method involves in-house fabrication of 10 μm thick membranes and integration of optically efficacious inverted pyramid texture with feature size and pitch on the order of the solar wavelength via a resist-free laser-writing method.**

***Index Terms* — thin absorption, alkaline etching, crystalline-silicon, photovoltaic cells, surface texture, thin film devices, light trapping, direct laser writing.**

I. Introduction

Single junction photovoltaic cells made from c-Si are approaching their practical limits in efficiency. With smaller margins for improving efficiency, much research efforts have turned towards driving down the cost of these devices. The most straightforward way to do this is to make thinner cells (i.e. use less material). However, as cells are made thinner they begin to experience greater transmission losses. This necessitates the use of light trapping (LT) schemes to overcome these losses and maintain reasonable light absorption in the cell. The most common scheme for LT in silicon is surface texturing. Inverted pyramid structures are etched onto the surface, and serve to bend light into the cell. For typical thick silicon cells, surface textures have feature sizes on the order of microns. For example, a grating texture of 9 μm inverted pyramids (IP) has been used to demonstrate the highest efficiency 400 μm thick c-Si photovoltaic device [1]. These feature sizes are incompatible with cell thicknesses on the micron scale since most of the cell's active thickness would be consumed in the texturing process. As well, large textures exhibit poor light trapping. Optical modeling studies have shown that textures with periodicity and feature sizes comparable to the wavelength of light are more suitable for light trapping, since they diffract light at high angles into the cell [2]. Micron scale periodic texturing of the silicon surface is generally achieved using a lithographic process that involves spin coating of resist [3,4]. Because thin silicon membranes cannot withstand spin coating, textured silicon membranes can only be obtained by post-thinning [4] of thick (textured) silicon which involves huge loss of silicon during this post-thinning step. However, for 20 μm thick free-standing c-Si membranes available in the market [5] it was necessary to design a new texturing process which involves minimum handling and breaking.

We present a resist-free contactless integration of wavelength-scale inverted-pyramid textures onto a 10 μm thick c-Si membrane for low cost high efficiency solar cells. The texturing process involves laser patterning of a silicon nitride hard mask deposited on the device layer of a silicon-on-insulator (SOI) wafer. This is followed by the thinning of the SOI wafer and the alkaline etching of the exposed silicon into inverted pyramidal features formed by slow etching (111) planes. Our group has previously demonstrated wavelength-scale IPs [6] and membrane solar cells [7].

II. Integrated Device

Firstly, IP textures are fabricated on the 10 μm thick device layer of an SOI wafer (Fig 1 a). To fabricate wavelength scale textures, we perform high resolution laser writing of a hard-mask on the Si surface [6]. The process involves selective delamination of a thin-film dielectric (silicon nitride) coating on c-Si (001) using ultra-short pulses followed by anisotropic etching of the exposed Si into an IP lattice. A 100 kHz femtosecond pulsed fiber laser with λ = 522 nm was used to blister (Fig 1 a) and catapult (Fig 1 b) a thin dielectric coating on c-Si (001) to form to form a pattern of shallow ablation craters on (001) c-Si which thereby enables chemical etching of Si into an IP array (Fig 1 c). A 20 nm thick silicon nitride (SiN dielectric layer grown by Plasma Enhanced Chemical Vapor Deposition) was used as an optimal hard-mask to obtain the smallest possible mask aperture while effectively masking Si selectively during etching. A 30% KOH (potassium hydroxide) solution at 60°C was used to achieve smooth etching.

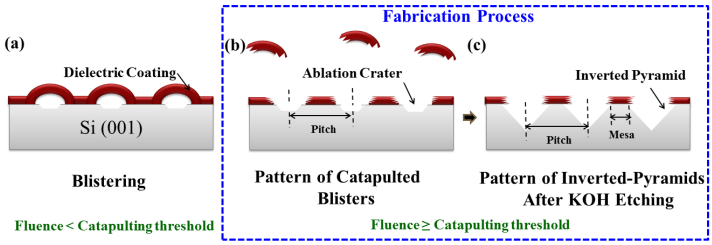

Fig 1. A schematic illustrating a) blistering of a dielectric coating upon interaction with femtosecond pulses, b) catapulting of blisters at higher laser fluence to form a pattern of shallow ablation craters in c-Si, and c) the resulting inverted pyramid structure following KOH etching.

After systematically investigating the ablation crater diameter and the effect of KOH over a broad range of single pulse exposure conditions, the laser fluence of 0.45 J/cm^2 and KOH etching time of 2.5 minutes was selected as optimal to reproducibly form the smallest (1.13 µm wide) IP structure without any visible damage. Further, the craters produced at optimized fluence were tightly packed with a 1.5 µm pitch in two orthogonal directions to form a grid with minimum collateral damage and etched into a high fidelity array of IPs. The IP size can be varied from 1.13 µm to 1.3 µm by regulating the KOH etching time.

The method results in high fidelity IP texture with wavelength scale features having defect rates of less than 1 in 10^4 (Fig 3). The technique permits control over the positional placement and size of the IP in the texture during processing, which is necessary for the attainment of optimal high efficiency texture design. The method is scalable for large area micro-fabrication of thin c-Si PVs.

To study the effectiveness of wavelength scale IPs compared to larger textures, we have also investigated an array of 5 µm wide IPs. These are fabricated using standard photolithography. An SEM image of this array is presented in Fig. 4.

Once the texturing is completed, a 10 µm thick silicon membrane is formed by thinning down the SOI wafer. The textured membrane is then converted into a photovoltaic cell. A hole with diameter of 1 cm is chemically 'drilled' into the SOI handle wafer using a custom etching apparatus immersed in a solution of potassium hydroxide (KOH) until the device layer is reached. The process flow is depicted schematically in Fig. 2.

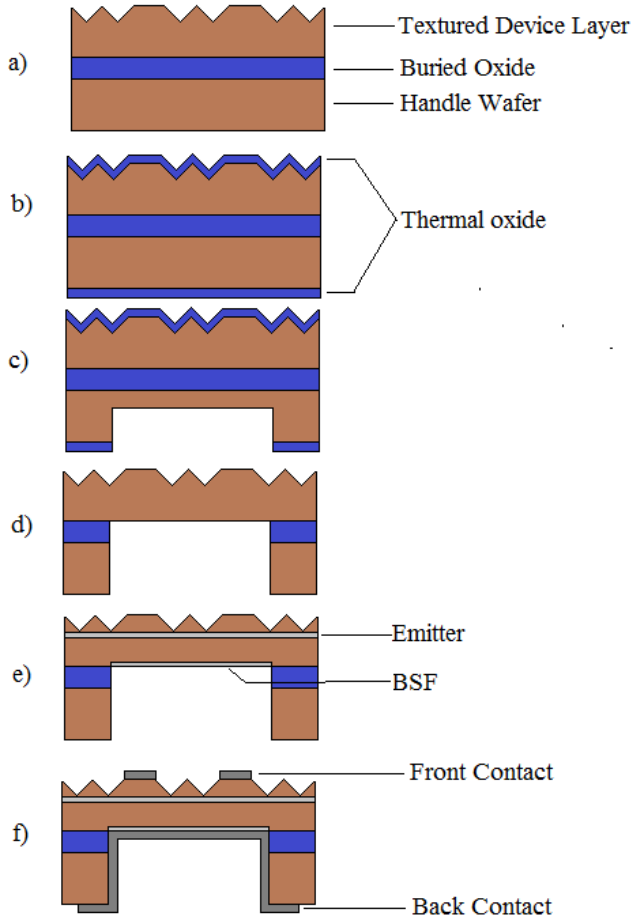

Fig 2. Schematic of membrane process flow. The device layer of an SOI wafer was first textured (a), the sample was cleaned and then a protective thermal oxide was grown on its surface (b). A circular area 1 cm in diameter was removed from the handle wafer via KOH etching (c,d). The buried oxide and thermal oxide are removed with BHF (d). The n-type emitter and p-type back surface field were created using ion-implantation (e). The sample was then cleaned, annealed and lastly, metallized using e-beam evaporation through a shadow mask (f).

After the creation of the textured silicon membrane an n-type emitter is doped into the front surface by ion-implantation. A p-type back surface field is then doped into the rear of the membrane using ion-implantation of boron. The sample is then cleaned again using the RCA procedure and annealed using a three-step process [8]. Front and rear Ti/Pt/Au contacts are deposited using e-beam evaporation (Fig. 2 (f)). The entire back surface is metallized, whereas the front side uses an optimized mask pattern. Finger width and spacing were determined by the optimization calculations given in [9]. The optimization considered resistive power losses in the emitter layer and the metallization versus the

shadow losses of the metallization. To improve contact to the silicon surface, the regions directly under the fingers are left untextured using computer controlled stages during the texturing step.

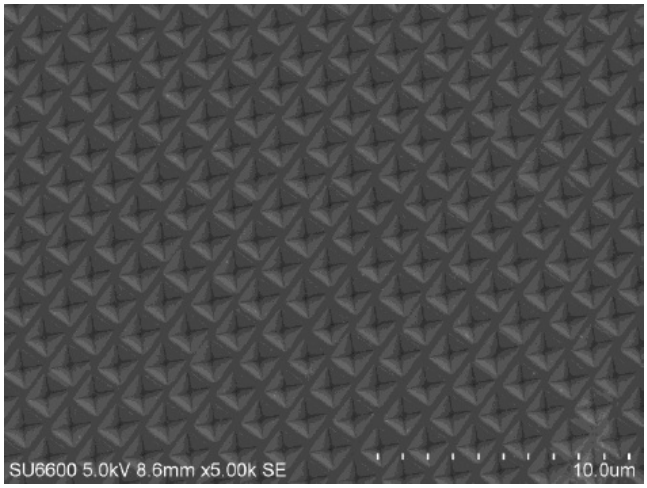

Fig 3. Fabricated high fidelity array of 1.3 μm inverted-pyramids at 1.5 μm pitch

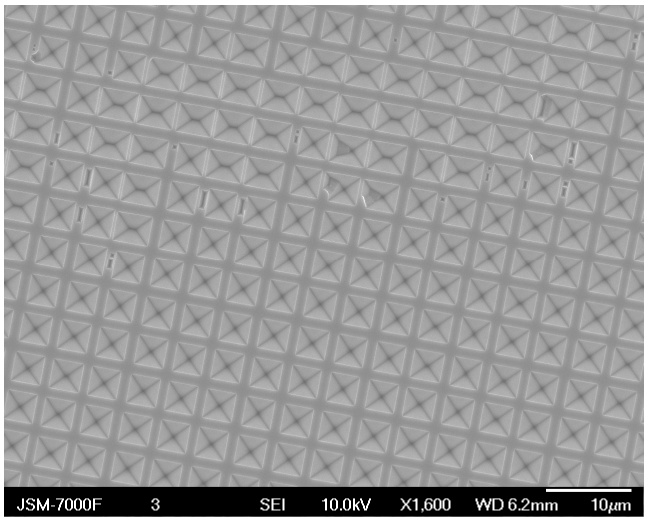

Fig 4. Fabricated high fidelity array of 5 μm inverted-pyramids

We expect surface texturing to benefit the membrane solar cell performance in two ways. Firstly, texturing acts as an effective anti-reflection medium. With a 1.3 μm pitch, we have observed a reduction in the surface reflectance from 34.7% (untextured) to 13.6% on a silicon surface [6]. The anti-reflection effects of the texturing are expected to improve the spectral response of the cell over a broad range of wavelengths. Secondly, texturing acts as a diffraction grating and redirects light into the cell laterally, increasing its pathlength thus enhancing its absorption. Light diffracted beyond the critical angle undergoes total internal reflection, completely trapping it inside the cell. Since the absorption pathlength for infrared photons is very small in silicon [10], we expect to see significant enhancements in external quantum efficiency (EQE) in the infrared region of the spectrum. Detailed optical wave simulations of an ideal 10 μm cell predict an efficiency of 21.9% for a cell with texturing vs 12.07% without. If a back reflector is included, the predicted efficiency of the textured cell is 23.2%

IV. Results

Three samples have been prepared for this study. Sample 1 is a fully functional membrane solar cell without front surface texturing. It was fabricated from the procedure outlined in Fig 2 from steps b) to f). This sample serves as a control to test textured membrane cells against. Sample 2 is a membrane textured with the 5 μm wide IPs. This sample was fabricated up to step d) in the procedure in Fig 2. Sample 3 was a silicon wafer textured with the 1.3 μm IPs.

For sample 1, a layer of silicon nitride is deposited on the surface via sputtering to serve as an antireflection coating (ARC). The coating is designed to minimize reflectance at 500 nm, the peak of the solar spectrum. The cell's short circuit current density, open circuit voltage, fill factor, and efficiency under AM1.5G spectrum conditions were 22.7 mA/cm^2, 0.55 V, 0.67, and 8.4 % respectively.

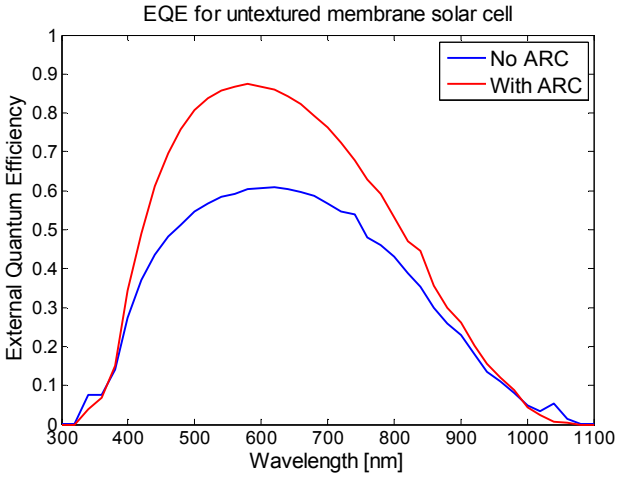

Fig 5. External Quantum Efficiency (EQE) measurements for untextured membrane solar cell, with and without an antireflection (ARC) coating.

External quantum efficiency (EQE) data for this cell is shown in Fig. 5. EQE measurements were taken both prior to and following ARC deposition. Firstly, it can be seen that energy

conversion suffers at long wavelengths, especially for wavelengths greater than 800 nm where the EQE drops below 50%. Secondly, the addition of the ARC does not strongly affect the EQE at longer wavelengths. This is due to the small absorption constant in silicon for wavelengths near the band edge. Clearly light trapping is necessary to improve energy conversion in this region of the spectrum.

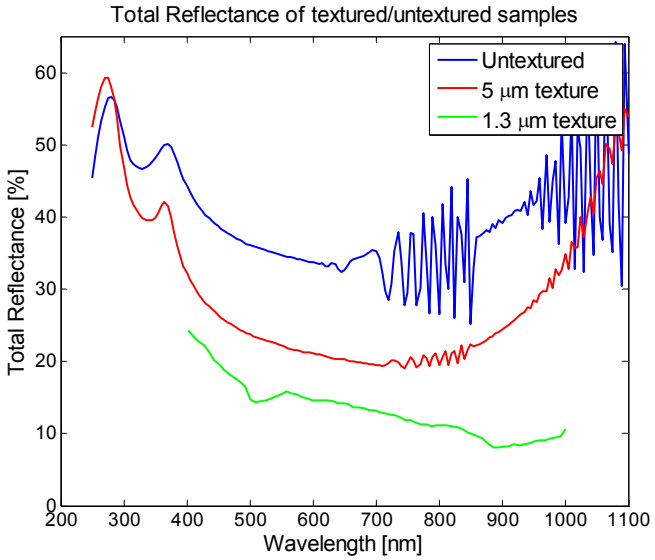

Fig 6. Total reflectance for sample 2, sample 3 and untextured membrane.

Total reflectance measurements for sample 2, sample 3, and an untextured membrane with no ARC are shown in Fig. 6. We can see that the IP texturing suppresses reflection across the entire solar spectrum, with the most improvement coming from the 1.3 μm IPs. These wavelength scale IPs result in a considerable (over 30% at some wavelengths) reduction in total reflectance. Total reflectance can be further suppressed with an ARC. It should be noted that since the 1.3 μm IPs are fabricated on a silicon wafer, the total reflectance cannot be directly compared with the membrane samples for wavelengths above 700 nm. Above this wavelength the absorption coefficient in silicon is small enough that light reflected from the back surface of a 10 μm thick membrane can escape through the front side.

IV. Summary

We have fabricated a photovoltaic device that can integrate wavelength-scale light trapping structures into a 10 μm thick solar cell. The textures are designed to be compatible with c-Si cells on the order of tens of microns of thickness. We expect texturing to increasing light absorption in the cell through its anti-reflection effect (surface reflectance is reduced from 34.7% to 13.6% for a textured vs. untextured Si surface), and through its diffraction effect which redirects light laterally into the cell. The bifacial nature of the cell architecture allows transmission losses to be measured directly. This architecture is thus well suited for characterizing the effectiveness of light-trapping structures, essential for their optimization. Combining transmission measurements with reflection measurements, we are able to directly determine the total optical absorption in the silicon cell and evaluate the performance of different light trapping approaches.

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