Facile Nanometer Thick Native Oxide Based Passivation of Silicon for High Efficiency Photovoltaics

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Abstract

Fabrication of low cost solar cells using ultra-thin (approximately 20 μm) silicon wafers is a viable route given the significant potential of reduced material cost and its versatility to a range of portable and terrestrial applications. Low temperature processing is a compelling opportunity for the synthesis of high-efficiency ultra-thin silicon wafers. Further, excellent surface passivation attainable through facile low temperature processing techniques is an essential enabler for effective manufacturing of ultra-thin silicon solar cells, and thus paving the way for high-efficiency low-cost silicon foil photovoltaics. This article presents a novel low temperature passivation scheme using approximately 1 nm thick facile native oxide and 75 nm PECVD SiN_X. A maximum lifetime of 1.7 ms has been obtained for the passivation scheme. Moreover, the passivated wafers were also used to fabricate Back Amorphous-Crystalline Silicon Heterojunction (BACH) cells using double side polished *n*-type FZ wafers. A maximum cell efficiency of 16.7% is obtained for facile native oxide - PECVD SiN_x bilayer passivated cells having V_{OC} of 641 mV, J_{SC} of 33.7 mA/cm^2 and fill-factor of 0.77 for a 1 cm^2 untextured cell (all measurements having been performed under AM 1.5 global spectrum illumination).

Introduction

Over the last three decades crystalline silicon (cSi) based solar cells have undergone remarkable technological advances, experienced a significant drop in silicon feedstock cost, and today are at or approaching grid parity in a number of regions of the world [1].

The next step in the evolution of silicon photovoltaics is the realization of high efficiency ultra-thin silicon photovoltaics (PV), rendering silicon PV an inevitable economically competitive reality. In this framework the advent of amorphous-crystalline silicon heterojunction PV coupled with compatible low temperature passivation schemes [2] provide a path for the production of high efficiency silicon foil solar cells.

The interface quality of the absorbing material of a solar cell, especially as the absorber thickness (silicon foil) becomes smaller, plays a great role in determining the cell performance. The interface quality at the native silicon oxide - crystalline silicon junction has traditionally been deemed to be of poor and non-uniform quality *vis-à-vis* its interfacial defect density. Contrary to conventional wisdom, we have recently demonstrated that the controlled growth of native oxide on crystalline silicon followed by an over layer of silicon nitride yields a high quality silicon oxide - silicon interface with reduced defect density [3]. This paper details the growth and characterization of facile native oxide-silicon nitride (*f*-SiO_X-SiN_X) passivation layer, showing the attainment of low surface recombination velocity, and illustrating its application for high-efficiency silicon photovoltaics.

The *f*-SiO_X-SiN_X passivation scheme is a low temperature scheme and is suitable for ultra-thin silicon wafers. The excellent surface passivation quality is achieved not only by reducing the dangling bond density at the interface but also through suitable charge density at the interface that results in field passivation. Consequently, the positive charge density of the *f*-SiO_X-SiN_X passivation layer also serves as the front surface field for *n* type cSi wafers. Moreover, wide band-gap materials used in the passivation scheme results in reduced parasitic absorption at the front surface. Also, the use of ultra-thin facile silicon oxide, placed between SiN_X and cSi, makes the passivation scheme more suitable from a light trapping perspective in comparison with passivation schemes where thicker (greater than or equal to 10 nm) thermal oxide and PECVD SiN_X are used [4-7]. Excellent passivation qualities in terms of surface recombination velocities (SRV) have been reported for alternative passivation schemes. Specifically, SRVs of 10 cm/s [4-7] and 6 cm/s [4] were reported for the thermal oxide (10 nm thick)-SiN_X and PECVD oxide (50 nm thick)-SiN_X passivation schemes, respectively.

This article presents a novel passivation scheme with an ultra-thin layer of native oxide (approximately 1 nm) grown at room temperature followed by the deposition of PECVD SiN_X layer at 400°C on cSi surfaces. The passivation scheme was then integrated within the Back Amorphous-Crystalline silicon Heterojunction (BACH) photovoltaic cell [8], substituting for hydrogenated amorphous silicon or alternative passivation schemes, in order to demonstrate the potential of the novel passivation scheme for high efficiency silicon solar cells.

Experimental details

n-type double-side polished 300 μm thick (100) FZ crystalline silicon wafers with 1-5 Ω resistivity were used for this study. The wafer was passivated using *f*-$SiO_x$and PECVD SiN_x. The *f*-SiO_x was grown in a controlled clean room ambient at room temperature for different time period to determine the suitable growth time or/and the suitable native oxide thickness. At the conclusion of the facile native oxide growth period, 75 nm

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thick SiN_X layers were deposited using Oxford PlasmaLab 100 PECVD tool. Once the surfaces were passivated, subsequent processing steps were carried out to fabricate the BACH cell by selective etching of SiN_X layer from the back surface and depositing approximately 20 *nm* thick *n* and *p* doped hydrogenated amorphous silicon (aSi:H) layers. Chrome-silver metal layers were deposited on the back surface using *e*-beam evaporation.

The oxide thicknesses were measured using parallel angle resolved x-ray photoelectron spectroscopy (PARXPS). Theta Probe from Thermo Scientific™ was used for the PARXPS measurements. The excess carrier density (ECD) dependent effective minority carrier lifetime, τ_{eff}, was measured using a Sinton Silicon Lifetime Tester WCT-120 system. Transient and Quasi-Steady-State Photo-Conductance (QSSPC) methods were used to measure injection-dependent τ_{eff} of the sample. Spatial distributions of the lifetime of the sample were measured using Semilab's WT-2000 PVN Microwave Photo Conductance Decay (μ-PCD) instrument.

The *I–V* characteristics were measured using the neonsee's IV AM 1.5 Solar Simulator. The light intensity was adjusted using a calibrated cell. The aperture area of 1×1 cm^2 was defined by a shadow mask on the cell front side for cells having approximately the same cell area.

Results and Discussion

Oxide Growth Time (OGT) on silicon surface in cleanroom ambient was varied from 20 min to 40K min for the *f*-SiO_X-SiN_X passivation of crystalline silicon. PARXPS shows that the oxide growth saturates to a thickness of approximately 1nm in 40K minutes. Moreover, the passivation quality also depends on the thickness of the facile oxide layer. Accordingly, a small enhancement in passivation quality with the increased OGT was observed for the passivation scheme where OGTs were below 20K minutes. Excellent passivation quality, having SRV values lower than 20 cm/sec with increasing OGTs, were realized for OGTs above 20K minutes. A maximum minority excess carrier lifetime of approximately 1.7 ms was obtained for this passivation scheme as measured using the Sinton Lifetime Testing Instrument for a facile oxide layer grown for four months. Fig. 1 shows the spatial profile of the passivation quality achieved using *f*-SiO_X-SiN_X as measured by the µ-PCD instrument.

Multiple cells were fabricated in a wafer where the cells had different doped-region widths and varying inter-digital gaps (IDGs) between doped-regions. The width of the *n*-doped hydrogenated amorphous silicon (a-Si:H) region varied from 180 µm to 410 µm while the ratio of *p*-doped region width to *n*-doped region width (*p*/*n* ratio) was varied from 2.1 to 2.67. The *n*-width to the IDG ratio (*n*/IDG ratio) was also varied from 1.5 to 4. The maximum cell efficiency obtained for *f*-SiO_X-SiN_X passivation was 16.7% with V_{OC} of 641 mV, J_{SC} of 33.7 mA/cm^2 and fill-factor of 77% under AM1.5 solar spectrum; the corresponding IV curve is shown in Fig. 2.

Conclusion

The novel facile native oxide and PECVD SiN_X bilayer passivation provides excellent surface passivation for crystalline silicon surfaces. A maximum lifetime of 1.7 ms was obtained for this low temperature passivation scheme. BACH cells with different design conditions were successfully fabricated using the passivation scheme on a double side polished crystalline silicon wafer. The maximum cell efficiency of 16.7% was obtained for *f*-SiO_X-SiN_X passivation under AM1.5 solar spectrum.

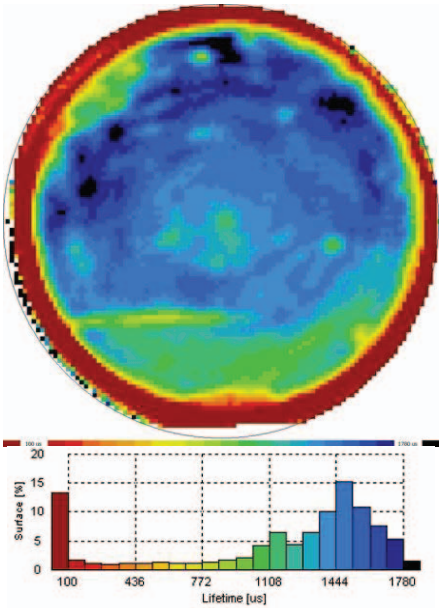

Fig. 1 Passivation quality achieved by *f*-SiO_x - SiN_x passivation measured using µ-PCD.

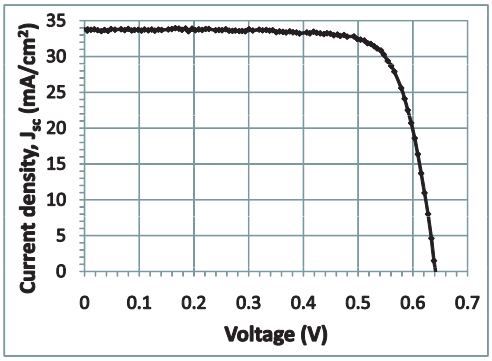

Fig. 2 IV curve for the BACH cell with maximum cell efficiency of 16.7% with V_{OC} of 641 mV, J_{SC} of 33.7 mA/cm^2 and fill-factor of 77% under AM1.5 solar spectrum.

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