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High-quality surface passivation of silicon using native oxide and silicon nitride layers

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We report on the attainment of high quality surface passivation of crystalline silicon using facile native oxide and plasma enhanced chemical vapour deposition SiN_x. Using systematic measurements of excess carrier density dependent minority carrier lifetime, it is observed that the inferred interface defect density decreases with increasing native oxide thickness while the interface charge density remains unchanged with thickness, which ranges from 0.2 Å to 10 Å. A surface recombination velocity of 8 cm/s is attained corresponding to a native oxide layer thickness of ∼10 Å. Similar chemically grown oxide layer followed by SiN_x deposition is shown to yield comparable passivation, indicating practical viability of the passivation scheme. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4733336]

Excellent surface passivation of crystalline silicon using low temperature processes enables the use of ultra-thin wafers for photovoltaic (PV) solar cell manufacturing, thus paving the way for high-efficiency low-cost silicon photovoltaics. Fabrication of low cost cells using such schemes is viable because of the reduced material costs and low thermal budget. Low temperature deposition of hydrogenated amorphous silicon (aSi:H),[1,2] plasma enhanced chemical vapour deposition (PECVD) of silicon oxide (SiO_x),[3,4] PECVD silicon nitride (SiN_x),[3–7] and PECVD silicon carbide (SiC_x)[8] have been reported as potential passivation compounds for crystalline silicon (cSi) surface.

Out of these passivation schemes, PECVD SiN_x has been studied extensively. Stoichiometric SiN_x is deemed more suitable owing to its lower absorption in the UV region compared to silicon rich SiN_x. Further, stoichiometric SiN_x has better chemical etching selectivity against cSi than silicon rich SiN_x,[6] which is desirable where selective etching of SiN_x is necessary for device fabrication. High values of fixed positive charge density, Q_s, at the cSi-SiN_x interface leads to field effect passivation in the case of nearly stoichiometric SiN_x. Charge densities of more than $10^{12}\,cm^{-2}$ have been reported.[9,10] But an induced inversion layer due to the high trapped charge density can lead to parasitic shunting which reduces the short circuit current.[11] A thin layer of thermally grown SiO_2 (Refs. 12–14) or low temperature PECVD oxide[15] layer is deposited between the cSi surface and SiN_x layer in order to reduce or remove the parasitic effect. Excellent passivation using these schemes has been reported, with surface recombination velocity (SRV) of 10 cm/s (Refs. 10, 12–14) and 6 cm/s (Ref. 10) for the introduced thermal oxide (10 nm thickness) and PECVD oxide (50 nm thickness) layers, respectively.

This article reports attainment of excellent surface passivation of *n*-type float zone (FZ) crystalline silicon using controlled facile native oxide growth at room temperature followed by the deposition of low-temperature PECVD SiN_x. Contrary to the conventional practice of etching, the native amorphous silicon oxide layer using hydrofluoric acid prior to SiN_x deposition, we show that the presence of a facile native oxide layer, denoted $f\,SiO_x$, plays a critical role in reducing the interface dangling bond defect density, N_s. Using the dangling bond interface recombination model,[16,17] we infer N_s and Q_s from excess carrier density (ECD) dependent lifetime measurements, showing interface defect density as low as $7.2 \times 10^9\,cm^{-2}$ and surface charge density of $4.3 \times 10^{11}\,cm^{-2}$ which correspond to a SRV of less than 8 cm/s at ECD of $10^{15}\,cm^{-3}$ (7 cm/s at ECD $5 \times 10^{14}\,cm^{-3}$).

Double-side polished *n*-type (100) FZ wafers with resistivity of 1 to 5 Ω cm were used in this passivation study. The wafers were cleaned using standard RCA cleaning steps.[18] The wafers were subsequently dipped in 5% HF for 2 min to etch the native oxide and then kept in a cleanroom environment, with ambient average humidity of 50% and temperature of 25 °C, for different durations; during this period the wafers were stored within a typical 25 wafer carrier box. The duration for the growth of facile native oxide layers prior to the deposition of SiN_x was varied from 20 min to 40 000 min. The 100 mm diameter circular wafers were cut into four quadrants prior to the deposition of SiN_x deposition. Silicon nitride deposition was carried out using the Oxford PlasmaLab 100 direct rf PECVD system. During a series of preliminary experiments, it was determined that higher SiN_x deposition temperatures resulted in better passivation, and accordingly all the SiN_x depositions were carried out at 400 °C. While the use of low chamber pressure (200 mTorr) and high plasma power (100 W) has been reported for SiN_x passivation studies using a similar system,[6] our experience indicated significant non-uniformity in film quality. Instead, we found that operating at a higher chamber pressure of 1 Torr and lower plasma power of ∼25 W yielded uniform and reproducible films. Further, the use of higher chamber pressure allowed better convective heat transfer from the substrate holder to the wafer and hence required a lower

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preheating period compared to that at a lower chamber pressure. Operating at higher plasma power increased the deposition rate of SiN_x albeit with no significant change in the passivation quality. Accordingly, all SiN_x depositions were carried out at the low plasma power of ~25 W and chamber pressure of 1 Torr.

Precursor gases for silicon nitride depositions consisted of NH_3, which was held constant at a flow rate of 50 sccm, and 5% silane in nitrogen at flow rates ranging from 200 sccm to 550 sccm. We define the precursor gas ratio (GR) as the quotient of $(SiH_4 + N_2)$ to NH_3 flow rates. The effect of varying the GR from 4 to 7 was explored for samples where the facile native oxide growth time (OGT) ranged from 20 min to 2 K min. A small enhancement in passivation was observed for these relatively short OGTs. On the other hand, excellent passivation enhancement in quality was observed for facile native oxide growth times of the order of 40 K min. For these samples, the GR was varied from 4 to 11. For all samples, the SiN_x deposition time was held constant at 7 min; further, SiN_x was deposited on both sides of the wafer to yield a symmetric set of passivation layers. Thicknesses and refractive indices of the SiN_x films were measured using SOPRA *GES5E* spectroscopic ellipsometer.

The ECD dependent effective minority carrier lifetime, τ_{eff}, was measured using a Sinton Silicon Lifetime Tester WCT-120 system. Transient and quasi-steady-state photoconductance (QSSPC) methods were used to measure injection-dependent τ_{eff} of the sample.[19] Spatial distributions of the lifetime for different samples were measured using Semilab's WT-2000 PVN microwave photo conductance decay (μ-PCD) instrument. Oxide thicknesses were measured using parallel angle resolved x-ray photoelectron spectroscopy (PARXPS). Theta Probe from Thermo Scientific® was used for the PARXPS measurements.

In fitting the data obtained from SE measurements, we included a thin native oxide layer between the cSi substrate and SiN_x layer. Silicon nitride layer thickness of ~93 nm thickness was inferred from the SE measurements which corresponds to a growth rate of 13.3 nm/min. Refractive index (at 633 nm wavelength) increased from 1.9 to 2.06 with increasing silane precursor concentration, i.e., the GR. The increase in the refractive index is consistent with a transition from a sub-stoichiometric to a silicon-rich silicon nitride film.[6]

τ_{eff} values at an excess carrier density of 10^{15} cm^{-3} (unless stated otherwise) were used to calculate the effective SRV, S_{eff},

$$S_{eff} = W/(2\,\tau_{eff}), \tag{1}$$

where W is the thickness of the sample and the bulk lifetime is assumed to be infinite. Fig. 1 shows the effective SRV values at an ECD of 10^{15} cm^{-3} for samples with a range of native OGTs as a function of the GR. It is evident from the figure that the passivation quality for the fSiO$_x$-SiN$_x$ layers generally improves with the facile native oxide growth time and increasing GR. In particular, we find that a reduction in SRV with OGT is moderate up to OGT of 2 K min, however, significant improvement in passivation is observed for OGT of 20 K min and yet a further enhancement for OGT of 40 K min. For the

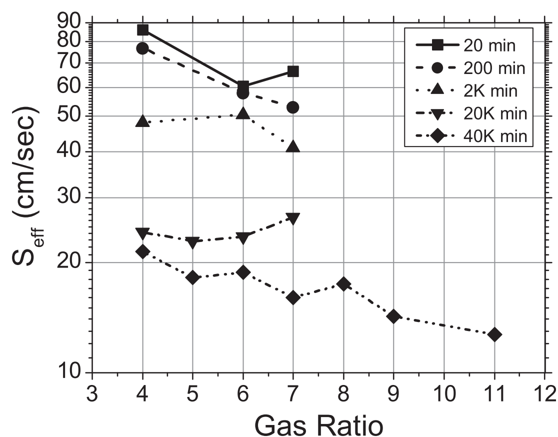

FIG. 1. S_{eff} for an ECD of 10^{15} cm^{-3} for the facile native oxide (fSiO$_x$)-SiN$_x$ passivation schemes. OGT and the GR for the SiN_x deposition were varied.

sample with an OGT of 40 K min, the SRV is reduced further with an additional increase in the GR from 7 to 11.

The high resolution Si_{2p} data measured by Theta Probe were used to fit mixed Lorentzian and Gaussian functions (i.e., Voigt function) with a modified Shirley background. The relative contributions of oxide and elemental silicon signals (percentage contributions) were determined from the fitting. Fig. 2 shows the percentage contributions of oxide and elemental silicon signals varying over a range of incident angles for different oxide growth times. Theoretical percentage contributions were also calculated for the oxide layers on cSi with different oxide thicknesses using the Beer-Lambert equation. Oxide thicknesses were determined based on the best fitting of the measured and theoretical percentage contributions. The measured native oxide thicknesses are of same order of magnitude as reported in Morita *et al.*'s investigation of native oxide growth[20] on *n*-type cSi wafer having a doping concentration similar to that used in this study. It is noted that the XPS measurements carried out by Morita *et al.*[20] used only a single take-off angle of the photoelectrons.

Fig. 3 shows the passivation quality as a function of measured native oxide thicknesses for different OGTs. As

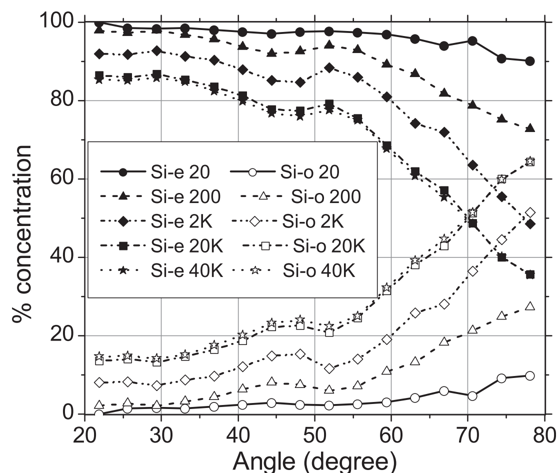

FIG. 2. The relative oxide and elemental silicon signals measured using parallel angle resolved XPS technique, showing contribution of elemental silicon (Si-e) and silicon oxide (Si-o) at different incident angles and oxide growth time.

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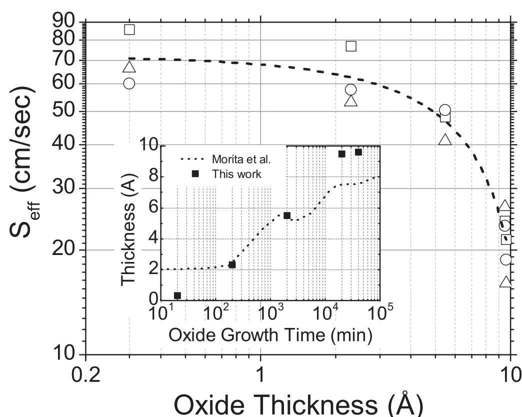


FIG. 3. S_{eff} for different gas ratios (□ GR 4 ○ GR6 Δ GR 7) as a function of the measured facile native oxide thickness measured using PARXPS. The inset shows the measured (this work and by Morita *et al*. (Ref. 20)) native oxide thickness as a function of oxide growth time.

seen from the figure, increase in the native oxide thickness corresponds to an improvement in the passivation quality. The inset shows that the facile native oxide thickness plateaus with oxide growth time to a limiting value of 10 Å. Morita *et al*. reported a limiting oxide thickness of 8 Å.[20]

The surface charge density, Q_S, and defect density, N_S, are inferred from the ECD dependent S_{eff} and simple closed form (SCF) dangling bond interface recombination model.[16,17] The measured and SCF fitted S_{eff} are shown in Fig. 4 for several samples with different native OGT and GR. The extracted Q_S and N_S values are shown in Figs. 5(a) and 5(b), respectively. Notwithstanding some scatter in the data, the average trapped charge density remains essentially unchanged over the range of OGT studied here as well as the GR. However, on average, the interfacial dangling bond defect density decreases with increasing OGT, which corresponds to the observed reduction in SRV. These results indicate the important role of a native oxide layer of less than or approximately 1 nm in thickness, along with hydrogenated silicon nitride, in markedly reducing the defect density at the interface.

A sample with a facile native oxide growth time of 160 K min was also prepared using identical SiN_x deposition

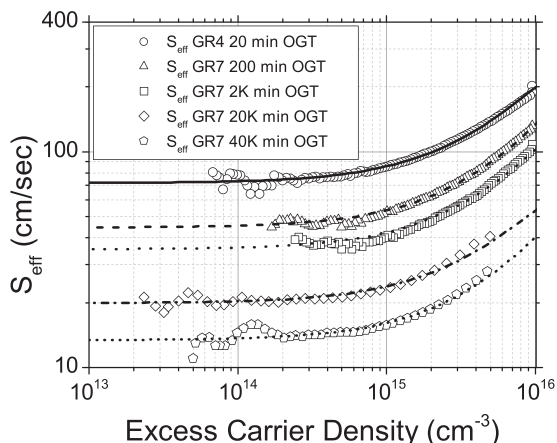
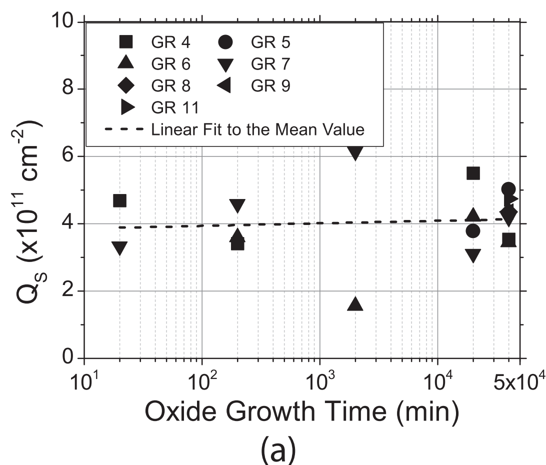


FIG. 4. ECD dependent S_{eff} for different GR and OGT. Lines show the fitting using dangling bond interface recombination model in simple closed form (Refs. 16 and 17).



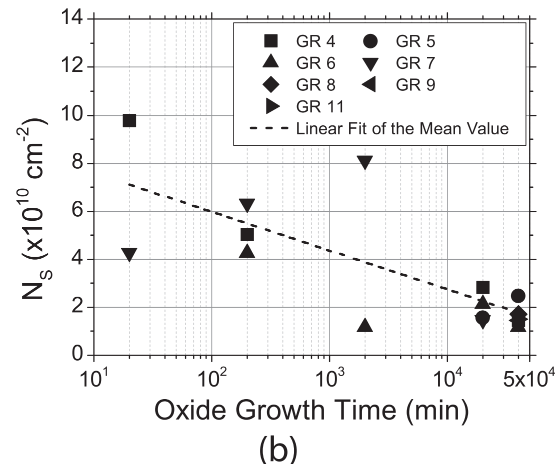


FIG. 5. (a) Interface charge density, Q_S, and (b) dangling bond defect density, N_S, for different GR as a function of OGT. These values are inferred by fitting the ECD dependent S_{eff} values using dangling bond interface recombination model.

conditions stated above and at a GR of 7. Fig. 6(a) shows the spatial profile of the passivation quality measured using the μ-PCD tool. A corresponding maximum lifetime of 1.7 ms was measured which is equivalent to S_{eff} of $\sim$8 cm/s.

Given the observed importance of the facile oxide layer, we also explored the potential of a similar chemically grown oxide playing an equivalent role. Using a 62% nitric acid solution at 60 °C, facile silicon oxide was grown on a quadrant of a cSi wafer by submerging it in the bath for 60 min. The spatial distribution of the passivation attained, for a process that has yet to be optimized, is shown in Fig. 6(b). This result corresponds to a lifetime of 0.76 ms or a SRV of 18 cm/s as measured using the Sinton lifetime tester. Further optimization of the chemically grown oxide and PECVD SiN_x passivation is expected to yield results similar to the native oxide layers grown in ambient atmosphere at room temperature.

The article presents an excellent passivation scheme for crystalline silicon surfaces using facile native $fSiO_x$ and PECVD SiN_x dual layers. The native $fSiO_x$ layer, which is approximately 1 nm in thickness, can be grown readily using a number of equivalent techniques at or near ambient temperature, results in very low dangling bond density at the interface while the field effect passivation due to interface and trapped charges remains essentially unchanged. The low-temperature passivation scheme is potentially amenable

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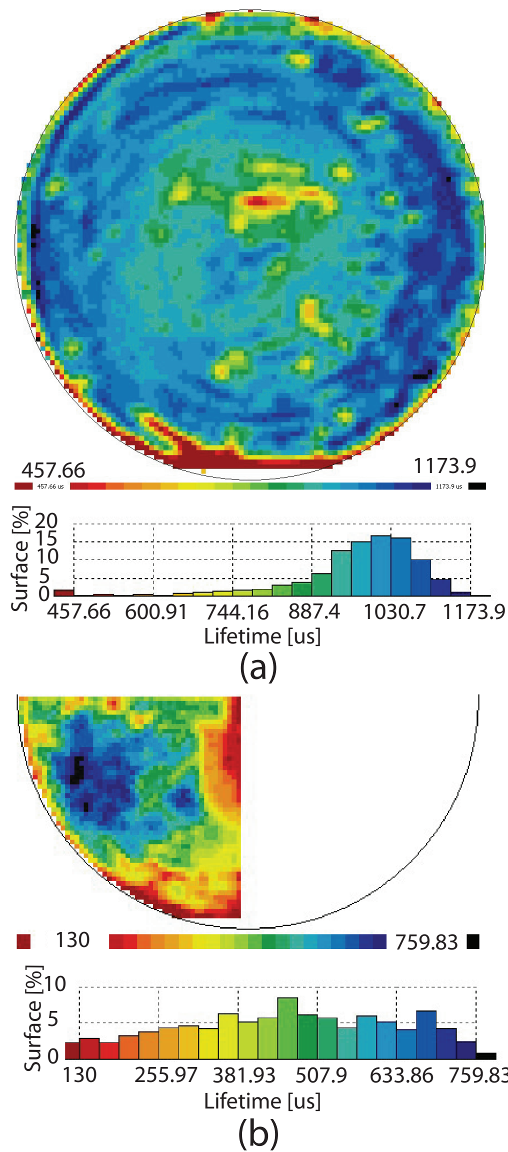

FIG. 6. Spatial profile of the lifetime measured using μ-PCD tool. (a) Native oxide-SiN_x passivation where facile native oxide was grown for 4 months. (b) Chemically grown oxide and SiN_x passivation. HNO_3 solution was used for the oxide growth.

to high-efficiency ultra-thin silicon photovoltaics and allied microelectronic and optical devices.

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[1]M. Taguchi, M. Taguchi, H. Sakata, and E. Maruyama, Sol. Energy Mater. Sol. Cells **95**, 18 (2011).
[2]U. Rau, N. Jensen, and J. H. Werner, in *Proceedings of the 22nd European Photovoltaic Solar Energy Conference, Milan, Italy* (2007), p. 816.
[3]C. Leguijt, P. Lölgen, J. A. Eikelboom, P. H. Amesz, R. A. Steeman, W. C. Sinke, P. M. Sarro, L. A. Verhoef, P. P. Michiels, Z. H. Chen, and A. Rohatgi, Sol. Energy Mater. Sol. Cells **34**, 177 (1994).
[4]Z. Chen, A. Rohatgi, and D. Ruby, in *Proceedings of the IEEE 1st World Conference on Photovoltaic Energy Conversion*, Waikoloa, HI (IEEE, 1994), p. 1331.
[5]T. Lauinger, J. Schmidt, A. G. Aberle, and R. Hezel, Appl. Phys. Lett. **68**, 1232 (1996).
[6]J. Schmidt and M. Kerr, Sol. Energy Mater. Sol. Cells **65**, 585 (2001).
[7]H. Mäckel and R. Lüdemann, J. Appl. Phys. **92**, 2602 (2002).
[8]I. Martin, M. Vetter, A. Orpella, J. Puigdollers, A. Cuevas, and R. Alcubilla, Appl. Phys. Lett. **79**, 2199 (2001).
[9]W. L. Warren, J. Kanicki, J. Robertson, E. H. Poindexter, and P. J. McWhorter, J. Appl. Phys. **74**, 4034 (1993).
[10]G. Dingemans, M. M. Mandoc, S. Bordihn, M. C. M. van de Sanden, and W. M. M. Kessels, Appl. Phys. Lett. **98**, 222102 (2011).
[11]S. Dauwe, L. Mittelstädt, A. Metz, and R. Hezel, Prog. Photovoltaics **10**, 271 (2002).
[12]J. Schmidt, M. Kerr, and A. Cuevas, Semicond. Sci. Technol. **16**, 164 (2001).
[13]S. Narasimha and A. Rohatgi, Appl. Phys. Lett. **72**, 1872 (1998).
[14]Y. Larionova, V. Mertens, N.-P. Harder, and R. Brendel, Appl. Phys. Lett. **96**, 032105 (2010).
[15]M. Hofmann, S. Janz, C. Schmidt, S. Kambor, D. Suwito, N. Kohn, J. Rentsch, R. Preu, and S. W. Glunz, Sol. Energy Mater. Sol. Cells **93**, 1074 (2009).
[16]S. Olibet, E. V.-Sauvain, and C. Ballif, Phys. Rev. B **76**, 035326 (2007).
[17]B. Bahardoust, A. Chutinan, K. Leong, A. B. Gougam, D. Yeghikyan, T. Kosteski, N. P. Kherani, and S. Zukotynski, Phys. Status Solidi A **207**, 539 (2010).
[18]J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology Fundamentals, Practice and Modeling* (Prentice-Hall, Englewood Cliffs, NJ, 2000).
[19]R. A. Sinton and A. Cuevas, Appl. Phys. Lett. **69**, 2510 (1996).
[20]M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, and M. Ohwada, J. Appl. Phys. **68**, 1272 (1990).

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