Excellent Low Temperature Passivation Scheme With Reduced Optical Absorption for Back Amorphous-Crystalline Silicon Heterojunction (BACH) Photovoltaic Device

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***Abstract* — Low temperature processing of silicon photovoltaic (PV) solar cells with excellent passivation quality enables the effective use of ultra-thin wafers for solar cell manufacturing, thus paving the way for high-efficiency low-cost silicon photovoltaics. This article presents Back Amorphous-Crystalline Silicon Heterojunction (BACH) cell performance using low temperature (<= 400°C) facile native oxide-PECVD silicon nitride (SiN_x) dual layer passivation scheme. The cell performance is also compared with the BACH cells fabricated using intrinsic hydrogenated amorphous silicon (*i*-aSi:H) and PECVD SiN_x layer passivation. Reduced optical absorption in the native oxide-SiN_x passivation layer resulted in a higher short-circuit current, J_{SC}, compared to the *i*-aSi:H-SiN_x passivated cells. The fill-factor also improved for the native oxide-SiN_x passivated cells owing to the improved transport properties. The *i*-aSi:H-SiNx passivated cells exhibited optimum cell performance of 10.9% efficiency with V_{OC} of 598.7 mV, J_{SC} of 34.3 mA/cm^2 and fill-factor of 0.531. In contrast, a maximum cell efficiency of 16% is obtained for native oxide-SiN_x passivated cells with V_{OC} of 651 mV, J_{SC} of 35.4 mA/cm^2 and fill-factor of 0.694 for a 1 cm^2 untextured cell (all measurements having been performed under AM 1.5 global spectrum illumination). The above untextured cell performance is a record efficiency for a back amorphous-crystalline silicon heterojunction PV device synthesized using *all* low temperature processes, exceeding the previously reported highest cell efficiency of ~15%.**

***Index Terms* — facile oxide, PECVD nitride, heterojunction, photovoltaic cells, silicon**

I. Introduction

The recently proposed Back Amorphous-Crystalline silicon Heterojunction (BACH) solar cell [1] integrates high efficiency features of heterojunction silicon solar cells and back contact homojunction solar cells. The fabrication of the BACH cell requires only relatively low temperature processing steps. This significantly reduces thermal stress in silicon wafers. Thermal stress can adversely affect the semiconductor properties of the absorber, and complicate the manufacturing process of cells particularly when using very thin wafers.

The low-temperature processed BACH cell avoids shadowing losses by relegating electrical contacts to the back surface, minimizes ohmic losses by maximizing the width of the alternating metal contacts, minimizes surface recombination of carriers through optimum surface passivation and/or configuration of the contacts, and implements favourable light trapping features in order to attain the high conversion efficiency.

The back-contact back-junction cell of SunPower places all contacts at the back or non-light facing side of the cells. It has been demonstrated that it is possible to reach a cell efficiency of 24.2% in mass production [2]. Sanyo has reported [3] a high-efficiency (23%) solar cell using hydrogenated amorphous silicon (aSi:H)-crystalline silicon (cSi) heterojunction with contacts on both sides of a wafer. The Interdigitated Back Contact Silicon Hetero Junction (IBC-SHJ) cell [4] and the Back Enhanced Heterostructure with INterDigitated contacts (BEHIND) cells [5] use configurations similar to the BACH cell. Cell efficiencies of 15% and 10.2% have been reported for IBC-SHJ [4] and BEHIND [5] cells, respectively.

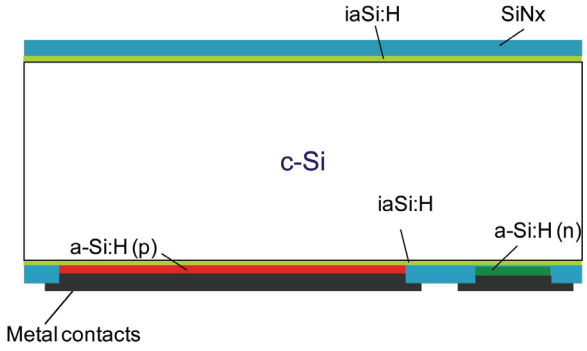
Intrinsic hydrogenated amorphous silicon (*i*-aSi:H) and PECVD silicon nitride (SiN_x) dual layer passivation was used for both IBC-HJ and BEHIND cell fabrication. Thin layer of *i*-aSi:H at the front surface invariably results in optical absorption loss that reduces the short circuit current. The use of *i*-aSi:H as a buffer layer between cSi wafer and the doped amorphous silicon layer however improves the passivation quality of the interface. The open-circuit voltage, V_{OC} typically improves because of the buffer layer but the fill-factor is usually reduced owing to the poor transport of carriers through low mobility *i*-aSi:H layer. Moreover, when thin *i*-aSi:H (~10 nm) is used as part of the passivation scheme the selective etching or removal of this layer while maintaining excellent interface quality is difficult.

An alternative passivation scheme for BACH cell with all low temperature processing is proposed in this study [6]. An ultra-thin layer of facile native oxide (~10Å) grown uniformly at room temperature followed by the deposition of PECVD SiN_x layer at 400°C are used for the passivation of cSi surfaces. Comparison of cell performances between *i*-aSi:H-SiN_x passivation (Scheme 1) and native oxide-SiN_x

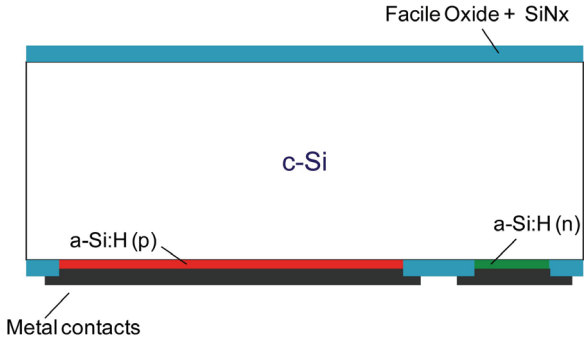
passivation (Scheme 2) illustrate the viability of the novel passivation scheme.

II. CELL STRUCTURE

Fig. 1(a) and 1(b) show the two cell structures used in this study. Two separate *n*-type FZ wafers with 1-5 Ω resistivity double side polished wafers are passivated using *i*-aSi:H-SiN$_x$ and facile native oxide-SiN$_x$ bilayers. The *i*-aSi:H layer and the SiN$_x$ layer thicknesses were approximately 10 nm and 75 nm, respectively. The SiN$_x$ layer on the back surface was selectively etched in order to deposit ~20 nm doped (*n* and *p*) hydrogenated amorphous silicon layers using the DC saddle field technique [7]. Chrome-silver metal layers are deposited on the back using e-beam evaporation.



(a)



(b)

Fig. 1. Schematics of the BACH cell structure using (a) Scheme 1, i-aSi:H and SiNx passivation (b) Scheme 2, facile native oxide and SiNx passivation.

III. EXPERIMENTAL DETAILS

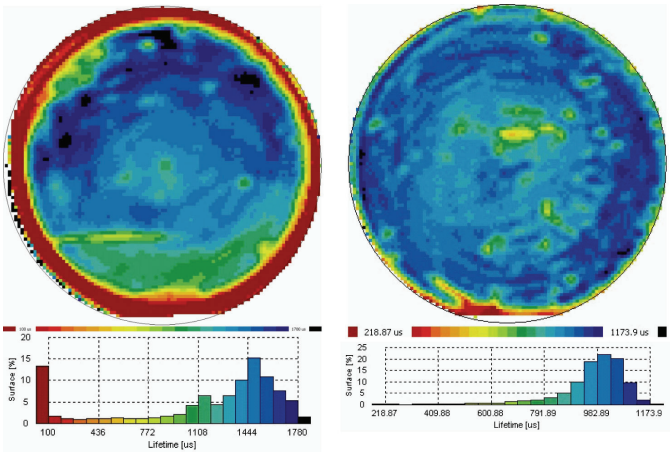
Silicon nitride deposition was carried out using the Oxford PlasmaLab 100 direct rf PECVD system. Optimization of *i*-aSi:H-SiN$_x$ has been reported previously [8]. For Scheme 2 SiN$_x$ layer was deposited on facile native oxide layer at a substrate temperature of 400°C. The chamber pressure for the SiN$_x$ deposition was 1 Torr and rf power was 25 W. Flow rates of NH_3 and silane mixture (5% SiH_4 in N_2) were 50 sccm and 350 sccm, respectively.

The excess carrier density (ECD) dependent effective minority carrier lifetime, τ_{eff}, was measured using a Sinton Silicon Lifetime Tester WCT-120 system. Transient and Quasi-Steady-State Photo-Conductance (QSSPC) methods were used to measure injection-dependent τ_{eff} of the sample. Spatial distributions of the lifetime for different samples were measured using Semilab's WT-2000 PVN Microwave Photo Conductance Decay (μ-PCD) instrument.

The *I–V* characteristics were measured using the neonsee IV AM 1.5 solar simulator. The light intensity was adjusted using a calibrated cell. The aperture cell area of 1×1 cm^2 was defined by a shadow mask on the cell front side.

IV. RESULTS AND DISCUSSION

A maximum minority excess carrier lifetime ~2 ms was obtained for both passivation schemes measured using Sinton Lifetime Testing Instrument. Fig. 2 shows the spatial profile of the passivation quality measured using μ-PCD instrument.



(a) (b)

Fig. 2. Passivation quality of (a) Scheme 1, *i*-aSi:H and SiNx passivation (b) Scheme 2, facile native oxide and SiNx passivation.

Multiple cells were fabricated on a wafer where the cells (of 1 cm^2 total area) had different doped region widths and separation (gap) between doped regions. The width of the *n*-doped aSi:H region varied from 180 μm to 410 μm while the ratio of *p*-doped region width to *n*-doped region width (*p*/*n* ratio) was varied from 2.1 to 2.67. The *n*-width to the gap ratio (*n*/gap ratio) was also varied from 1.5 to 4.

Increased p/n ratio and reduced n/gap ratio resulted in improved cell performance for a particular passivation scheme. The maximum cell efficiency occurred for p/n ratio of 2.67 and *n*/gap ratio of 1.5 for both passivation schemes. The widths of the *n*-doped regions for these cells were approximately 200 μm. Fig. 3 shows the cell performance for the cells with the maximum efficiency for both passivation schemes. As observed in the figure the short circuit current density J_{SC} is higher for passivation Scheme 2 considering the

absence of the absorbing amorphous silicon layer on the front surface. Furthermore, the fill-factor is better for the cells with passivation scheme 2 due to the absence of the buffer layer (*i*-aSi:H) in the rear *p*-*n* and *n*-*n* heterojunctions.

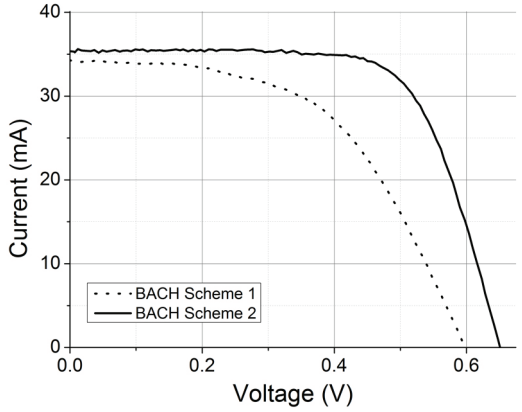


Fig. 3. IV characteristics of highest cell performance for BACH cells with i-aSi:H and SiNx passivation (Scheme 1) and facile native oxide and SiNx passivation (Scheme 2).

The maximum efficiency for the cell passivated with scheme 1 is 10.9% with V_{OC} of 598.7 mV, J_{SC} of 34.3 mA/cm^2 and fill-factor of 0.531. A maximum cell efficiency of 16% is obtained for the cells passivated using scheme 2 with V_{OC} of 651 mV, J_{SC} of 35.4 mA/cm^2 and fill-factor of 0.694. This untextured cell performance with passivation scheme 2 exceeds the highest reported cell efficiency of ~15% [4] which uses a similar configuration and all low temperature processing.

V. Conclusion

An excellent passivation scheme using facile native oxide-SiN_x layers with reduced optical absorption is presented in this article. The performance of PV cells passivated using the proposed passivation scheme are compared to the performance of cells passivated using the more common *i*-aSi:H-SiN_x passivation scheme. Higher values of J_{SC} and FF for the proposed passivation scheme resulted in much improved cell performance (untextured cell efficiency of 16% with V_{OC} of 651 mV, J_{SC} of 35.4 mA/cm^2 and fill-factor of 0.694 under AM1.5 solar spectrum). The demonstrated cell performance is a record efficiency for back contact amorphous silicon-crystalline silicon heterojunction cell concepts utilizing *all* low temperature processing.

Acknowledgement

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