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RESEARCH ARTICLE

Back amorphous-crystalline silicon heterojunction (BACH) photovoltaic device with facile-grown oxide - PECVD SiN_x passivation

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ABSTRACT

This article reports on the integration of facile native oxide-based passivation of crystalline silicon surfaces within the back amorphous-crystalline silicon heterojunction solar cell concept. The new passivation scheme consists of 1-nm thick native oxide and nominally 70-nm thick PECVD silicon nitride. The low temperature passivation scheme provides uniform high quality surface passivation and low parasitic optical absorption. The interdigitated doped hydrogenated amorphous silicon layers were deposited on the rear side of the silicon wafer using the direct current saddle field PECVD technique. A systematic analysis of a series of back amorphous-crystalline silicon heterojunction cells is carried out in order to examine the influence of the various cell parameters (interdigital gap, *n*-doped region width, ratio of widths of *p*, and *n*-doped regions) on cell performance. A photovoltaic conversion efficiency of 16.7% is obtained for an untextured cell illuminated under AM 1.5 global spectrum (cell parameters: V_{OC} of 641 mV, J_{SC} of 33.7 mA-cm^{-2} and fill factor of 77.3%). Copyright © 2014 John Wiley & Sons, Ltd.

KEYWORDS

passivation; native oxide; heterojunction; silicon; low temperature; photovoltaics

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1. INTRODUCTION

Passivation of crystalline silicon (cSi) surfaces is central to the attainment of high-efficiency silicon solar cells. The influence of the quality of surface passivation on device performance becomes even more important as the thickness of silicon wafers is reduced [1]. The International Technology Road Map for Photovoltaics projects that the wafer thickness in silicon solar cells will reduce to 100 μm by the end of the decade [2,3]. Further, over the last several years, a number of research advances suggest the viability of producing ultra-thin silicon foils using both top-down and bottom-up approaches [4]. Within this framework, the use of amorphous-crystalline silicon heterojunction photovoltaics [5,6] coupled with compatible low temperature passivation schemes provide a path for the production of high efficiency silicon foil solar cells. Moreover, integrating the back contact cell concept with low-temperature silicon heterojunction photovoltaics is even more attractive, principally because of the potential of higher short circuit current density. Recently, a high-quality low-temperature passivation scheme using facile grown native oxide (SiO_x) and plasma-enhanced chemical vapor-deposited (PECVD) silicon nitride (SiN_x) has been reported [7,8]. In this article, we undertake a detailed parametric investigation of the back-contact silicon heterojunction photovoltaic cell concept within the framework of this novel passivation scheme; specifically, we avail the optimal facile grown SiO_x-SiN_x bilayer [7].

Several back-contact silicon heterojunction cell designs using all low temperature fabrication processes have been reported recently. The interdigitated back contact silicon heterojunction (IBC-SHJ) cell [9,10] and the back enhanced heterostructure with interdigitated contacts

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(BEHIND) cell [11] use intrinsic amorphous silicon—silicon nitride passivation on both the front (light facing) and rear sides of the wafer. The interdigitated doped amorphous-crystalline silicon heterojunctions and metal contacts are relegated to the back side. For the IBC-SHJ cell, efficiencies as high as 15.7% have been demonstrated for textured surfaces [10] (15% for untextured surfaces [9]). A conversion efficiency of 10.2% has been reported for the BEHIND cell. In both cell designs, the bilayer passivation consists of ∼5 nm *i*-aSi:H and ∼70 nm SiN_x layers. Interdigitated doped amorphous-crystalline silicon heterojunctions were formed by opening appropriate windows in the SiN_x layer on the back side. Use of the *i*-aSi:H layer on the light-facing surface results in parasitic optical absorption losses, while the presence of the passivating *i*-aSi:H layer between the doped aSi:H layers and the cSi absorber presents a transport barrier and thus renders a lower fill factor (FF). A cell efficiency of 19% has been reported for the structuring by laser ablation of silicon heterojunction cell concept that is a back-contact silicon heterojunction cell structure that utilizes laser processing to isolate doped amorphous silicon layers [12].

An alternative cell concept, the back amorphous-crystalline silicon heterojunction (BACH) solar cell, which has reported a conversion efficiency of 8.1%, uses 100-nm thick thermal oxide passivation on both surfaces with appropriate openings in the oxide on the rear side in order to accommodate the doped heterojunctions [13]. While this approach overcomes the parasitic optical absorption losses, the device lacks a front-surface field. Recently, Mingirulli *et al.* [14] have reported cell effciency of 20.2% for back-contact heterojunction cell wherein they introduce a front-surface field through thermal diffusion of phosphorus in the textured front surface followed by consecutive growth of 10-nm thick thermal oxide (SiO_2) and deposition of 70-nm thick PECVD SiN_x on both the front and rear surfaces; appropriate windows are opened in the SiO_2–SiN_x layer on the back side to make the doped heterojunctions. While this result is impressive, the cell concept departs from the low-temperature paradigm of amorphous-crystalline silicon heterojunction photovoltaics. More recently, researchers at LG, Korea have reported a conversion efficiency of 23.4% (unconfirmed) for an IBC-SHJ cell where all process steps are carried out at low temperature [15]. In this case, the cell structure uses a thin layer of *n*-doped amorphous silicon to create the front surface field as well as providing interfacial passivation.

In this article, we report on the integration of the facile-grown native oxide—silicon nitride passivation scheme within the context of the BACH photovoltaic device. The combination of device materials and architecture now affords all low temperature processing, provides excellent interfacial passivation, delivers a front surface field through the trapped charges in the silicon nitride, is free of parasitic optical absorption losses, and renders enhanced transport by relaxing the use of the intrinsic passivating layer in the back junctions. A series of BACH cells having different cell design parameters, principally through the variation of the back interdigitation, are fabricated, characterized, and systematically analyzed. All the cells reported herein were fabricated on untextured crystalline silicon.

2. CELL STRUCTURE

n-type double-sided polished 280-μm thick (100) FZ crystalline silicon wafers with 1- to 5-Ω resistivity were used for the study. Figure 1 shows a schematic diagram of the BACH cell fabricated in this study. As shown in the diagram, the wafers were passivated using facile-grown SiO_x and PECVD SiN_x layers. The facile-grown SiO_x was grown in a controlled clean room ambient at room temperature for a defined period. At the conclusion of the facile native oxide growth period, 70-nm thick SiN_x was deposited using plasma-enhanced chemical vapor deposition (PECVD). Complete details on the growth and characterization of the passivation and surface field properties of the facile-grown SiO_x–SiN_x are presented elsewhere [7]. Subsequently, the facile-grown SiO_x–SiN_x layer on the back surface was selectively etched using buffered oxide etch (BOE) solution to deposit approximately 20-nm thick *n* and *p* doped aSi:H layers. The passivating layer on the front and in the gap regions remained on the substrate through all cell processing steps. Chromium-silver metal layers were deposited on the back surface using *e*-beam evaporation.

Multiple cells each of 1-cm^2 area were fabricated simultaneously on a wafer with different *n*-doped and *p*-doped region widths and varying interdigital gaps between doped regions. The interdigital gap, *g*, was varied from 60 to 200 μm, while the width of *n*-doped region (*n*-width), also referred to as the back surface field (BSF), was varied from 180 to 410 μm. The width of the *p*-doped region (*p*-width), also referred to as the emitter, were set to ∼2.15 or ∼2.67 times that of the BSF. Two cells were fabricated for each cell configuration at different locations on the wafer. Moreover, cells were fabricated on two different wafers resulting in a total of four fabricated cells for a particular cell design parameter. A list of the cell design parameters scanned is given in Table I.

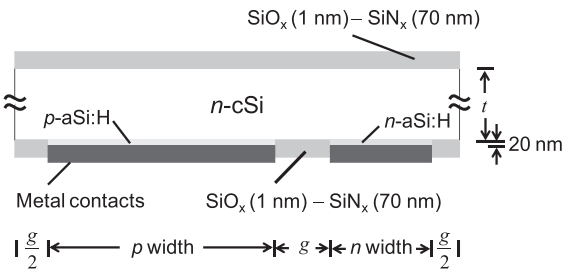

Figure 1. Schematic diagram of the BACH cell using double-sided polished crystalline silicon with facile-grown SiO_x and PECVD SiN_x passivation and surface field.

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Table I. Experimental cell design parameters scanned for the BACH cell concept.

p/*n* ratio	Interdigital gap, g (μm)	*n*-width (μm)	*p*-width (μm)
2.15	60	250	530
2.15	80	330	710
2.15	100	410	890
2.15	160	280	600
2.15	200	350	750
2.67	120	180	480
2.67	160	240	640
2.67	200	300	800

The interdigital gap (*g*), *n*-width, and *p*-width are defined in Figure 1. The *p*/*n* ratio is the quotient of the widths of the *p*-doped and *n*-doped regions.

3. EXPERIMENTAL DETAILS

As-received double-sided polished wafers were dipped in 5% hydrofluoric acid solution following a series of standard RCA cleaning steps [16]. The hydrogen-terminated samples were left in the clean room for a period of the order of a month to grow facile silicon native oxide (SiO_x). Subsequently, silicon nitride was deposited using the Oxford PlasmaLab 100 direct rf PECVD system. Optimization of the deposition conditions for facile-grown SiO_x–SiN_x dual layer passivation has been reported previously [7]. The SiN_x deposition was carried out at a chamber pressure of 1000 mTorr, rf power of 25 W and substrate temperature of 400°C. Flow rates of NH_3 and silane mixture (5% SiH_4 in N_2) were set to 50 and 350 sccm, respectively. The SiN_x film, together with the facile-grown SiO_x, was optimized for excellent surface passivation and selective etching vis-*à*-vis silicon.

Alternative equivalent facile oxide growth techniques amenable at low temperature and yielding much higher growth rates include the use of nitric acid, piranha, and ozone rich ambient; an example of high quality passivation using one of these schemes has been reported in an earlier study [7].

Doped aSi:H layers were deposited on selectively etched regions of the SiN_x layer. Photolithographic processing was used for patterning doped aSi:H and metal layers on the back surface. The silicon wafer, with appropriate openings in the SiN_x layer for the corresponding doped layer, was dipped in 1% HF to etch the native oxide; the HF etching process was carried out in a dry nitrogen atmosphere glovebox. The wafer was then loaded into the direct current saddle field (DCSF) [17] PECVD chamber via a load-lock interface within the glovebox. Amorphous silicon depositions were carried out using a silane (SiH_4) flow rate of 30 sccm at a chamber pressure of 160 mTorr, while maintaining an anode current of 34.5 mA, anode voltage of 600–700 V and substrate temperature of 170°C. The deposition time was set to attain a nominal thickness of 20 nm for the doped layers. Better cell performance was observed for BACH cells with doped aSi:H layers deposited directly on the cSi substrate than for the cells that included a 10-nm thin intrinsic aSi:H layer between the doped aSi:H layer and the cSi substrate. The basis of this result is a function of the current state of development of the intrinsic layers deposited using the DCSF PECVD system. Indeed, introducing thinner (<10 nm) intrinsic layers to take advantage of improved passivation while ensuring minimal degradation of transport properties can further improve the cell performance [6].

Thicknesses of the doped aSi:H layers was measured using a SOPRA GES 5E spectroscopic ellipsometer (SE). Optical model for SE thickness measurement was calibrated against transmission electron microscopy (TEM) measurement and has been reported by Saha *et al.* [18]. The excess carrier density (ECD) dependent effective minority carrier lifetime, τ_{eff}, was measured using a Sinton Silicon Wafer Lifetime Tester WCT-120 system. Transient and Quasi-Steady-State Photo-Conductance (QSSPC) methods were used to measure injection-dependent τ_{eff} of the sample. Spatial distributions of the lifetime for different samples were measured using Semilab's WT-2000 PVN Microwave Photo Conductance Decay (μ-PCD) instrument. The *I*–*V* characteristics were measured using the neonsee IV AM 1.5 solar simulator. The light intensity was standardized using a calibrated cell. The aperture cell area of 1×1 cm^2 was defined by a shadow mask on the cell's front side. The External Quantum Efficiency (EQE) was measured using a 300 W xenon lamp with an Oriel Cornerstone 260 1/4 m monochromator. The cell performance was compared with a Si reference cell that is traceable to the National Institute of Standards and Technology. The reflectance measurements were carried out using a Universal Reflection Accessory in the Perkin Elmer Lambda 1050 UV/VIS/IR spectrometer.

4. RESULTS AND DISCUSSION

Using SE, the refractive index of the ∼1-nm thick native silicon oxide was determined to be comparable with that of bulk silicon oxide, which is 1.46. The refractive index and optical bandgap of the PECVD SiNx were determined to be 2.0 and 3.5 eV, respectively, using SE. Further, the SE-determined native oxide thicknesses were confirmed by independent X-ray Photoelectron Spectroscopy (XPS) measurements reported previously [7].

Figure 2 shows the μ-PCD lifetime distribution in one of the two wafers at the conclusion of the cell fabrication process wherein crystalline silicon was passivated using the facile-grown SiO_x–SiN_x dual layer passivation scheme. The low lifetime regions represent the 1-cm^2 cell areas that include the doped aSi:H and metal layers deposited on the back side of the wafer. The high lifetime regions between the cells reflect the passivation quality and its stability against the cell processing steps. The minority carrier lifetime of the wafer, measured following the application of the passivation layers but prior to any

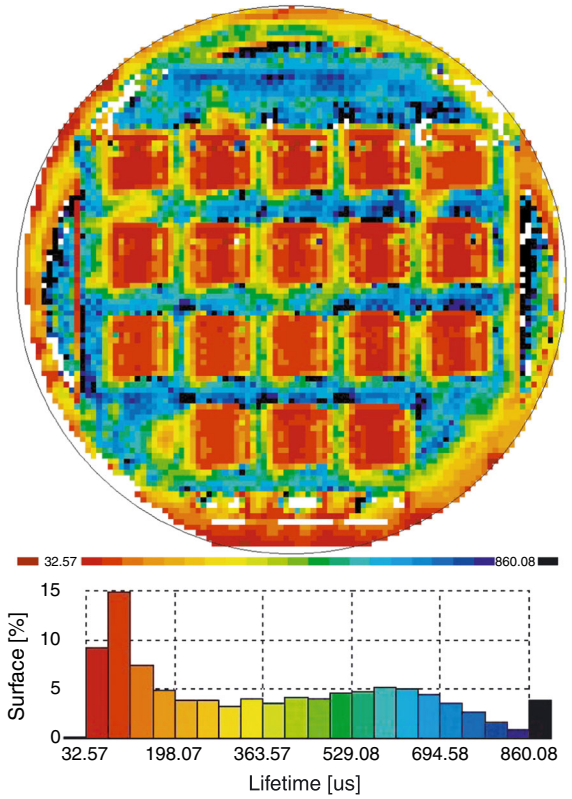

Figure 2. μ-PCD lifetime measurement scan of the front side of one of the two wafers following fabrication of the complete cells, that is, inclusive of the doped aSi:H and metal layers on the back side of the wafer.

cell processing steps, was 1100±100 μs at an ECD of 10^{15} cm^{-3} as determined by the Sinton Silicon Wafer Lifetime Tester.

We analyze the cell performance characteristics in relation to the cell design parameters. Specifically, the cell design parameters of note are the *p*/*n* ratios, the interdigital gap, and *n*-width. The cell data are divided into two broad groups: the first group having a *p*/*n* ratio of ∼2.15 and the second group having a ratio of ∼2.67. The first group is further divided into two sub-groups, one having a smaller interdigital gap (≤100 μm) and the other having a larger interdigital gap (>150 μm), considering the significant influence of the interdigital gap on the short-circuit current, J_{SC}. Average values of four points corresponding to a given cell design parameter are presented in this article. The error bars represent ± one standard deviation.

Figure 3 shows the J_{SC} variation with the interdigital gap. It is observed that the reduction in the interdigital gap generally results in a higher J_{SC} notwithstanding minor variations of the cell design parameters comprising the present study. This result indicates the dominant dependence of recombination losses on the interdigital gap. This is further illustrated in Figure 3(b) which, in addition to showing a decrease in J_{SC} (on average) with increasing *n*-width, indicates a downward shift of J_{SC} with increasing interdigital gap—specifically, for $g > 100$ μm in comparison with $g \leq 100$ μm. Physically, increasing the interdigital gap or the *n*-width or both effectively decreases the collection area for the minority carriers, otherwise referred to as an increase in the electrical shading loss [19,20]. It is also worth noting that the variation in the *p*/*n* ratio does not have a significant influence on J_{SC} for the range of values explored in this experiment.

Fill factors obtained from the cell performance data are observed to be principally influenced by the *n*-width, notwithstanding minor variations of the cell design parameters comprising the present study, as illustrated in Figure 4. The maximum FF (∼76% average for the group and ∼78% the maximum observed for an individual cell)

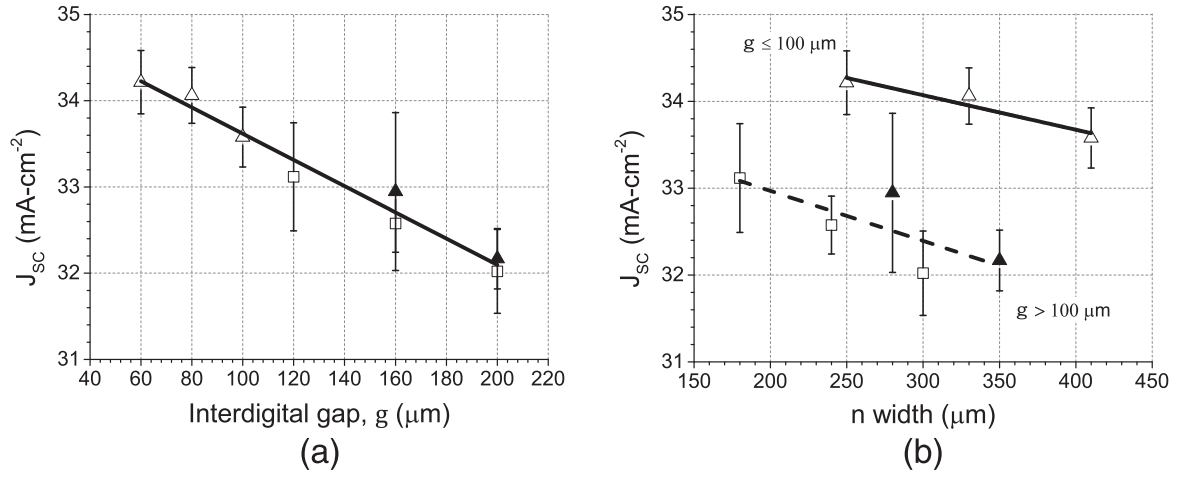

Figure 3. Short circuit current density, J_{SC}, shown as a function of the (a) interdigital gap and (b) *n*-width. △ for *p*/*n* ratio ∼2.15 and interdigital gap ≤100 μm, ▲ for *p*/n ratio ∼2.15 and interdigital gap >150 μm, and □ for *p*/n ratio ∼2.67 and interdigital gap >100 μm. In (a), solid line represents the linear fit of all the data points, and in (b), solid and dashed lines represent the linear fit of the data points for cells with interdigital gap ≤100 μm and interdigital gap >100 μm, respectively.

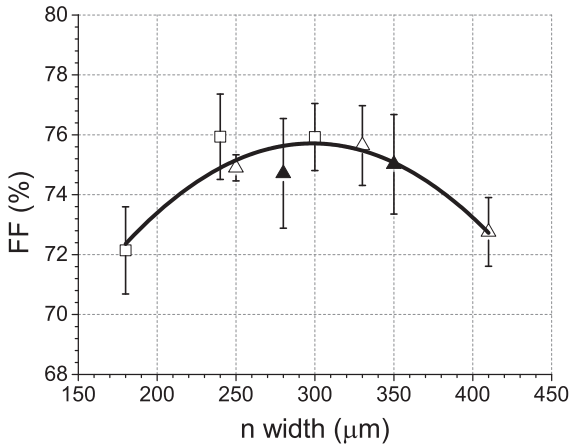

Figure 4. Fill factor (FF) as a function of the *n*-width. △ for *p*/*n* ratio ∼2.15 and interdigital gap ≤100 μm, ▲ for *p*/n ratio ∼2.15 and interdigital gap >150 μm, and □ for *p*/n ratio ∼2.67 and interdigital gap >100 μm. Solid line represents the second-order polynomial fit of the data points.

was obtained for an *n*-width of approximately 300 μm. A detailed analysis of the cell parameters yielding the optimum *n*-width is presented later in this section.

The cell performance can also be analyzed in terms of the equivalent circuit parameters representing the solar cell. We use the standard two-diode model where the current–voltage relationship is expressed by the following:

$$J = J_{SC} - G_P(V + J\,R_S) - J_{01}\left[\exp\left(\frac{V + J\,R_S}{m_1\,V_t}\right) - 1\right] - J_{02}\left[\exp\left(\frac{V + J\,R_S}{m_2\,V_t}\right) - 1\right] \quad (1)$$

where J_{SC} is the photogenerated short circuit current density, R_S is the series resistance per unit area, G_P is the shunt conductance per unit area, and J_{01} and J_{02} are the saturation current densities corresponding to recombination currents associated with ideality factors $m_1 = 1$ and $m_2 = 2$, respectively. The parameter J_{01} physically represents the recombination in bulk and surface, while the J_{02} represents junction recombination. V_t is the thermal voltage. These parameters are extracted from photo *I*–*V* curve using a method described by Merbah *et al.* [21].

From the data presented in Figure 3, we observed that J_{SC} varied with the interdigital gap and *n*-width. We now present the variation in R_S and J_{02} as a function of *n*-width in Figure 5. It is seen that with increasing *n*-width, the series resistance increases, while the junction recombination current decreases. These two counteracting effects result in an optimum *n*-width of approximately 300 μm. It is noteworthy that for a constant *p*/*n* ratio, the effect of increasing *n*-width is an increase in the pitch, hence the observed trends. Junction recombination current density, J_{02}, is also observed to vary with the interdigital gap of the cell as seen in Figure 5(b). This decrease is a reflection of the decrease in current density with increasing *n*-width. Recombination current parameter, J_{01}, varies slightly with *n*-width and is observed to peak at an *n*-width value of ∼330 μm, as shown in Figure 6. The fact that at the optimal value of *n*-width, J_{01} is at its maximum can be understood by noting that under these conditions, the excess carrier density in the cell is maximized and hence the recombination current (J_{01}) is also maximized—notwithstanding that the surface and bulk passivation quality are essentially unchanged. For the cell parameters examined here, a definitive relation between the shunt conductance (G_P) and *n*-width was not readily evident (not shown); the shunt conductance has an average value of 2×10^{-3} Ω^{-1}-cm^{-2}.

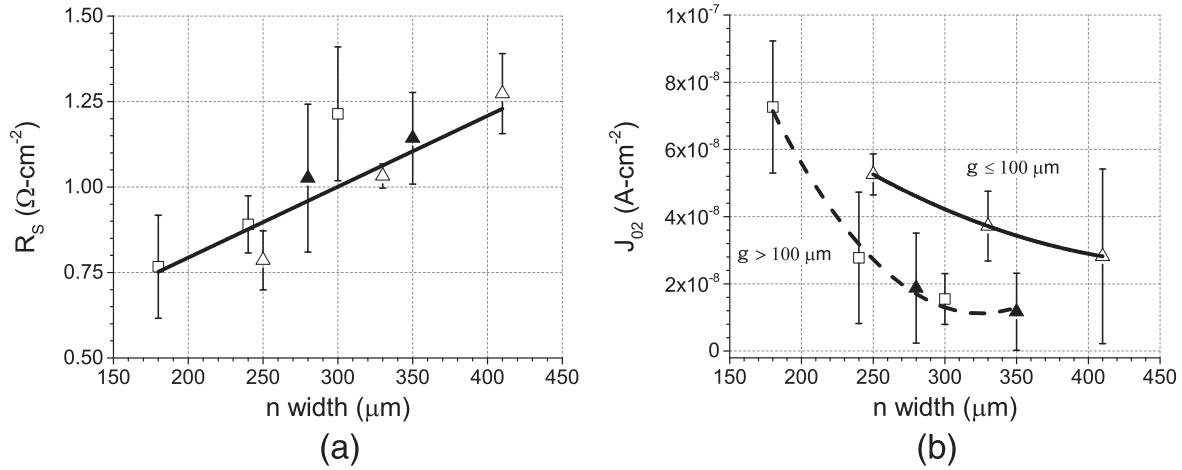

Figure 5. (a) Series resistance, R_s, and (b) junction recombination parameter, J_{02}, as a function of *n*-width. △ for *p*/*n* ratio ∼2.15 and interdigital gap ≤100 μm, ▲ for *p*/*n* ratio ∼2.15 and interdigital gap >150 μm, and □ for *p*/*n* ratio ∼2.67 and interdigital gap >100 μm. The solid line in (a) represents the linear fit of the data points. The solid and dashed lines in (b) are the second-order polynomial fits of the data points for two groups of cells having interdigital gap ≤100 μm and >100 μm, respectively.

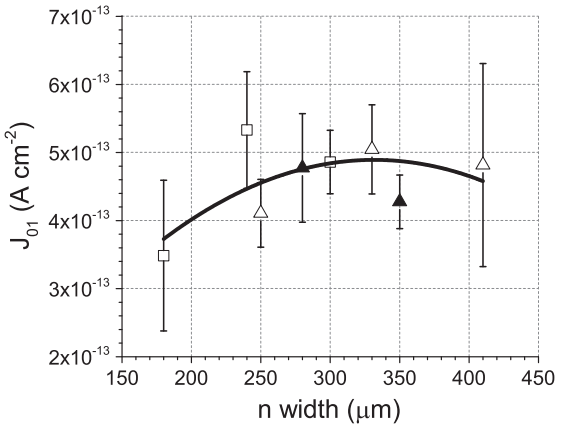

Figure 6. Bulk and surface recombination parameter as a function of *n*-width. △ for *p*/*n* ratio ∼2.15 and interdigital gap ≤100 μm, ▲ for *p*/*n* ratio ∼2.15 and interdigital gap >150 μm, and □ for *p*/*n* ratio ∼2.67 and interdigital gap >100 μm. The solid line represents a second-order polynomial fit of the data points.

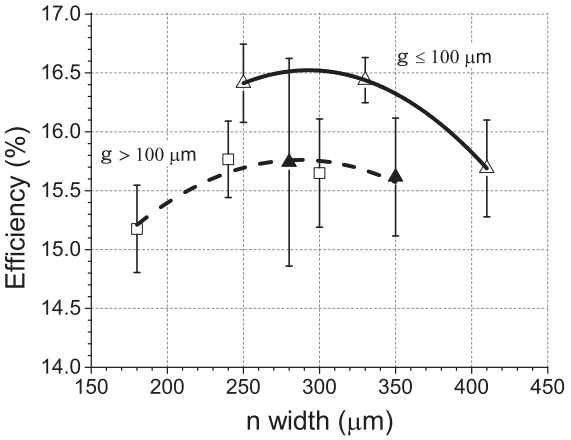

Figure 8. Cell efficiency as a function of *n*-width. △ for *p*/*n* ratio ∼2.15 and interdigital gap ≤100 μm, ▲ for *p*/*n* ratio ∼2.15 and interdigital gap >150 μm, and □ for *p*/*n* ratio ∼2.67 and interdigital gap >100 μm. The solid and the dashed lines represent second-order polynomial fit of the data points for cells with interdigital gap ≤100 and >100 μm, respectively.

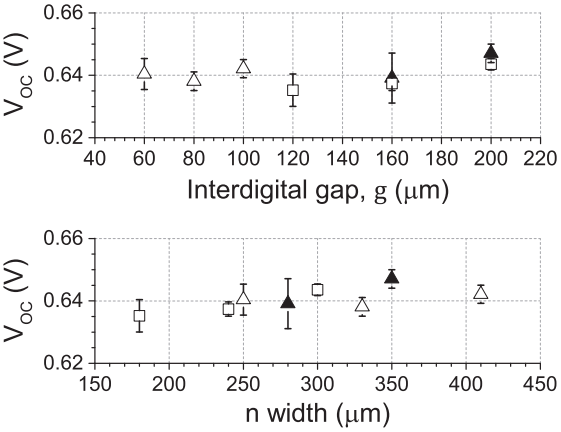

Figure 7. Open circuit voltage, V_{OC}, as a function of *g* and *n*-width. △ for *p*/*n* ratio ∼2.15 and interdigital gap ≤100 μm, ▲ for *p*/*n* ratio ∼2.15 and interdigital gap >150 μm, and □ for *p*/*n* ratio ∼2.67 and interdigital gap >100 μm.

The open circuit voltage, V_{OC}, as a function of the interdigital gap *g* and *n*-width is shown in Figure 7. The average value of the V_{OC} is 641.6 mV with a standard deviation of 4 mV. The small variation of V_{OC} is perhaps because the flat-band structure for all the cells is essentially identical (i.e., *n*-doped and *p*-doped aSi:H layers, cSi absorber, and surrounding passivation layers) notwithstanding the different cell design parameters. It is interesting to observe that the measured V_{OC} is markedly lower than the implied open-circuit voltage of ∼700 mV as determined from the Sinton Lifetime Testing tool. This lower open-circuit voltage is attributed to the poor interfacial passivation at the *p*-doped aSi:H and *n*-cSi junction. The open-circuit voltage can be enhanced through the deposition of high quality doped layers and further by including thin intrinsic hydrogenated amorphous silicon.

Figure 8 shows the efficiency of BACH cells as a function of cell design parameters. The performance of the BACH cell is observed to be influenced by variations in the short-circuit current that is principally due to changes in the interdigital gap and affected by variations in the fill factor that is principally due to changes in *n*-width. It is seen that higher cell efficiencies are obtained for cells with a lower interdigital gap because of the higher short-circuit current density. Further, it is observed that the set of cells within each of the interdigital gap groups (i.e., either $g \leq 100$ or $g > 100$) exhibit a maximum cell efficiency at a common *n*-width of 300 μm, which in turn yields the highest fill-factor.

Finally, Figure 9(a) shows the *I*–*V* characteristics, and Figure 9(b) shows the normalized EQE and reflectivity for the BACH cell fabricated using facile-grown SiO_x–PECVD SiN_x passivation using a double-sided polished wafer. The maximum cell efficiency of 16.7% is obtained with J_{SC} of 33.7 mA-cm^{-2}, FF of 77.3%, V_{OC} of 641 mV under AM1.5 solar radiation spectrum. The EQE is observed to peak around 600 nm, consistent with the reflectance properties of the untextured cell. It is worth noting that within the range of device parameters examined here, the optimal cell design parameters are $g = 60$ μm, *n*-width = 300 μm, *p*/*n* ratio = 2.15. The J_{SC} of the cell can be substantially enhanced through the integration of a texture on the front surface with a bilayer antireflective coating and implementing an optimal cell design. The overall cell performance can be further increased by reducing the series resistance losses of the grids (thicker conductors) and contacts (better matched metal-semiconductor work functions), and improved transport and interfacial

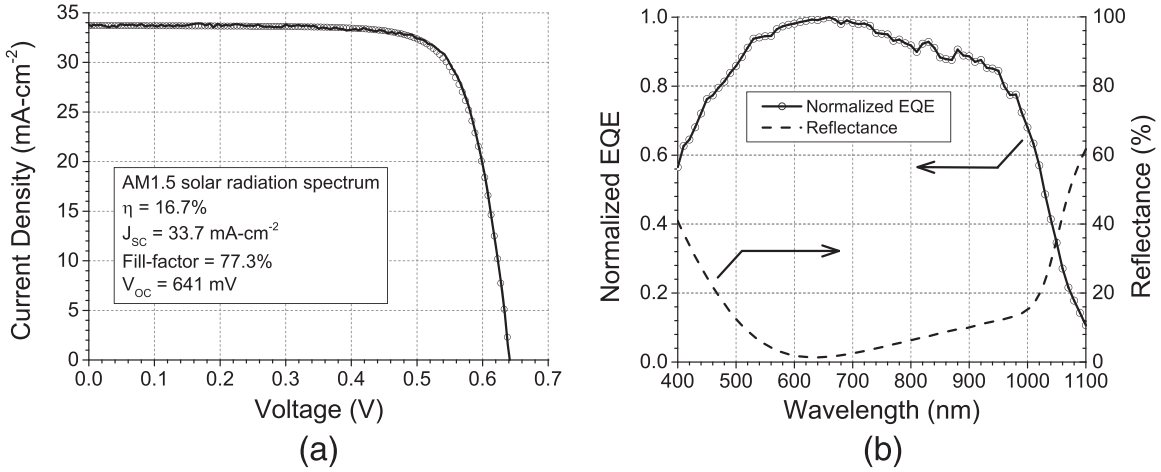

Figure 9. (a) Measured *I–V* characteristics of the BACH cell with the highest cell efficiency and (b) normalized EQE of a typical high efficiency BACH cell and measured reflectance from the front surface of the cell. Solid line in (a) represents the measured data, while the open circles represent the fitted curve using the two diode model.

passivation properties of the hydrogenated amorphous silicon layers.

While in the present study, we have not examined the stress in the SiNx films, reports in the literature show that the use of dual frequency SiNx deposition can mitigate the total stress [22] and thus suggesting the viability of the proposed passivation dielectric bilayer for ultra-thin silicon photovoltaic.

5. CONCLUSION

This article presents experimental results on the BACH solar cell concept using the novel facile-grown SiO_x–PECVD SiN_x passivation scheme. The facile oxide-based passivation of crystalline silicon provides a surface with uniform low surface recombination velocity (SRV), low parasitic optical absorption, and a low temperature synthesis process. The doped amorphous-silicon layers in the BACH cells were deposited using the DCSF PECVD technique. A maximum cell efficiency of 16.7% is reported for a double-sided polished silicon cell for the designs examined in this study. Systematic analysis of BACH cells having a range of cell design parameters (interdigital gap, *n*-width, and *p*/*n* ratio) yields the basis of an optimal cell design. Integration of effective light trapping features, optimal cell design, and further improvement of contacts and amorphous silicon layers define a path to 20% plus facile oxide-based BACH cells.

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